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Revision of AES42-2001

AES standard for acoustics — Digital interface for microphones

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Abstract
This standard describes an extension of the existing digital audio interface AES3 to provide a digital interface for microphones.

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Contents

Foreword

[This foreword is not a part of *AES standard for acoustics — Digital interface for microphones,* AES42-2001.]

This standard has been produced under project AES-X42, Digital Interfacing of Microphones, following the rules of the AES Standards Committee by the SC-04-04 Working Group on Microphone Measurement and Characterization, of the SC-04 Subcommittee on Acoustics.

At the 102nd AES Convention in Munich, Germany, in 1997, Task Group SC-04-04-D, headed by S. Harris, discussed the concept of a digital microphone interface. Two fundamental possibilities of data transmission based on AES3 were considered, an asynchronous mode (mode-1 operation) and a synchronous mode (mode-2 operation). In 1998 a writing body within the task group was set up, headed by K. Konrath to draft a proposal for mode 1. The writing body included J. Binder, D. Flackus, M. Goodman, A. Haupt, H. Jahne, O. Kern, Konrath, J. Kühnast, C. Langen, M. Lienert, W. Niehoff, S. Peus, and H. Wollherr. During three meetings in 1999 the body drafted the proposed standard and presented it during the 106th AES Convention in Munich.

In 1999 and 2000, mode 2 was designed and tested, and has been incorporated into the standard.

The standard notes that the microphone connector remains under consideration. Extensive discussion took place in the working group regarding possible equipment damage resulting from the use of the XLR connector specified by AES3 when voltages and currents could be high enough to damage incorrectly connected equipment. The discussion considered two opposing points:

a) the desirability of consistency in AES3 interface connections;
b) the possibility of connection errors being made.

Some in the group felt that technical personnel would be able to differentiate the connections just as they now do for differentiation of AES3, microphone, and line-level uses of the XLR connector. Others felt that the stresses of field environments would lead to damage. To resolve these points, the working group agreed to specify the XLD connector for applications where producers and users require some assurance against damage. However, the XLD connector is not required and the working group has taken no position on its efficacy.

D. Josephson, chair
J. Green, vice-chair
SC-04-04

Foreword to second edition

After the initial release of AES42, some refinements to the normative part of the standard continued to be discussed, principally on the topic of allocating bits in the command stream for control and reporting of gain and limiter/compressor settings. Accordingly, the principal changes in this document define additional operating features in the command structure so that processing internal to the microphone may be controlled from a mixing console, for example.

The draft was prepared by Task Group SC-04-04-D, which was led by C. Langen.

NOTE In AES standards documents, sentences containing the verb "shall" are requirements for compliance with the standard. Sentences containing the verb "should" are strong suggestions (recommendations). Sentences giving permission use the verb "may." Sentences expressing a possibility use the verb "can."

AES standard for acoustics — Digital interface for microphones

0 Introduction

0.1 Patents

The Audio Engineering Society draws attention to the fact that it is claimed that compliance with this AES standard may involve the use of the US patent 5 051 799 dated 1991-09-24. It may also involve the use of the European Application EP 0766494A1 dated 1995-09-29. This application includes a priority for a US application: 05886656. It may also involve the use of the German patent DE 19606261 dated from 1996-02-06. This application includes a priority for the European Application EP 0794686 and the US patent 6028946.

The AES holds no position concerning the evidence, validity, and scope of these patent rights.

The holder of the US patent right has assured the AES that it is willing to negotiate licenses under reasonable and non-discriminatory terms and conditions with applicants throughout the world. In this respect, the statement of the holder of this patent right is archived with the AES.

The holder of the German patent right has assured the AES that it is willing to negotiate licenses under reasonable and non-discriminatory terms and conditions with applicants throughout the world. In this respect, the statement of the holder of this patent right is archived with the AES.

Information on the European application may be obtained from SGS-Thompson. Information on the US patent 5 051 799 may be obtained from Digital Technology Licensing LLC, C/O General Patent Corporation International, 75 Montebello Road, Suffern, NY 10901 – 3740 USA. Information on the German patent may be obtained from Stage Tec Entwicklungsgesellschaftfür professionelle Audiotechnik mbH, Tabbertstrasse 10, 12459 Berlin, Germany.

Attention is drawn to the possibility that some of the elements of this AES standard may be the subject of patent rights other than those identified herein. The AES shall not be held responsible for identifying any or all such patent rights.

0.2 Conventions used in this standard

0.2.1 Decimal points

According to International Electrotechnical Commission (IEC) directives, the comma is used in all text to indicate the decimal point. However, in the specified coding, including the examples shown, the full stop is used, as in IEC programming language standards.

0.2.2 Data representation

In this standard, all coding and data representations are printed in an equally spaced font.

0.2.3 Non-printing characters

Non-printing characters are delimited by angle brackets, as in <CR> for carriage return..

0.3 Reserved bits

Unless otherwise indicated, bit assignments shown as reserved are reserved for future standardization by the AES, only by means of amendment or revision of this document.

0.4 Precautions regarding equipment damage

The AES holds no position on the issue of possible damage to equipment by users of this document, but draws attention to 4.1, 4.2, and 4.3. Use of this document is voluntary and the AES has no authority to review, certify, or mandate compliance with its provisions, either by its members or by the general public.

1 Scope

This standard describes an extension of the existing digital audio interface AES3 to provide a digital interface for microphones.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this document. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this document are encouraged to investigate the possibility of applying the most recent editions of the indicated standards.

AES3-2003 *AES Recommended Practice for Digital Audio Engineering — Serial transmission format for two-channel linearly represented digital audio data.*

AES14-1992 (r2003) *AES standard for professional audio equipment — Application of connectors, part 1, XLR-type polarity and gender.*

IEC 61938 (1996-12) *Audio, video and audiovisual systems — Interconnections and matching values — Preferred matching values of analogue signals*. Geneva CH: International Electrotechnical Commission.

ISO/IEC 646:1991, *Information technology — ISO 7-bit coded character set for information interchange*. Geneva CH: International Electrotechnical Commission.

3 Definitions and abbreviations

3.1 Definitions

3.1.1 Interface

digital interface compliant with this standard

3.1.2 digital phantom power

DPP

d.c. supply power provided over this interface

3.1.3 mode 1

synchronization mode using no external clock

3.1.4 mode 2

synchronization mode using an external clock

3.1.5 XLD

keyed connector configuration

3.1.6 U-nibble
upper nibble as 4 bit binary coded decimal (BCD) number 0 to 9

3.1.7 L-nibble
lower nibble as 4 bit BCD number 0 to 9

3.1.8 low-cut filter
filter for attenuation of bass effects such as proximity and rumble

3.1.9 zebra ring
striped ring attached to a connector to identify it as XLD

3.2 Abbreviations

3.2.1 LSB
least significant bit

3.2.2 MSB
most significant bit

3.2.3 ADC
analog-to-digital converter

3.2.4 DAC
digital-to-analog converter

3.2.5 MS
stereophonic microphone technique using gradient elements to separate middle and side wavefronts

3.2.6 XY
stereophonic technique using coincident cardioid microphones

3.2.7 ASCII
character set described in ISO/IEC 646

4 Configuration

4.1 AES3 compliance

This interface shall conform to AES3. Users shall exercise caution with regard to the d.c. potentials involved in power circuits for the interface (see 0.4). Digital audio information from an AES3 source shall be received normally by a receiver that conforms to this standard.

If the microphone is a monophonic microphone that does not use one of the single-channel double-sampling-frequency modes, then both AES3 sub-frames shall carry the same information and the AES3 channel status shall be set to indicate single-channel mode (monophonic).

4.2 Connector

See annex F.

4.3 Equipment compatibility

A compliant receiver shall include means such as in 4.2, or other means with or without 4.2, which may include warnings, to avoid damage to analog microphones and to studio equipment. A microphone conforming to this standard shall not be damaged by the application of phantom power conforming to IEC 61938. See 0.4.

4.4 Sampling Frequencies

The microphone shall default to a base-rate sampling frequency of 44,1 or 48 kHz. Other sampling frequencies may be selected as listed in table A17 and using remote control instructions defined in table A17.

5 Power requirements

The limit of common-mode rejection specified in AES3, 8.3.5, shall be extended to 15 V for this standard.

NOTE In principle, this standard describes a method for applying power to any cable-wired mobile AES3 source, although the scope of the standard covers only a digitally interfaced microphone.

5.1 Receiver

A compliant receiver (for example, in a mixing console) shall contain a power supply source with a nominal d.c. voltage of +10 V with a tolerance of +0,5 V to –0,1 V, called the DPP voltage. The maximum ripple on the d.c. voltage shall not exceed 50 mV peak to peak. Additional optional modulation of this voltage is used for transferring remote control data as shown in 6.

The DPP-voltage source shall drive a maximum load current of 250 mA and a peak current of not more than 300 mA (if modulated) charging additional load capacitance (for example, cable capacitance). The voltage source shall be protected against possible short circuits on the cable run.

The DPP voltage shall be applied to both wires of a symmetrical AES3 cable with the ground shield of the cable serving as return path for DPP. To apply the DPP voltage inside the AES3 receiver and transmitter, the optional transformer described in AES3 shall include a center tap at its cable side.

5.2 Transmitter

The transmitter shall consume a maximum DPP supply current of 250 mA. The maximum load capacitance at the DPP-voltage input inside the microphone shall not exceed 120 nF.

6 Remote-control system

The receiver may include a remote-control system controlling possible features of the source device, which are described in annex A. The remote-control data are represented in form of positive pulses added to the DPP voltage, modulating the DPP voltage in this manner. The level of these pulses shall be +2 V ± 0,2 V. The pulse is described in annex B.

The remote-control pulses may be sent as one single burst when activated or, if necessary for synchronization purposes, a burst of remote-control pulses may be sent repeatedly in certain intervals. For frames rates (FR) of 44,1 kHz and 48 kHz the data rate shall be FR/64. For FR of 88,2 kHz and 96 kHz the data rate shall be FR/128. For FR of 176,4 kHz and 192 kHz the data rate shall be FR/256. The data rate is therefore 750 bit/s for frame rates of 48 kHz, 96 kHz, and 192 kHz, and 689,06 bit/s for frame rates of 44,1 kHz, 88,2 kHz, and 176,4 kHz.

7 Synchronization

7.1 Mode-1 operation

A microphone operating in mode 1 shall derive its sample clock internally. The audio signals from multiple mode-1 microphones should be synchronized inside the receiver device; by means of sampling frequency conversion, for example.

A mode-1 microphone is a self-clocking device, which derives its sample clock internally. The audio signals from multiple microphones are synchronized inside the receiver device by means of a sampling frequency converter.

7.2 Mode-2 operation

As an alternative to mode 1, synchronization of microphones shall be performed by using a voltage-controlled oscillator (VCO) and a control voltage, transmitted by using the remote-control pulses of the optional remote-control system described in 6. The VCO and DAC converting the control voltage shall be located inside the transmitter (for example, a microphone). The control voltage shall be processed by a simple phase-locked loop (PLL) system and should be generated by phase-frequency comparison between an external master wordclock and the wordclock of the received microphone. The PLL system shall be located in the receiver (for example, a mixing console). If mode-2 operation is not supported by a receiver, mode-2 microphones shall work in mode 1 automatically. Mode-2 requirements are described in annex C.

NOTE An additional advantage of mode-2 operation is a constant phase relation (close to 0°, compared to the master wordclock, and controlled by the PLL) between different signal sources (microphones) independent of cable length or other influences.

8 Microphone identification (ID) and status flag indicators

Apart from the digital audio bits, additional information may be sent from the transmitter to the receiver unit. For that purpose the user data channel shall be used. The structure, with its possible features such as microphone identification and status information, shall be as described in annex D.

Annex A

(normative)

Remote-control instructions

Control instructions shall be divided into three formats: the simple instruction, the extended instruction, and the manufacturer-specific instruction. Every microphone that supports extended instructions is also required to support simple instructions. Every microphone that supports at least simple instructions shall have a default state that it enters on power up when no instructions have been received. The physical switches located on the microphone shall take precedence over incoming commands.

NOTE The physical switches can have a remote-on position while in other positions the remote-off status bit should be sent to the console (see annex D, status page 1, byte 2).

Implementation of a manufacturer-specific instruction is not included in this standard and is left to the individual manufacturer. However, this standard specifies the framing method for entering and exiting the manufacturer-specific instruction.

A.1 Simple instruction

The simple instruction shall control the most important parameters of the microphone and can be decoded with the minimal amount of digital hardware. This instruction shall have a 2-byte format.

NOTE Two 8-bit shift registers are all that is required to support the minimal command set. Up to four registers may be used to decode the complete set of control parameters specified by the simple instruction.

A.1.1 Data format

The data format of the simple instruction shall be according to figure A.1. An address byte shall be transmitted first, followed by a data byte. Both bytes shall be transmitted MSB first. A break of at least 1-byte length shall be inserted between the data byte and the next command byte to latch the data. See the timing diagram in annex B.

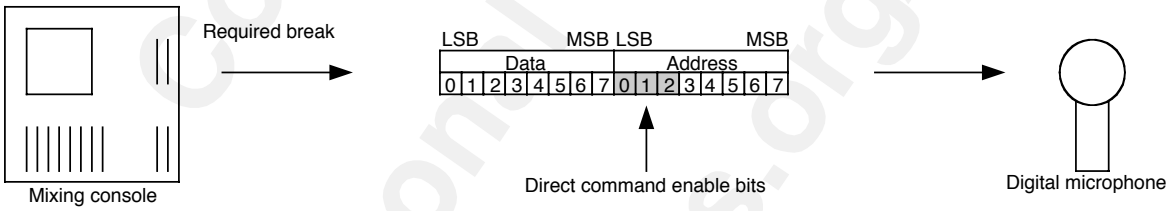


Figure A.1 — Data format of the simple instruction

Three direct-command enable bits (bits 0 to 2) of the address byte shall be used to implicitly select one of up to three direct-command registers located within the microphone. Table A.1 illustrates this addressing scheme.

Table A.1 — Simple instruction addressing scheme

Command type	Extended address bits					Direct-command enable bits		
	7	6	5	4	3	2	1	0
Direct command 1	0	0	0	0	0	0	0	1
Direct command 2	0	0	0	0	0	0	1	0
Direct command 3	0	0	0	0	0	1	0	0

Each bit of the direct-command registers 1–3 shall be responsible for setting the value of a particular parameter within the microphone directly without any additional decoding hardware (see figure A.3) according to table A.2. The functions of the individual bits within the direct-command registers shall be according to tables A.3 through A.9.

Table A.2 — Parameters controlled by direct command registers

Command number	Bit values in the data byte							
	7	6	5	4	3	2	1	0
Direct command 1	Pre-attenuation		Directivity pattern control (4 bit)				Low-cut filter	
Direct command 2	Signal gain (6 bit)						Limiter	Mute
Direct command 3	Synchronization control data							

Table A.3 — Signal pre-attenuation

Bit value	Corresponding setting
00	No attenuation (default)
01	-6 dB (minimum)
10	-12 dB
11	-18 dB (maximum)

Table A.4 — Directivity pattern

Bit value	Corresponding setting
0000	Manufacturer-specific default adjustment (default)
0001	Omnidirectional pattern
0010 to 0100	Increasing directivities
0101	Sub-cardioid
0110 to 0111	Increasing directivities
1000	Cardioid
1001	Increasing directivity
1010	Supercardioid
1011	Hypercardioid
1100 to 1110	Increasing directivities
1111	Figure of eight

Table A.5 — Low-cut filter

Bit value	Corresponding setting
0 0	No filter (default)
0 1	40 Hz
1 0	80 Hz
1 1	160 Hz

Table A.6 — Signal gain

Bit value	Corresponding setting
000000	+ 0 dB (default)
000001	+ 1 dB
000002 to 111111	Increasing at 1 dB per count
111111	+ 63 dB

Table A.7 — Signal limiter

Bit value	Corresponding setting
0	Limiter disabled (default)
1	Limiter enabled

Table A.8 — Mute function

Bit value	Corresponding setting
0	Mute off (default)
1	Mute on

Table A.9 — Protocol of synchronization data

Bit value	Corresponding setting
11111111	Maximum positive tuning of VCO
10000000	Center frequency of VCO
00000000	Maximum negative tuning of VCO

A.1.2 Synchronization control word extension

To increase resolution of the control word from 8 bit to 13 bit, the 5 extended address bits may be used as LSB extended data of the synchronization control word. Direct-command bit 7 should be MSB of this lower bit field and direct-command bit 3 should be LSB of the lower bit field.

NOTE A detailed description of the synchronization method can be found in annex C. The extension of the resolution of synchronization data is fully compatible with low-resolution systems and vice versa. The extension can reduce jitter.

A.2 Extended instruction

The extended instruction format allows access to 31 additional commands, many of which are not currently implemented and are reserved. Two bytes shall be used. The data format shall be the same as the simple instruction, but the addressing scheme should be different. The data format of the extended instruction shall be according to figure A.2.

NOTE If the number of commands specified herein becomes insufficient for future use, more address space can be obtained by adding another address byte. The byte can be sent first, so those microphones able to work with only one address byte can ignore the additional byte. 256 additional commands can be addressed but the regular address byte, defined in A.1.1, should be set to default (all zero).

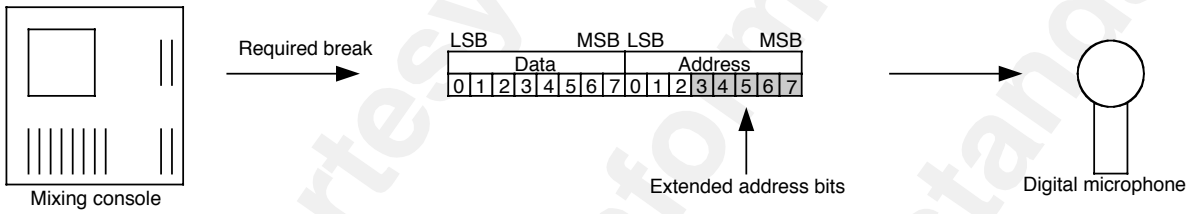


Figure A.2 — Data format of the extended instruction

Five extended address bits (bits 3 to 7) shall contain the address for 31 additional commands as well as the default command (command 0). The addresses of additional commands (commands 4 to 34) can be decoded out of these 5 bits. Table A.10 illustrates this addressing scheme.

Table A.10 — Extended-instruction addressing scheme

Command type	Extended address bits					Direct command enable bits		
	7	6	5	4	3	2	1	0
Command 0 (default)	0	0	0	0	0	0	0	0
Command 4	0	0	0	0	1	0	0	0
Command 5	0	0	0	1	0	0	0	0
Command 6	0	0	0	1	1	0	0	0
Command 7	0	0	1	0	0	0	0	0
Command 8	0	0	1	0	1	0	0	0
Command 9 to Command 33	(continued count)					0	0	0
Command 34	1	1	1	1	1	0	0	0

Table A.11 describes the functions controlled by the additional commands (commands 4 to 34). Tables A.12 through A.21 detail the additional commands.

Table A.11 — Functions of additional commands addressable through extended address bits

Command	Function							
	7	6	5	4	3	2	1	0
4	Page request		Reset	ADC calibrate	Test signal		Light control	
5	Reserved	Sampling frequency			Dither and noise shaping			
6	MS-XY select	Balance width						
7	Equalization curve select							
8	Reserved						Stereo	Polarity
9	Reserved							
10 to 28	Reserved							
29	Compressor/limiter release time				Compressor/limiter attack time			
30	Comp./lim. peak limit	Reserved	Side chain frequency response		Reserved	Compressor/limiter ratio		
31	Comp./lim. enabled	Reserved	Compressor/limiter threshold (-dBFS)					
32	Brightness light 1				Brightness light 2			
33	Manufacturer-specific instruction begin							
34	Manufacturer-specific instruction end							

NOTE A microphone ID-status request is not needed, because the microphone sends it automatically.

Table A.12 — Page request

Bit value	Corresponding setting
00	Page 0 (default)
01	Page 1
10	Page 2
11	Page 3

Table A.13 — Reset

Bit value	Corresponding setting
0	No reset (default)
1	Reset

Table A.14 — ADC calibration

Bit value	Corresponding setting
0	No calibration (default)
1	Calibrate ADC

Table A.15 — Test signal

Bit value	Corresponding setting
0 0	No test signal (default)
0 1	Test signal 1 (under consideration)
1 0	Test signal 2 (under consideration)
1 1	Test signal 3 (under consideration)

Table A.16 — Light control

Bit value	Corresponding setting
0 0	No light (default)
0 1	Light 1
1 0	Light 2
1 1	Both lights

Table A.17 — Sampling frequency

Bit value	Corresponding setting
0 0 0	44,1 kHz
0 0 1	48 kHz
0 1 0	88,1 kHz; multiple = 2
0 1 1	96 kHz; multiple = 2
1 0 0	176,4 kHz; multiple = 4
1 0 1	192 kHz; multiple = 4
1 1 0	352,8 kHz; multiple = 8
1 1 1	384 kHz; multiple = 8

Table A.18 — Dither and noise shaping

Bit value	Corresponding setting
0000	Dither and noise shaping off (default)
0001	(under consideration)
0002 to 1110	(under consideration)
1111	(under consideration)

Table A.19 — MS or XY Select

Bit value	Corresponding setting
0	XY stereo (default)
1	MS stereo

Table A.20 — XY balance, MS width

Bit value	Corresponding setting		
	Left channel	Right channel	Balance
0111111	1,0	0,0	Left (A) channel only
0000000	0,5	0,5	Center (default)
1000000	0,0	1,0	Right (B) channel only

Signed 2's complement notation shall be used to encode the channel weights. Bit 7 is sign extension = -2^0, bit 6 = 2^{-1} and so on until bit 0 = 2^{-6}.

Table A.21 — Equalization-curve select

Bit value	Corresponding setting
00000000	No equalizer (default)
00000001	Manufacturer-specific equalization
00000002 to 11111110	Manufacturer-specific equalization
11111111	Manufacturer-specific equalization

Table A.22 — Polarity Select

Bit value	Corresponding setting
0	0° - No polarity reverse (default)
1	180° - Polarity reverse

Table A.23 — Stereo/Mono Select

Bit value	**Corresponding setting**
0	Stereo setting for stereo microphone (default)
1	Mono setting (both channels transmit same signal)

Table A.24 — Compressor/limiter attack time

Bit value	**Corresponding setting**
0000	0 ms (default)
0001	0.1 ms
0010	0.3 ms
0011	1 ms
0100	3 ms
0101	10 ms
0110	30 ms
0111	100 ms
1000	Auto attack mode 1
1001	Auto attack mode 2
1010	Auto attack mode 3
1011	Auto attack mode 4
1100	Auto attack mode 5
1101	Auto attack mode 6
1110	Auto attack mode 7
1111	Auto attack mode 8

Table A.25 — Compressor/limiter release time

Bit value	Corresponding setting
0000	Manufacturer specific release time (default)
0001	50 ms
0010	0.1 s
0011	0.2 s
0100	0.5 s
0101	1 s
0110	2 s
0111	5 s
1000	Auto release mode 1
1001	Auto release mode 2
1010	Auto release mode 3
1011	Auto release mode 4
1100	Auto release mode 5
1101	Auto release mode 6
1110	Auto release mode 7
1111	Auto release mode 8

Table A.26 — Compressor/limiter ratio

Bit value	Corresponding setting
000	1,2 : 1
001	1,5 :1
010	2 :1
011	3 : 1
100	4 : 1
101	6 : 1
110	8 : 1
111	∞ : 1 (limiter)

Table A.27 — Side chain frequency response

Bit value	Corresponding setting
0 0	Flat
0 1	1 kHz low-pass filter
1 0	2 kHz low-pass filter
1 1	4 kHz low-pass filter

Table A.28 — Compressor/limiter peak limit

Bit value	Corresponding setting
0	Peak limiter Off (default)
1	Peak limiter On

Table A.29 — Compressor/limiter threshold (-dBFS)

Bit value	Corresponding setting
0 0 0 0 0 0	0 dB
0 0 0 0 0 1	-1 dB
0 0 0 0 0 2 to 1 1 1 1 1 0	Increasing at 1 dB per count
1 1 1 1 1 1	-63 dB

Table A.30 — Compressor/limiter enable

Bit value	Corresponding setting
0	Compressor/limiter disabled (default)
1	Compressor/limiter Enabled

Table A.31 — Brightness light 2

Bit value	Corresponding setting
0 0 0 0	Brightness 1 (dark)
0 0 0 1	Brightness 2
0 0 0 2 to 1 1 1 0	(continued increments)
1 1 1 1	Brightness 16 (bright)

Table A.32 — Brightness light 1

Bit value	Corresponding setting
0000	Brightness 1 (dark)
0001	Brightness 2
0002 to 1110	(continued increments)
1111	Brightness 16 (bright)

A.4 Hardware example, simple instruction mode

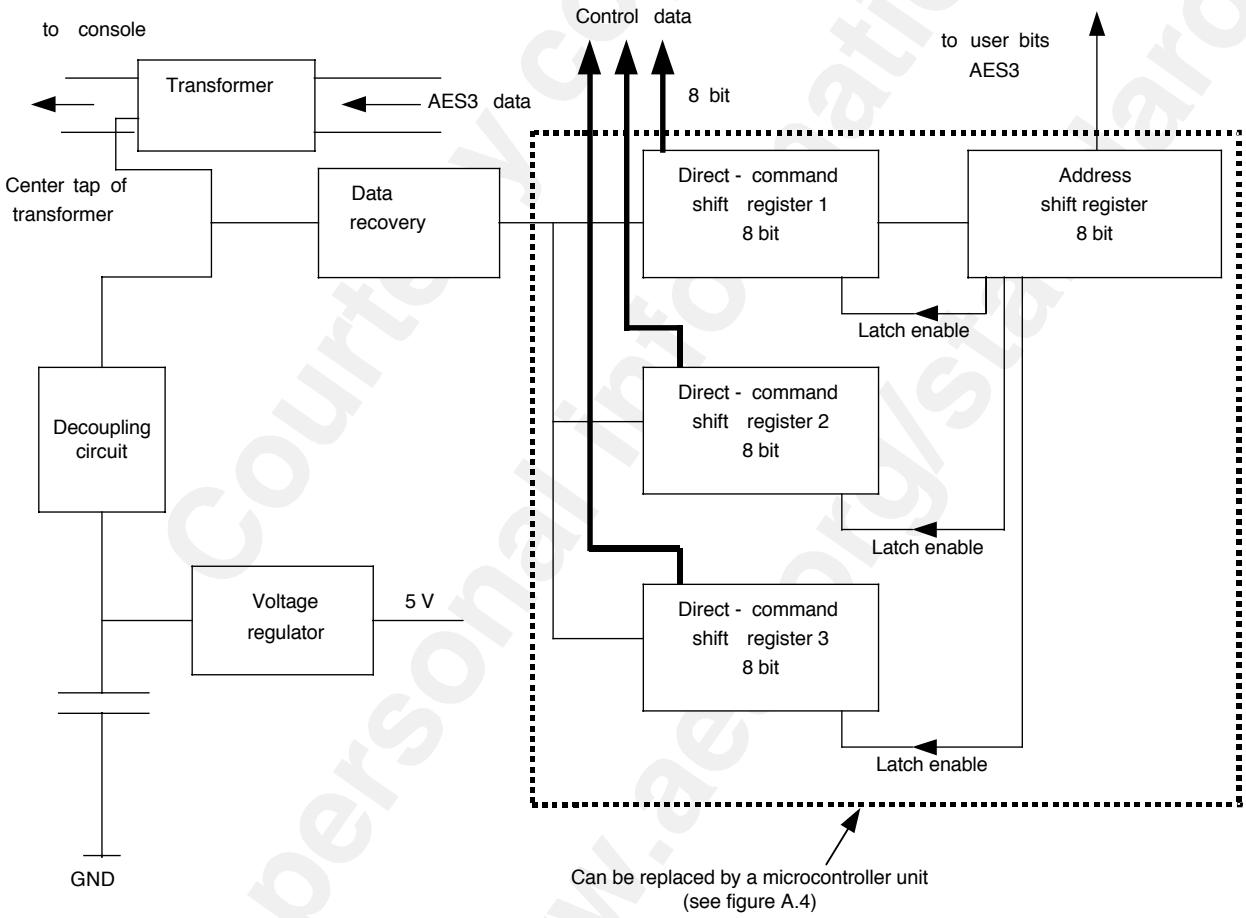


Figure A.3 — Hardware example, simple instruction mode

The decoupling of the remote control pulses is achieved by using the center tap of the transformer or equivalent circuit. A capacitor reduces the effects of radio-frequency interference in the cable. A decoupling circuit makes it possible to use higher data rates even though a large capacitor is needed in front of the voltage regulator to smooth out the voltage. Without the decoupling circuit, this large capacitor together with the cable resistance would constitute a low-pass filter and limit the maximum data rate.

The incoming data will be latched by several shift registers (direct-command shift registers 1 to 3 and address shift register) connected in parallel. The address byte is received in first and will be shifted through the direct-command shift registers and then latched in the address shift register. One of the three direct-command shift registers will be enabled by the related direct-command enable bits and will directly control hardware (command bytes 1 to 3). If a very simple microphone just controls the basic features (for example, features in command byte 1) it is possible to implement only direct shift register 1 and address shift register. The address shift register will be read out by a microcontroller according to the 5-bit address in the address byte (five MSBs) to use command bytes 4 to 35. The structure may also be implemented using a microcontroller or digital signal processing (DSP) solution.

A.5 Hardware example, extended instruction mode

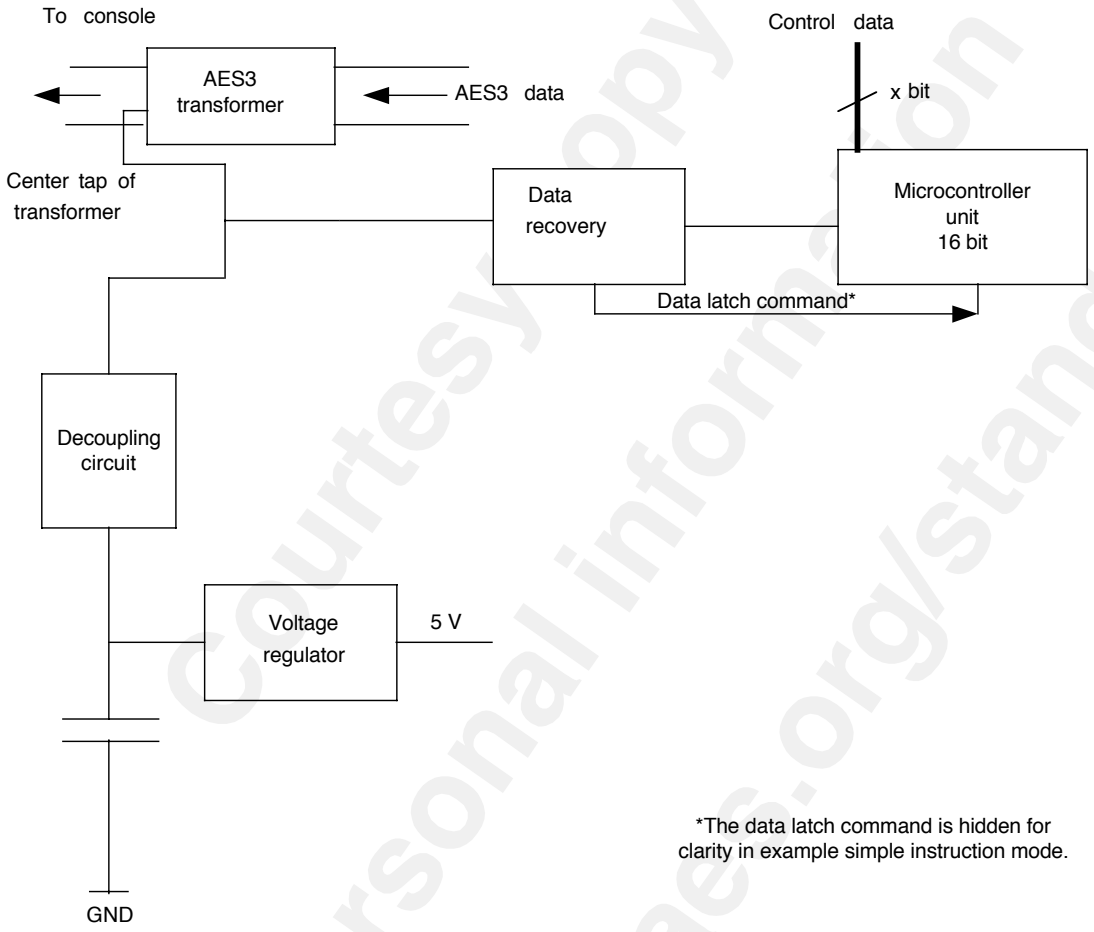
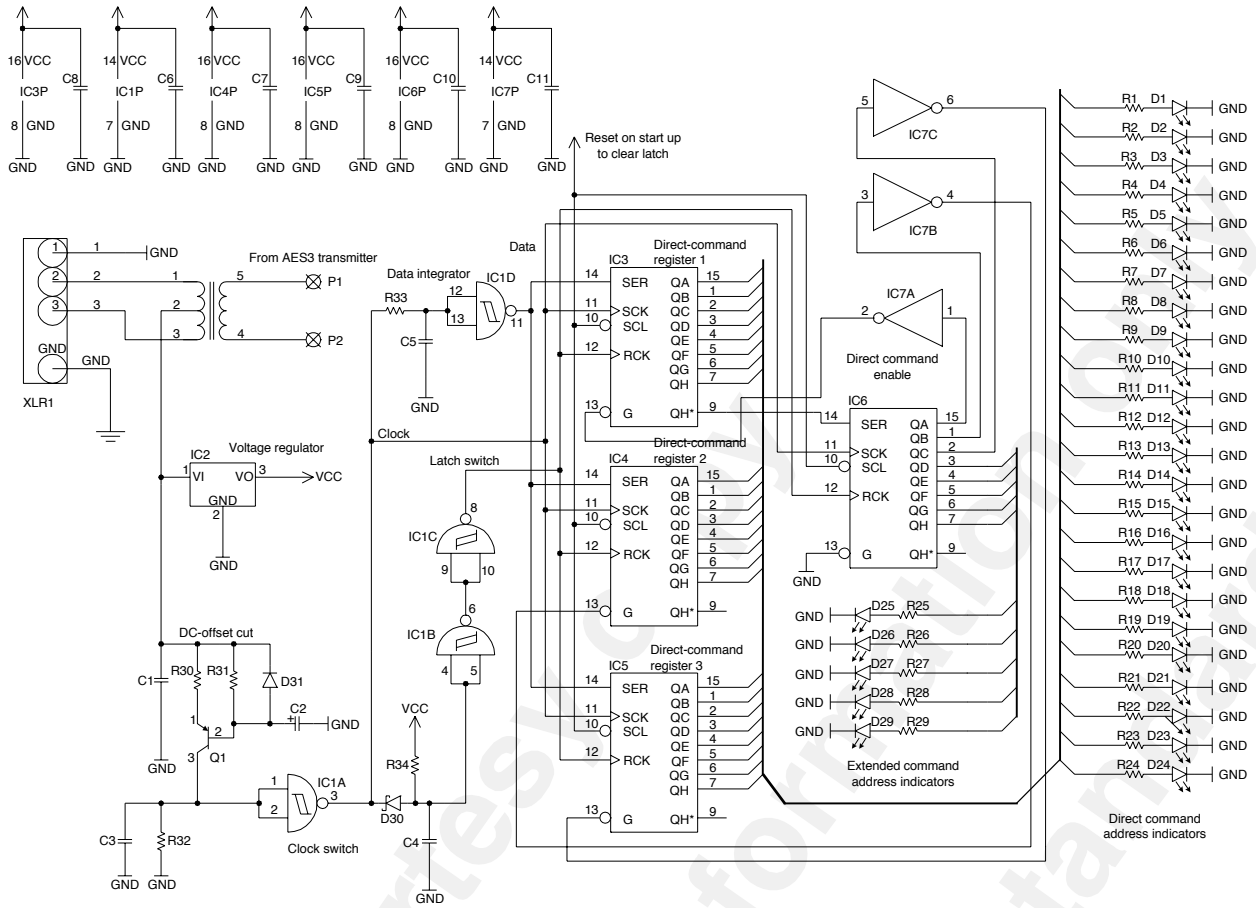


Figure A.4 — Hardware example, extended instruction mode



Components:

C1	capacitor	100 nF
C2	capacitor	10 μF
C3	capacitor	120 pF
C4	capacitor	15 nF
C5	capacitor	15 nF
C6 to C11	capacitor	10 nF
D1 to D29	low current LED	(for example, HPMP-K150)
D30	Schottky diode	BAT43
D31	signal diode	
IC1	Schmitt trigger	74HC132
IC2	voltage regulator	7805
IC3 to IC6	shift register	74HC595
IC7	inverter	74HC04
Q1	pnp transistor	BC557
R1 to R29	resistor	1,5 kΩ
R30	resistor	1 kΩ
R31	resistor	100 kΩ
R32	resistor	10 kΩ
R33	resistor	33 kΩ
R34	resistor	1 MΩ
TR1	transformer according to AES3, 6.1, with added center tap	
XLR1	XLR3 or XLD3 male connector	

Figure A.5 — Hardware example, data recovery

Annex B

(normative)

Structure of remote-control pulses

a) Positive pulses with different widths shall be added to DPP voltage with a peak-to-peak amplitude of 2 V ± 0,2 V

b) The data rate bit stream of these pulses shall be 750 bit/s at 48 kHz sampling frequency or multiples or 689 bit/s at 44,1 kHz (or multiples). It is given as the ratio of f_s/64 at sampling frequencies f_s = 48 kHz or 44,1 kHz.

c) A logical `1` shall be represented by a pulse width of 7 x 64/(8 f_s).

d) A logical `0` shall be represented by a pulse width of 1 x 64/(8 f_s).

e) The distance from a logical `0` pulse to the end of the last pulse shall be 7 x 64/(8 f_s).

f) The distance from a logical `1` pulse to the end of the last pulse shall be 1 x 64/(8 f_s).

g) A complete byte shall need a time of 8 x 64/f_s.

h) Command and data byte, transmitted in one block, shall need 16 x 64/f_s (for example, 21,28 ms at f_s=48 kHz).

i) An extended command byte preceding the regular command byte may be added to extend control features in the future.

j) There shall be no interrupt during transmission of pulses between extended command (optional), command, and data bytes.

k) A minimum break time of 8 x 64/f_s (1 byte) shall be set between different command-data byte blocks.

l) The end of any command-data block is defined by a minimum break time of 4 x 64/f_s to enable data latching in the microphone before the next command-data block can be received (see k).

m) The command and data byte shall be sent with the command byte first and with the MSB first and the LSB last.

n) The rise and fall times (from 10 % to 90 % of the amplitude) of the pulses shall be 10 μs ± 5 μs independent of the permitted load conditions (d.c. = 50 mA to 250 mA, C_{load} = 0 to 170 nF, including cable capacitance).

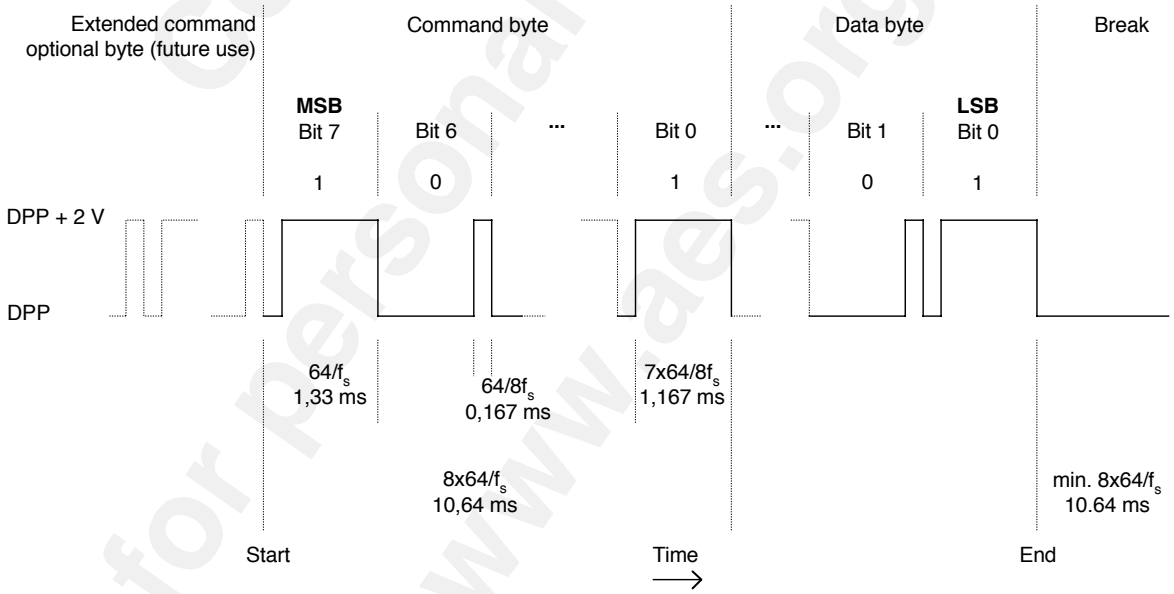


Figure B.1 — Bit structure with 48 kHz sampling frequency

Annex C

(normative)

Synchronization of digital microphones, Mode 2

C.1 Description of mode 2

In mode 2, synchronization of the microphone clock to an external master clock shall be performed by means of a simple PLL circuit controlling a VCO inside the microphone. Specifications of the system are listed below.

C.1.1 Circuit locations

The frequency-phase comparison and generation of the digital control signal shall be performed inside the receiver. Inside the microphone the control signal is recovered from the remote-control data stream and is converted to directly obtain the VCO control voltage.

C.1.2 Transmission of control signal

The generated control signal shall be sent continuously to the microphone according to the principles and protocol described for the remote-control system in annexes A and B.

C.1.3 Compatibility with mode 1

As long as no control signal is sent to a mode-2 microphone after power on, it shall operate in mode 1 (see 7.1) with the VCO running on frequencies according to AES11 specifications, that is, the control voltage should be set internally to the default value. When operating in mode 2, interruption of the transfer of the VCO control signal should result in the control voltage being stored with its last value.

C.1.4 Mode-2 identification

A mode-2 microphone shall send identification according to annex D to the receiver. The receiver shall automatically switch to mode-2 operation when this ID is received and mode 2 is supported.

C.2 Specification of PLL circuit

These specifications for the PLL circuit should be used to provide stable operation and compatibility between all mode-2 transmitters and receivers. The specifications are valid for a frequency-phase comparison working on a 48 kHz or a 44,1 kHz sampling frequency. Because of linear proportionality between comparison frequency and loop gain, in 88,2 kHz, 96 kHz, or higher sampling frequency systems, frequency dividers should be used or loop gain should be reduced directly. For example, double the value of C2 and half the value of R3 in figure C.1.

C.2.1 General requirements

Resolution of control signal	8 bit to 13 bit
Accuracy of ADC and DAC	± 1/2 LSB, monotonic
Minimum transmission rate of control signal	6 Hz (every fifth command data byte)

C.2.2 Receiver requirements

Phase comparator type	frequency-phase (zero-degree)
PLL characteristic	proportional, integrating, differentiating (PID)
Proportional constant K_p	1 LSB at 163 ns time error (that is, 2,8° at 48 kHz)
Integration time constant K_i	1 LSB/s at 163 ns time error
Differential constant K_d	1 LSB at 163 ns/s change of time error
Differential signal, maximum gain	8 LSB at 163 ns time error (fast change)
Required master clock accuracy	± 50 ppm

C.2.3 Transmitter requirements

VCO - basic accuracy	± 50 ppm
VCO - minimum tuning range	± (60 ppm + basic accuracy)
VCO – maximum tuning range	± 200 ppm
VCO - tuning slope	positive, f_{max} for control data = $0FF_{16}$
Control voltage LP-filter characteristic:	
d.c.-gain	1 (0 dB)
stage 1, first-order type	f_c = 68 mHz
maximum attenuation, f > 10 Hz	24 dB constant
stage 2, first-order type	f_c = 12 Hz

C.3 Functional diagram and hardware example

The function blocks drawn inside dashed borders designate the components used for mode-2 operation. The PID characteristic is given by the following components:

proportional gain	R3 / R1
integrating constant	C2, R1
differentiating constant	C1, R3
maximum differential signal gain	R3 / R2

C3 is used for averaging phase-frequency comparator pulses. The averaging time constant (C3, R3) should not exceed 10 ms. For the specified values it is assumed that the input voltage range of the ADC is given as ground to power supply voltage (V_{cc}), and that the phase-frequency comparator generates pulses of ± V_{cc}/2 relative to V_{cc}/2 (=V_{ref}). Other ratios of ADC input voltage range to phase-frequency comparator pulses will influence loop gain directly, and have to be considered by adjusting component values R3 and C2 accordingly.

The VCO control voltage in the microphone is to be processed by LP-filtering with the characteristic described in C.2.3 and shown in figure C.1 by the components R5, R6, C4, and C5. The components R7 and D1 are optional to decrease lock time after power on from about 6 s to 1,5 s.

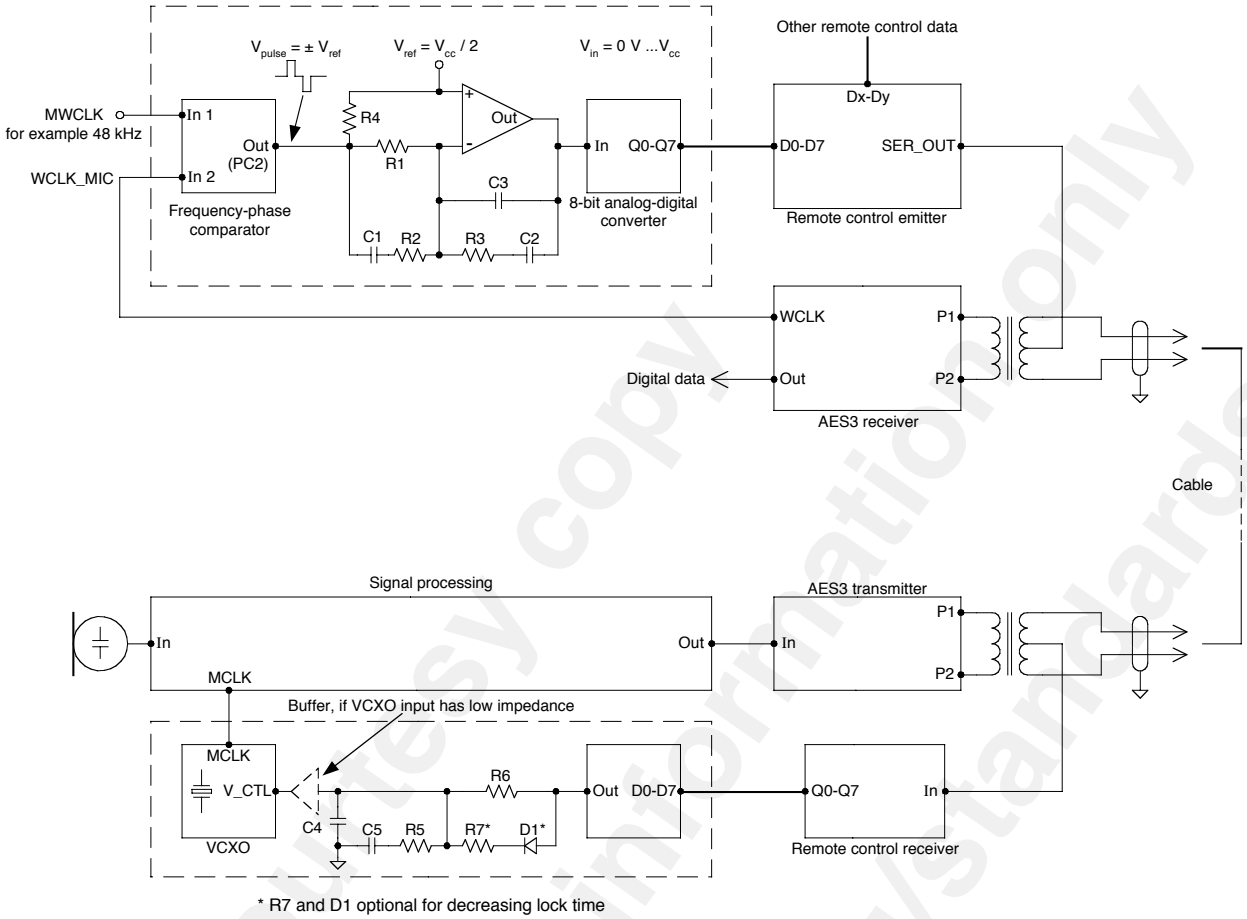


Figure C.1 — Hardware example

Components:

R1, R3	1 MΩ
R2	120 kΩ
R4	10 kΩ
R5	150 kΩ
R6	2,2 MΩ
R7	470 kΩ
C1, C2, C5	1 mF
C3	4,7 nF
C4	0,1 mF
PC2	frequency-phase comparator (for example, 74HC4046)

Annex D

(normative)

Microphone identification and status flag indicators

D.1 Description

A compliant transmitter sends status information using the user data bit defined in AES3. The channel status block start preamble is used to identify blocks of 192 bits of user data. A separate block of user data is assembled for each sub-frame in the AES3 frame, allowing independent settings for the user data associated with each sub-frame. This assembly allows subsequent independent routing of the sub-frame data, while still maintaining the integrity of the user data block.

D.2 Specifications

D.2.1 Monophonic microphones

For a monophonic microphone where the audio data are repeated in both sub-frames, the user data shall be repeated also in each sub-frame.

D.2.2 Identification and status data pages

The microphone status data shall be sent, LSB first, in pages of 192 bits organized as 24 bytes, as shown in tables D.1 to D.26. The user bit format carrying the microphone identification and status flag indicators shall be compatible to the AES3 channel status bit format. The LSB of byte 0 is identified by the channel-status-block start preamble. Byte 0 of each page contains the page identifier bits and certain time-critical status bits, for example, overload. Including the same byte 0 data in all pages results in the time-critical bits always being sent, no matter which page is being sent.

D.2.2.1 The microphone status data in page 0 shall be sent continuously.

D.2.2.2 The microphone shall send any additional pages of status data at least once per second, by default. The console may specify transmission of additional pages by using the page request command.

NOTE 1: In this manner, a continuous stream of microphone status indicator data gets transmitted that can be used to display the status indicators on a user interface or show error messages when any features are addressed which are not implemented in a connected microphone.

NOTE 2: See 0.3 for the status of reserved bits.

D.2.3 Receiver implementations

To ensure correct handling of the user bits by a receiver, the transmitter shall set the encoded user-bits-management field in the AES3 channel status data (byte 1, bits 4 to 7) to 0001. The receiver shall capture the user data bits and interpret them according to the following tables.

Table D.1 — List of status bytes, Page 0

Byte	Function
Byte 0	**Microphone status flags** Page identifier (2), limiter (1), overload (1), mute (1), reserved (3)
Byte 1	**Microphone configuration echo** Attenuation (2), pattern control (4), low-cut filter (2)
Byte 2	**Microphone switch monitoring** Remote off (1), call button (2), reserved (5)
Byte 3	**Microphone remote control feature indicator 1** Attenuation (1), pattern control (1), low-cut filter (1), gain control (1), limiter (1), MS-XY switch (1), balance width (1), equalization (EQ) curve selection (1)
Byte 4	**Microphone remote control feature indicator 2** Mute (1), reset (1), ADC calibrate (1), test signal (1), light control (1), multiple sampling frequencies (1), dither-noise shaping (1), mode-2 synchronization (1)
Byte 5	**Microphone remote control feature indicator 3** Reserved (5), Stereo (1), Compressor/limiter (1), Polarity (1)
Byte 6	**Wireless microphone status flags** Low battery (1), link loss (1), squelch (1), reserved (5)
Byte 7	**Wireless microphone battery status** Battery type (2), battery charge (4), reserved (2)
Byte 8	**Wireless microphone error handling flags** Forward error correction (FEC) capacity (3), error concealment (2), reserved (3)
Byte 9	Supported sampling rate frequencies (8)
Byte 10 to Byte 22	Reserved, all bits 0
Byte 23	Compressor/limiter gain reduction (8)

Table D.2 — List of status bytes, Page 1

Byte	Function
Byte 0	Page identifier (2), limiter (1), overload (1), mute (1), reserved (3)
Byte 1 to Byte 12	Manufacturer identification
Byte 13 to Byte 20	Microphone model identification
Byte 21 to Byte 23	Reserved, all bits 0

Table D.3 — List of status bytes, Page 2

Byte	Function
Byte 0	Page identifier (2), limiter (1), overload (1), mute (1), reserved (3)
Byte 1 to Byte 8	Microphone serial identification
Byte 9	Microphone hardware revision main counter
Byte 10	Microphone hardware revision index counter
Byte 11	Microphone software revision main counter
Byte 12	Microphone software revision index counter
Byte 13 to Byte 15	Delay in samples
Byte 16 to Byte 23	Reserved, all bits 0

Table D.4 — List of status bytes, Page 3

Byte	Function
Byte 0	Page identifier (2), limiter (1), overload (1), mute (1), reserved (3)
Byte 2 to Byte 23	Reserved, all bits 0

Table D.5 — Pages 0, 1, 2, and 3, byte 0 bit allocation: Microphone status flags

Bit	Assignment	Value	Indicates
7 (MSB) 6	**Page identifier**	00 01 10 11	Status bytes, page 0, Mic status Status bytes, page 1, Mic identification Status bytes, page 2, Mic revision Status bytes, page 3, Reserved
5	**Limiter**	0 1	Limiter not active (default) Limiter active
4	**Overload**	0 1	No overload condition (default) Overload condition
3	**Mute**	0 1	Mute not activated (default) Mute activated
2 1 (LSB)	**Reserved**	0	Reserved, bit set to 0

Table D.6 — Page 0, byte 1 bit allocation: Microphone configuration echo

Bit	Assignment	Value	Indicates
7 (MSB) 6	**Attenuation**	00 01 to 11	No attenuation (default) See table A.3
5 4 3 2	**Pattern control**	0000 0001 to 1111	Manufacturer-specific default adjustment (default) see table A.4
1 0 (LSB)	**Low-cut filter**	00 01 to 11	No low-cut filter (default) see table A.5

Table D.7 — Page 0, byte 2 bit allocation: Microphone switch monitoring

Bit	Assignment	Value	Indicates
7 (MSB)	**Remote off**	0 1	Remote parameter setting enabled (default) Remote parameter setting disabled
6 5	**Call button**	00 01 10 11	No button pressed Button 1 pressed Button 2 pressed Buttons 1 and 2 pressed
4 3 2 1 (LSB)	**Reserved**	0	Reserved, bit set to 0

Table D.8 — Page 0, byte 3 bit allocation: Microphone remote-control feature indicator 1

Bit	Assignment	Value	Indicates
7 (MSB)	**Attenuation**	0 1	Attenuation settings not available (default) Attenuation settings available, see table A.3
6	**Pattern control**	0 1	Directivity pattern settings not available (default) Directivity pattern settings available, see table A.4
5	**Low-cut filter**	0 1	Low-cut filter settings not available (default) Low-cut filter settings available, see table A.5
4	**Gain control**	0 1	Signal gain settings not available (default) Signal gain settings available, see table A.6
3	**Limiter**	0 1	Limiter settings not available (default) Limiter settings available, see table A.7
2	**MS-XY switch**	0 1	MS or XY selection not available (default) MS or XY selection available, see table A.19
1	**Balance-width**	0 1	MS width or XY balance not available (default) MS width or XY balance available, see table A.20
0	**EQ curve selection**	0 1	Equalization curve not available (default) Equalization curve available, see table A.21

Table D.9 — Page 0, byte 4 bit allocation: Microphone remote control feature indicator 2

Bit	Assignment	Value	Indicates
7 (MSB)	**Mute**	0 1	Mute selection not available (default) Mute selection available, see table A.8
6	**Reset**	0 1	Reset function not available (default) Reset function available, see table A.13
5	**ADC calibrate**	0 1	ADC calibration function not available (default) ADC calibration function available, see table A.14
4	**Test signal**	0 1	Test signal selection not available (default) Test signal selection available, see table A.15
3	**Light control**	0 1	Light control selection not available (default) Light control selection available, see table A.16
2	**Multiple sampling frequency**	0 1	Sampling frequency selection not available (default) Sampling frequency selection available, see table A.17
1	**Dither-noise shaping**	0 1	Dither and noise shaping not available (default) Dither and noise shaping available, see table A.18
0 (LSB)	**Mode-2 synchronization**	0 1	External synchronization feature not available External synchronization feature available

Table D.10 — Page 0, byte 5 bit allocation: Microphone remote control feature indicator 3

Bit	Assignment	Value	Indicates
7 (MSB) 6 5 4 3	**Reserved**	0	Reserved, bit set to 0
2	**Stereo**	0 1	Mono output signal available Stereo output signal available
1	**Comp./lim.**	0 1	Comp./lim function not available Comp./lim function available
0 (LSB)	**Polarity**	0 1	Polarity selection not available Polarity selection available, see table A.8

Table D.11 — Page 0, byte 6 bit allocation: Wireless microphone status flags

Bit	Assignment	Value	Indicates
7 (MSB)	**Low battery**	0 1	No low battery condition (default) Low battery condition
6	**Link loss**	0 1	RF link is operating (default) RF link is not operating
5	**Squelch**	0 1	Receiver squelch inactive (default) Receiver squelch active
4 3 2 1 0 (LSB)	**Reserved**	0	Reserved, bit set to 0

Wired microphones, which should set the flags to their default zero value, do not use the wireless microphone status flags.

Table D.12 — Page 0, byte 7 bit allocation: Wireless microphone battery status

Bit	Assignment	Value	Indicates
7 (MSB) 6	**Battery type**	00 01 10 11	Not indicated (default) Battery type is primary cell Battery type is rechargeable accumulator Reserved
5 4 3 2	**Battery charge proportion**	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 to 1111	100 % (default) 90 % 80 % 70 % 60 % 50 % 40 % 30 % 20 % 10 % 0 % Reserved
1 0 (LSB)	**Reserved**	0	Reserved, bit set to 0

Microphones supporting low battery indication shall use byte 6, bit 7. Microphones supporting battery charge indication shall support low battery indication in byte 6, bit 7 as well.

Table D.13 — Page 0, byte 8 bit allocation: Wireless microphone error handling flags

Bit	Assignment	Value	Indicates
7 MSB) 6 5	**FEC capacity**	000 001 010 011 100 101 110 111	FEC capacity is used 0 % (default) FEC capacity is used 20 % FEC capacity is used 40 % FEC capacity is used 60 % FEC capacity is used 80 % FEC capacity is used 100 % FEC capacity is overloaded Reserved
4 3	**Error concealment**	00 01 10 11	Error concealment not in use (default) Error concealment in use Reserved Reserved
2 1 0 (LSB)	**Reserved**	0	Reserved, bit set to 0

Table D.14 — Page 0, byte 9 bit allocation: Supported sampling frequencies flags

Bit	Assignment	Value	Indicates
7 (MSB)	Sampling rates (multiple flags are allowed to be set: x = bits don't care for selected flag)	xxxxxxx1	44,1 kHz supported
6		xxxxxx1x	48 kHz supported
5		xxxxx1xx	88,2 kHz supported
4		xxxx1xxx	96 kHz supported
3		xxx1xxxx	176,4 kHz supported
2		xx1xxxxx	192 kHz supported
1		x1xxxxxx	352,8 kHz supported
0 (LSB)		1xxxxxxx	384 kHz supported

Table D.15 — Page 0, bytes 10 to 22 bit allocation

Bit	Assignment	Value	Indicates
7 (MSB)	**Reserved**	0	Reserved, bit set to 0
6			
5			
4			
3			
2			
1			
0 (LSB)			

Table D.16 — Page 0, byte 23 bit allocation, gain reduction

Bit	Assignment	Value	Indicates
7 (MSB)	**Compressor/ limiter gain reduction**	00000000	0,00 dB
		00000001	0,25 dB
6		00000010	0,50 dB
5		00000011	
4		to	increasing 0,25 dB per count
3		11111110	
2			
1		11111111	63,75 dB
0 (LSB)			

Table D.17 — Page 1, bytes 1 to 12 bit allocation: Manufacturer identification

Bit	Assignment	Value	Indicates
7 (MSB)	**Reserved**	0	Reserved, bit set to 0
6	**ASCII MSB**		
5			
4			
3	**ASCII**		7-bit ASCII code of area 00, 20_{16} to $7E_{16}$ Non-printable code in area 01_{16} to $1F_{16}$ is prohibited
2			
1			
0 (LSB)	**ASCII LSB**		

The manufacturer identification character string shall begin in byte 1. Unused bytes shall be filled with zeros.

Table D.18 — Page 1, bytes 13 to 20 bit allocation: Microphone model identification

Bit	Assignment	Value	Indicates
7 (MSB)	**Reserved**	0	Reserved, bit set to 0
6 5 4 3 2 1 0 (LSB)	**ASCII MSB** **ASCII** **ASCII LSB**		7-bit ASCII code of area 00, 20_{16} to $7E_{16}$ Non-printable code in area 01_{16} to $1F_{16}$ is prohibited

The microphone model identification character string shall begin in byte 13. Unused bytes shall be filled with zeros.

Table D.19 — Page 1, bytes 21 to 23: Reserved

Bit	Assignment	Value	Indicates
7 (MSB) 6 5 4 3 2 1 0 (LSB)	**Reserved**	0	Reserved, bit set to 0

Table D.20 — Page 2, bytes 1 to 8: Microphone serial identifier

Bit	Assignment	Value	Indicates
7 (MSB)	**Reserved**	0	Reserved, bit set to 0
6 5 4 3 2 1 0 (LSB)	**ASCII MSB** **ASCII** **ASCII LSB**		7-bit ASCII code of area 00, 20_{16} to $7E_{16}$ Non-printable code in area 01 to $1F_{16}$ is prohibited

The microphone serial identifier character string shall begin in byte 1. Unused bytes shall be filled with zeros.

Table D.21 — Page 2, byte 9: Microphone hardware-revision main counter

Bit	Assignment	Content
7 (MSB) 6 5 4	**(MSB)** **U-nibble** **(LSB)**	Binary-coded decimal number (BCD)
3 2 1 0 (LSB)	**(MSB)** **L-nibble** **(LSB)**	Binary-coded decimal number (BCD)

Both nibbles represent numbers from 00 to 99 in BCD (Binary coded Decimal) encoding. Numbers less than 10 shall be coded with a leading zero.

Table D.22 — Page 2, byte 10: Microphone hardware-revision, index counter

Bit	Assignment	Content

7 (MSB) 6 5 4	**(MSB)** **U-nibble** **(LSB)**	Binary-coded decimal number (BCD)
3 2 1 0 (LSB)	**(MSB)** **L-nibble** **(LSB)**	Binary-coded decimal number (BCD)

Both nibbles represent numbers from 00 to 99 in BCD (Binary coded Decimal) encoding. Numbers less than 10 shall be coded with a leading zero. Bytes 9 and 10 concatenate to form the complete hardware revision number from 00,00 to 99,99. Byte 9 represents the integer part, byte 10 the fractional part.

Table D.23 — Page 2, byte 11: Microphone software-revision, main counter

Bit	Assignment	Content
7 (MSB) 6 5 4	**(MSB)** **U-nibble** **(LSB)**	Binary-coded decimal number (BCD)
3 2 1 0 (LSB)	**(MSB)** **L-nibble** **(LSB)**	Binary-coded decimal number (BCD)

Both nibbles represent numbers from 00 to 99 in BCD (Binary coded Decimal) encoding. Numbers less than 10 shall be coded with a leading zero.

Table D.24 — Page 2, byte 12: Microphone software-revision index counter

Bit	Assignment	Content
7 (MSB) 6 5 4	**(MSB)** **U-nibble** **(LSB)**	Binary-coded decimal number (BCD)
3 2 1 0 (LSB)	**(MSB)** **L-nibble** **(LSB)**	Binary-coded decimal number (BCD)

Both nibbles represent numbers from 00 to 99 in BCD (Binary coded Decimal) encoding. Numbers less than 10 shall be coded with a leading zero. Bytes 11 and 12 concatenate to form the complete hardware revision number from 00,00 to 99,99. Byte 11 represents the integer part, byte 12 the fractional part.

Table D.25 — Page 2, bytes 13 to 15: Delay in samples

Bit	Assignment	Content
7 (MSB) 6 5 4	**(MSB)** **U-nibble** **(LSB)**	Binary-coded decimal number (BCD)
3 2 1 0 (LSB)	**(MSB)** **L-nibble** **(LSB)**	Binary-coded decimal number (BCD)

Both nibbles represent numbers from 00 to 99 in BCD (Binary coded Decimal) encoding. Numbers less than 10 shall be coded with a leading zero. Bytes 13 to 15 concatenate to form the complete hardware revision number from 00,00 to 99,99. Byte 13 represents the LSByte, byte 15 the MSByte.

Table D.26 — Page 2, bytes 16 to 23: Reserved

Bit	Assignment	Value	Indicates
7 (MSB) 6 5 4 3 2 1 0 (LSB)	**Reserved**	0	Reserved, bit set to 0

Annex E

(informative)

XLD connector for digitally interfaced microphone applications

The XLD connector is based on the 3-contact XLR connector described in AES14 with the addition of grooves and user-insertable coding keys.

The chassis-mounting female connector includes a groove added to the inner contact insulator between contacts 2 and 3. In addition, a coding key may be added through the outer housing such that the end of the key protrudes into the space between the outer metal housing and the inner contact insulator. The key shall be positioned between contacts 1 and 2, close to contact 2. See figure E.4.

The male cable connector includes a groove that aligns with the optional coding key in the female connector. In addition, a coding key may be added through the outer shell of the male connector that aligns with the groove in the female connector. See figure E.1.

To be fully coded, a connector shall have both a groove and a coding key. A half-coded connector has a groove only.

When XLD connectors are to mate only with other XLD connectors but never with XLR connectors, then all XLD connectors shall be fully coded.

When complete interoperability of XLD connectors with XLR connectors is required, the coding keys shall not be inserted in either the male or the female XLD connectors.

Figure E.5 shows the mating possibilities allowed by fully coded, half-coded, and non-coded XLD connectors.

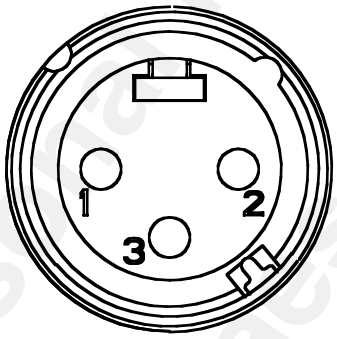


Figure E.1 — Fully coded male cable connector, mates with a fully coded female connector only

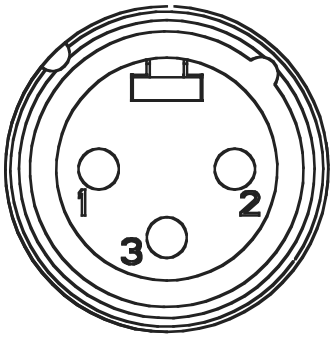


Figure E.2 — Half-coded male cable connector, mates with a standard female chassis connector as well as with a fully coded chassis connector

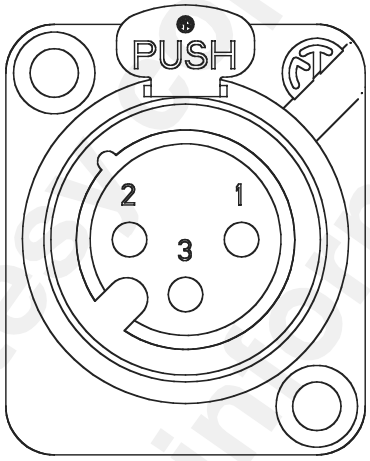


Figure E.3 — Half-coded female chassis connector, mates with all variations of male cable connectors

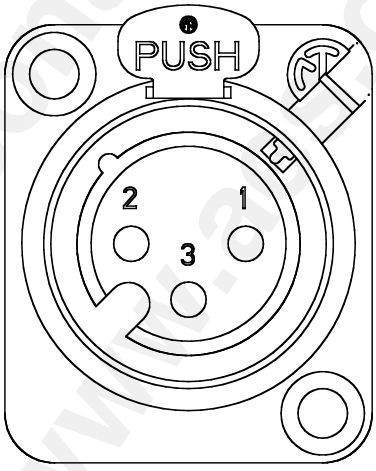


Figure E.4 — Fully coded female chassis connector, mates with a fully coded male cable connector only

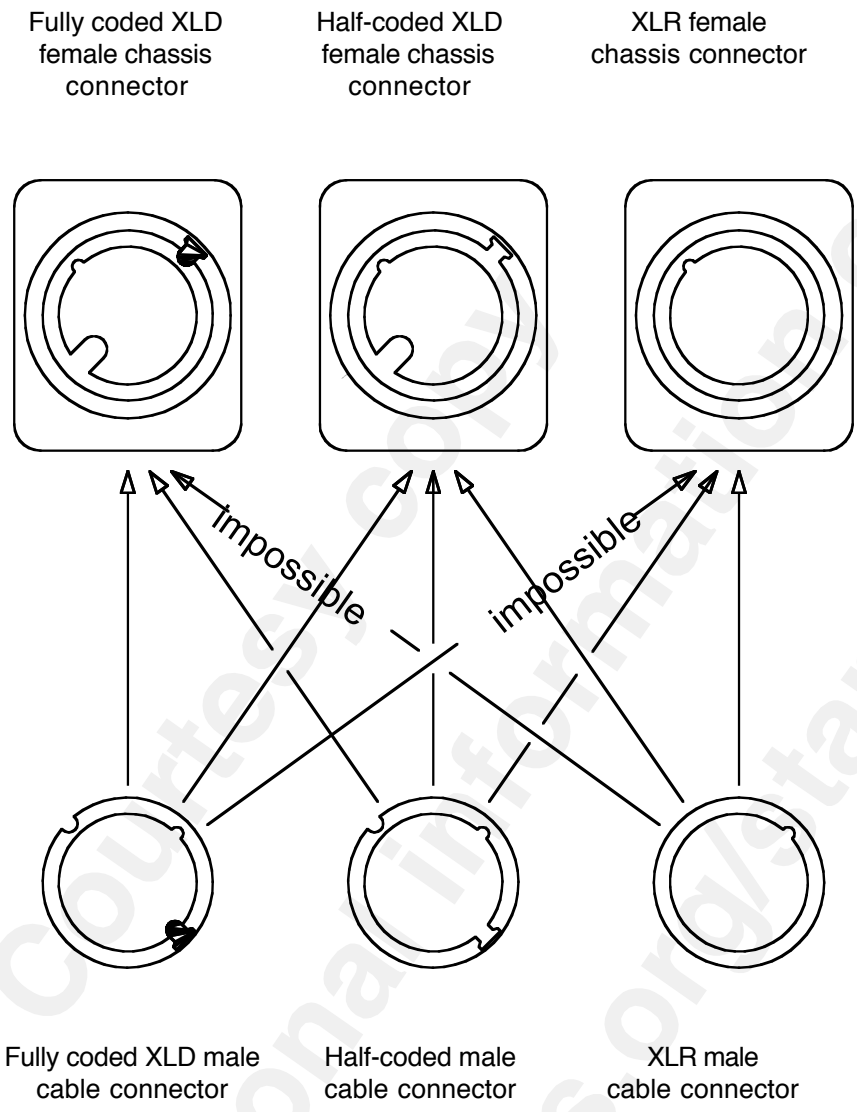


Figure E.5 — Connection logic

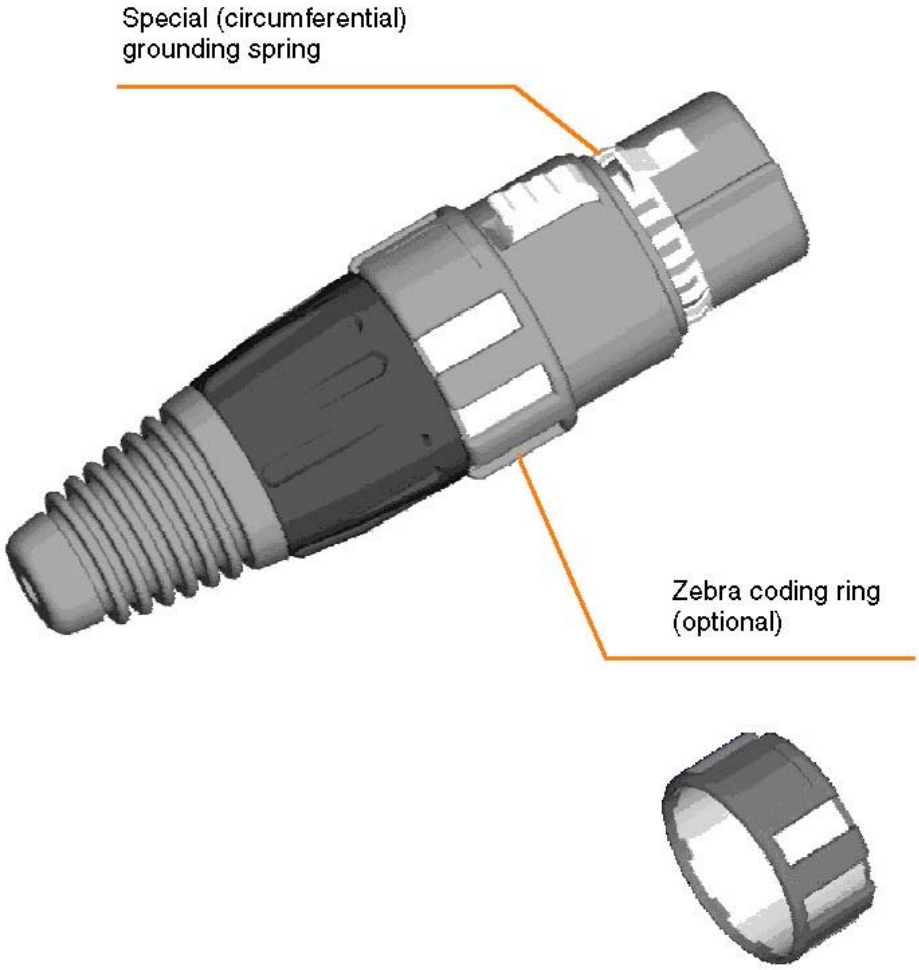


Figure E.6 — Zebra coding ring

Annex F

(normative)

Cable connector

The connector to be used by microphones and interface equipment complying with this standard is under consideration in the AESSC.

NOTE: While this standard requires full compatibility with AES3, equipment complying with this standard may use a connector that will prevent inadvertent connection with incompatible equipment, for example, analog microphone inputs of consoles. If and when a new connector is defined as standard for AES3 interconnections, it shall also be permitted to be used for microphones and interface equipment compliant with this standard under 4.1. When compatibility with other facilities is required, the XLR-3 connector described in AES14 can be used.

If an alternative connector is used, for example, to prevent mating with XLR connectors, that connector shall be the XLD connector described in annex E.

The XLD connector and associated wiring shall include a zebra ring. The color pattern on the ring shall be black-white-black-white for ease of recognition in low light environments. The ring shall have a rough surface (bumps) to facilitate tactile feedback to the user. An example of the zebra ring is shown in annex E.

The presence of the zebra ring on the XLD connector shall indicate that it carries a digital audio signal, that it may be carrying power, and that its associated circuitry cannot be damaged if power is applied in compliance with this standard.

The presence of the zebra ring on the associated cable indicates that the cable is intended for the transmission of digital signals.