

**THE DESIGN OF AN ASIC CONTROL CHIP FOR A
FORWARD ACTIVE CLAMP CONVERTER AND THE
INVESTIGATION OF INTEGRATABLE LATERAL POWER
DEVICES**

by

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(Abstract)

In Part I, the design of an ASIC control chip for a forward active clamp converter is presented. Integration of the control and drive circuit into one IC chip results in higher power density, higher reliability for the converter module. The designed ASIC control chip uses a 2.0 μm N well Analog CMOS process, and is fabricated at MOSIS. The design procedures of the ASIC chip are explained, and experimental results are presented.

Part II of the thesis focuses on the numerical investigation of several integratable lateral power devices. Lateral power devices are used in power IC designs because of their compatibility with analog & digital IC process. To obtain devices with high current density, large safe operating area, fast response and low cost is highly desirable for power ICs. In Part II of this thesis, several lateral power devices are discussed and simulated, including lateral IGBT, lateral MCT and double gate lateral MCTs. It is shown that lateral IGBT and lateral MCTs are good candidates for power IC applications.

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Part I

THE DESIGN OF AN ASIC CONTROL CHIP FOR A FORWARD ACTIVE CLAMP CONVERTER

Chapter 1

Introduction

1.1 Applications of Integrated Circuits in Power Electronics

Microelectronics has made great contributions to the development of electronic systems, especially for signal processing and computing. Today, large percent of circuits in electronic systems are implemented with Integrated Circuits (IC). Microelectronics has also made an impact on power electronics as seen from the various IC products employed in power electronics applications, and this trend is going on. The IC products used in power electronics today can be roughly divided into three categories. First is the discrete power devices. Two types of designs exist for DC converters, linear regulators, and switching converters. While linear regulator has low noise characteristic, its efficiency is relatively low. Switching converters can achieve a high efficiency of over 95%, and is widely adopted for power supply's design. Other switching power circuits include inverters, Power Factor Correction (PFC) circuits. Power switches play a significant role in these switching power circuits, and determine many characteristics of these circuits. Semiconductor power devices are usually used as switches, they evolved from earlier day's thyristors, bipolar device, DMOS to now more commonly used Power MOSFET[1], IGBT, MCT. Today's power devices have low forward voltage drop, fast switching response, high voltage and current ratings. Those features are highly desirable for power circuit's operations. Improvements in these power devices' characteristics make possible of power circuits that switch at high frequency, and operate with high efficiency, high power density. New devices with superior characteristics are still under investigation, and progress in this area will bring corresponding improvement in switching power circuits. The fabrication of devices in this category uses special vertical process, which has a thick epitaxial layer to block voltage. The chip areas of these devices are usually large for high voltage and current ratings.

Another category of ICs used in power electronics includes a wide variety of control and drive circuits, such as PWM control, resonant control chips which implement feedback control for switching power supplies[2]. Motor controls which provide precise speed and torque control in applications including washing machines, disk drives and shavers. Drivers that provide drive current to turn on and off big power devices. These ICs usually employ bipolar or BiCMOS process, because bipolar has a relatively large transconductance. Using BiCMOS process takes advantage of both CMOS's low power dissipation and bipolar's high transconductance.

The third category is usually known as power integrated circuits (PICs). Since recent advance in power devices has led to very much smaller dimensions for integratable power devices and to new gate-controlled device structures requiring very little drive power, these developments make an integrated circuit technology combining power devices and low-voltage control circuits economically viable. This kind of circuits that integrate power device and low-voltage analog and digital circuits on the same chip is referred to as power IC. Examples of such chips include automotive switches, which replace mechanical relays and expensive heavy wiring harnesses, high voltage driver for plasma display panels, power amplifiers. A special kind of PIC is known as high-voltage Integrated Circuits (HVIC) , which provides high-voltage interfacing at relatively low currents, generally between logic circuits and very high-power circuits [3] [4]. With the popularity of portable and personal communication systems, high quality power supplies for these systems are under development, and an approach using IC technology seems most likely for these highly

compact systems. People are trying to integrate battery charger with microprocessor and RAM to realize intelligent battery charging. Another interesting application is integrated DC-DC converter that converts battery voltage to the specific voltage the system needs. As now in these systems, power supplies still occupy a significant portion of space and weight. National Semiconductor has introduced one chip converter, which uses special packaging technique to include the inductor and capacitor along with the control. In the future, there may be more fully integrated DC converters designed specifically for these applications. The process used for PICs is special process which can implement both low voltage and power devices. Power devices in PICs usually take a lateral form, which is more compatible with low-voltage devices. Power dissipation of PICs are limited by the power that the chip, along with bonding and package can handle, and also isolation must be maintained between the power device and logic circuits. Usually they are not designed to handle big power, but to accomplish useful functions.

As technology advances, products from these categories are merging with each other. For example, there are power devices called “smart devices” [5], which integrate protection such as thermal shutdown, over current, over voltage protection, or drivers along with discrete power devices. As the trend goes towards more integration, in IC design, there is “system on chip”, power electronics is also engaged in more integration to achieve high power density, small volume and more flexibility. The research carried on now in VPEC on PEBB concept, and production of high efficient modules shows the leading technologies in this area. IC can be an aid in this effort, and using ICs effectively can help to meet the goals.

1.2 Motivation and Objective

In this thesis, design of an Application Specific Integrated Circuit (ASIC) control chip for a forward active clamp converter is presented. The forward converter module converts 48V input to 3.3V output, which is now the new standard supply voltage for digital circuits. The forward converter has an efficiency target of over 90% and power density target of $100W/in^3$. Such high power density is hard to achieve if all control are implemented with discrete components and IC

chips, therefore it seems desirable to integrate the control function into one chip. The integration of the control part offers several advantages, including enhanced performance, increased reliability and reduced parasitic inductance and capacitance. Since power circuits usually have a fast voltage and current switching transient, wiring inductance and stray capacitance in discrete circuits will cause significant switching noise, hence requiring special care in PCB layout design. In an integrated circuit, interconnecting leads are much shorter so that the inductive voltage spikes are significantly reduced. Capacitive coupling is also reduced since parasitic capacitance is much lower. Integration of control will reduce the volume of the overall converter circuit, since one chip is used instead of several discrete circuits. This improves the power density accordingly. Using one chip for control also provides a simpler interface to users, because only one chip is dealt with instead of several. All of these will contribute to a power converter circuit with higher quality.

The cost of an integrated method over a discrete implementation depends on the overall system economics, where benefit is derived from a lower package count, smaller printed circuit board, less weight, etc. On the other side, if complex process is required for IC design, the cost will rise. The unit price of ICs will depend largely on the production volume. Applications in power electronics are diverse in nature, and may require different designs for different applications, each has a relatively small volume. These difficulties can be addressed by offering more control capability and flexibility in the design, and a fast turn-around design cycle resulting from advanced design methodology, such as the use of standard cells.

CMOS process is therefore chosen for this design. CMOS has the advantages of low cost, low static power dissipation, high noise margin. It is the most widely used process for low-voltage integrated circuits applications. Traditional drive and control circuits for power electronics usually use bipolar process due to the higher current driving capability of bipolar transistor and excellent linearity of BJTs. The use of CMOS compatible process for these purposes are however becoming more and more attractive, due to its wide applications in VLSI design. Using CMOS process can reduce the cost and static power dissipation, and the circuits can be integrated with other CMOS logic circuits to form a complex system at a lower cost. CMOS process is also accessible to us through MOS Implementation Service (MOSIS) fabrication facility. MOSIS is a fabrication service operated by the Information Sciences Institute of the University of Southern California. It provides a good experimental environment for academic research. The ASIC chip for the forward active clamp converter is implemented using a 2.0 μm N-well CMOS process. ASIC design is a widely used concept in IC design, in order to optimize the system performance towards the target application, it requires a fully custom design procedures as against a standardized design. From the design of the ASIC control chip, the possibilities of using CMOS process for power electronics applications is also investigated.

Forward active clamp converter uses a clamp capacitor and a high side switch to reset the transformer. Pulse Width Modulation (PWM) logic is used for the control, two complementary control signals with a designed delay time between the turn-off of one switch and the turn-on of the other switch are required. Nowadays, PWM control is typically implemented with IC chips, there are series of PWM control chips from Unitrode, Texas Instrument, such as UC3825[2]. These chips typically output a single phase control signal or two-out-of phase control signals. At the time this work began, there is no commercially available IC chips for active clamp circuits control. During the course of this work, Unitrode introduced a new chip for single ended active clamp reset PWM, UCC3580[6]. One feature of the chip is programmable delay between two switches' transition, but the delays at the rising edge and falling edge are the same. The maximum duty cycle is 60%, and the output driver can sink 1A, source 0.5A for the main switch and sink 0.3A and source 0.3A for the auxiliary switch.

In Chapter 2, first the PWM control of the forward active clamp converter is discussed, followed by the circuit design of the control functions. Chapter 3 describes the VLSI realization procedure for the PWM control chip, and experimental results are presented. Chapter 2

Chapter 2

Design of ASIC PWM Control Chip

2.1 Introduction of PWM Control and Forward Active Clamp Converter

DC-DC converter converts one DC voltage to another, the average dc output voltage of a DC-DC converter is controlled by the switch's 'on' and 'off' duration (ton and toff). Pulse Width Modulation (PWM) control is widely used for switching converter's feedback control. In PWM switching, the switching frequency is constant, the switch duty ratio D , which is defined as the ratio of the 'on' duration to the switching period is varied. The switch control signal is generated by comparing a signal-level control voltage $V_{control}$ with a repetitive waveform (e.g. a sawtooth) as shown in Figure. 2-1(a) and 2-1(b). The control voltage signal is usually obtained by amplifying the difference between the actual output voltage and its desired value. The frequency of the repetitive waveform with a constant peak, establishes the switching frequency, usually from a few kilohertz to a few hundred kilohertz. When the amplified differential signal, which varies very slowly with time relative to the switching frequency, is greater than the sawtooth, the switch control signal becomes high, causing the switch to turn on. Otherwise, the switch is off. The switch duty ratio can be expressed as

$$D = \frac{t_{on}}{T_s} = \frac{V_{control}}{V_{st}},$$

where V_{st} is the peak of the sawtooth.

Key waveforms of the converter's operation, and equivalent circuits for different operating stages of the converter in one switching cycle are shown in Figure 2.3 and Figure 2.4. The circuit's operation can be explained as four modes.

Mode 1: Main Switch conduction ($T_0 - T_1$)

In this mode, the main switch (Q1) of the converter is on. The clamp capacitor (charged to V_c) is disconnected from the rest of the circuit by virtue of the clamp switch (and diode) being off. The input voltage is applied across the primary winding. the output rectifier is on and power transfer is taking place. At the same time, magnetizing current is linearly increasing. At the end of this period, Q1 is turned off.

Mode 2: Transition to Clamp Circuit ($T_1 - T_3$)

This transition involves charging of C_a to a voltage equal to $V_i + V_c$. Once the voltage reaches this level, diode D2 turns on and clamping action takes place. If switch Q2 is turned on prior to D2 turn-on, it is a non-ZVS transition, it is fairly easy to achieve ZVS for this transition. Part of the charging is linear with reflected load current charging the capacitor. The leakage energy (first) and magnetizing energy (next) are then utilized to complete the charging.

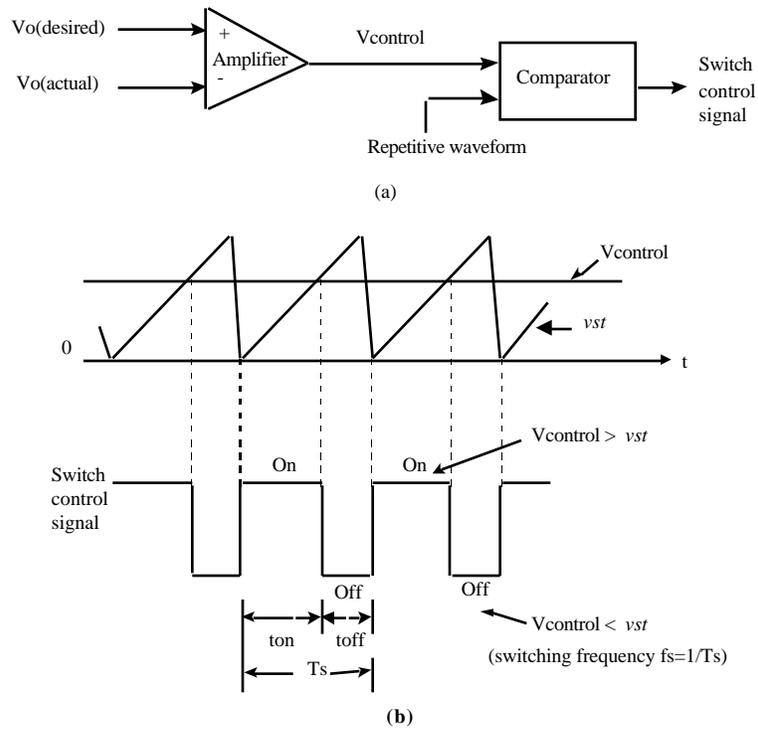


Figure 2.1 Pulse-width modulator: (a) block diagram; (b) comparator signals.

Figure 2.2 shows the circuit diagram of a forward active clamp converter that uses PWM control.

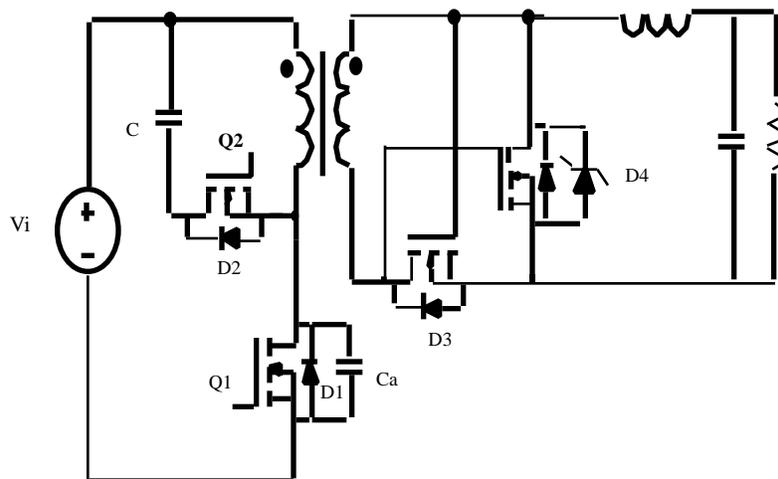


Figure 2.2 Forward active clamp converter

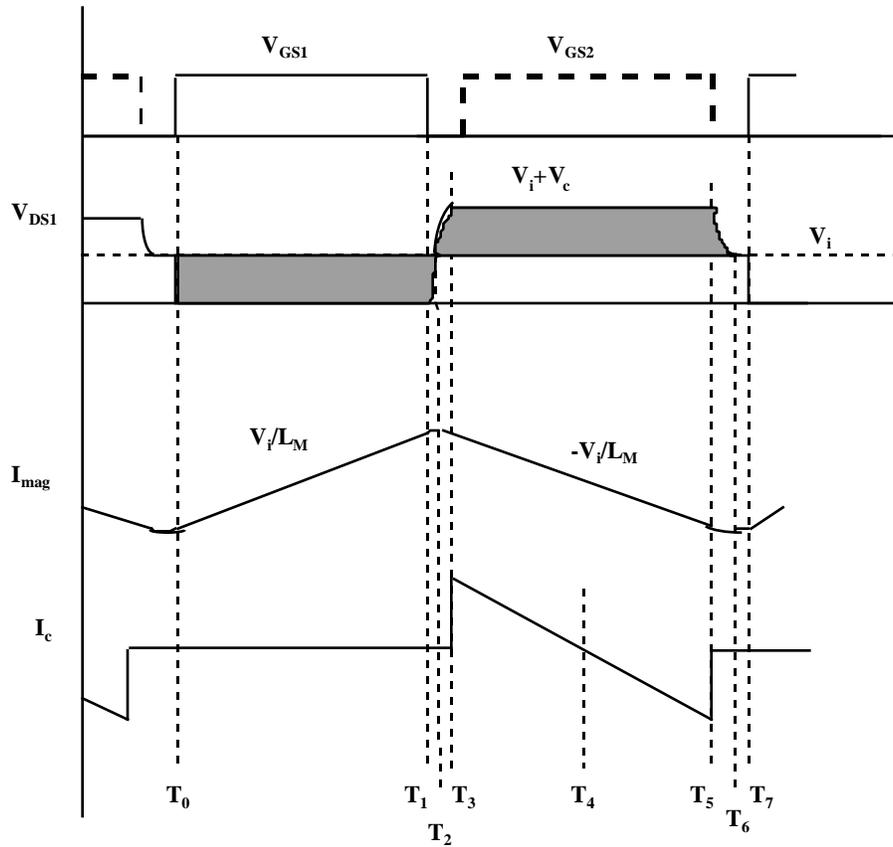


Figure 2.3 Operation waveforms of forward active clamp converter

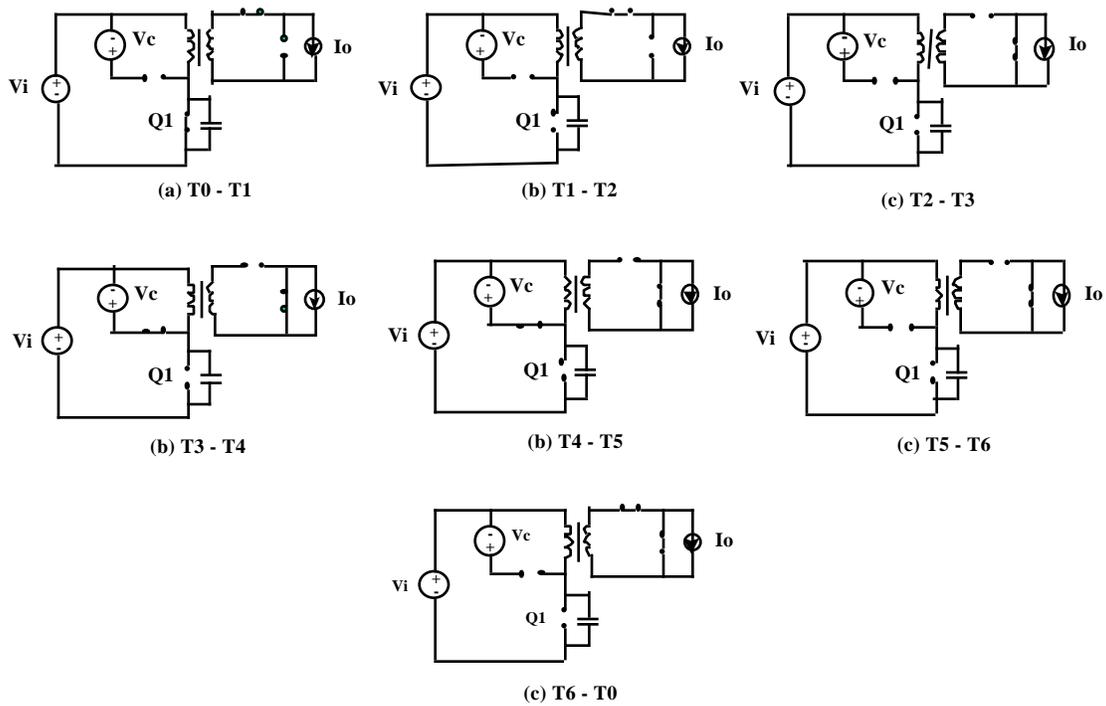


Figure 2.4 Equivalent circuits for different operating stages

Mode 3: Clamp Circuits Operation ($T_3 - T_5$)

The clamp circuit (D2/Q2/C) provides a low impedance path for most of the leakage inductance energy without allowing excessive ringing or power dissipation. During D2 conduction, the clamp capacitor is charged while providing negative voltage across the primary winding. Turning Q2 on allows C to discharge and energy to be stored back in the leakage and /or magnetizing inductance. The output is disconnected from primary ($i_p=0$) during this mode.

Mode 4: Main Switch Transition ($T_5 - T_0$)

This mode begins when Q2 is turned off. During this mode, Ca has to be discharged completely for zero voltage (lossless) turn-on of Q1. During the clamp mode, energy is stored in the leakage and magnetizing inductance (in reverse current polarities) to enable them to discharge the capacitance C_a . Magnetizing energy is used to reduce V_{CA} to zero voltage. There are two avenues available to the designer. One involves reducing the magnetizing inductance allowing higher negative current and stored energy. Second option is to increase the leakage inductance by adding external series inductance. For an ideal transformer, forward converter does not quite yield true zero-voltage switching - once the capacitor discharges below V_{in} , the output diode D3 turns on and diverts the magnetizing energy to the output. However, due to secondary side leakage inductance, this turn-on may be slower and sufficient to discharge the capacitor C_a . Additional primary series inductance helps in this case. However, this series inductance creates an imbalance in transformer operation, and this can lead to reverse core saturation during load transients, hence primary series inductance should be minimized in active clamp converters.

It is clear that the voltage transitions during modes 2 and 4 depend on circuits parameters and operating conditions. Any control and drive circuit for the active clamp converter has to allow programmable time delays between the turn-off of one switch and the turn-on of the other switch in order to accommodate these transitions and to achieve zero voltage turn-on conditions.

This active-clamp forward converter topology has many advantages over conventional forward converter [7,8]. The voltage stress of the main switch is relatively low in spite of input voltage variations since the increased transformer reset time would allow a lowering of reset voltage as the input voltage rises. Therefore there is no need for additional gate protection circuits if transformer turns ratio is selected properly. The transformer's leakage inductance is absorbed in C and the voltage surge is clamped. Zero-voltage transitions and non-dissipative return path is achieved for leakage inductance energy. Active clamp converters can operate at duty cycles much higher than 50% maximum level used for many traditional single-ended converters. As a result, higher primary to secondary turns ratio can be used leading to smaller size of output inductor, low current stresses on primary and low voltage stresses on secondary side. Alternatively, the input voltage range for the converter can be extended for the same primary to secondary turns ratio. Synchronous rectifiers are used in the converter to enhance the efficiency at low output voltages.

Therefore the PWM control chip under design is to provide the feedback control for the converter as shown in Figure 2.5.

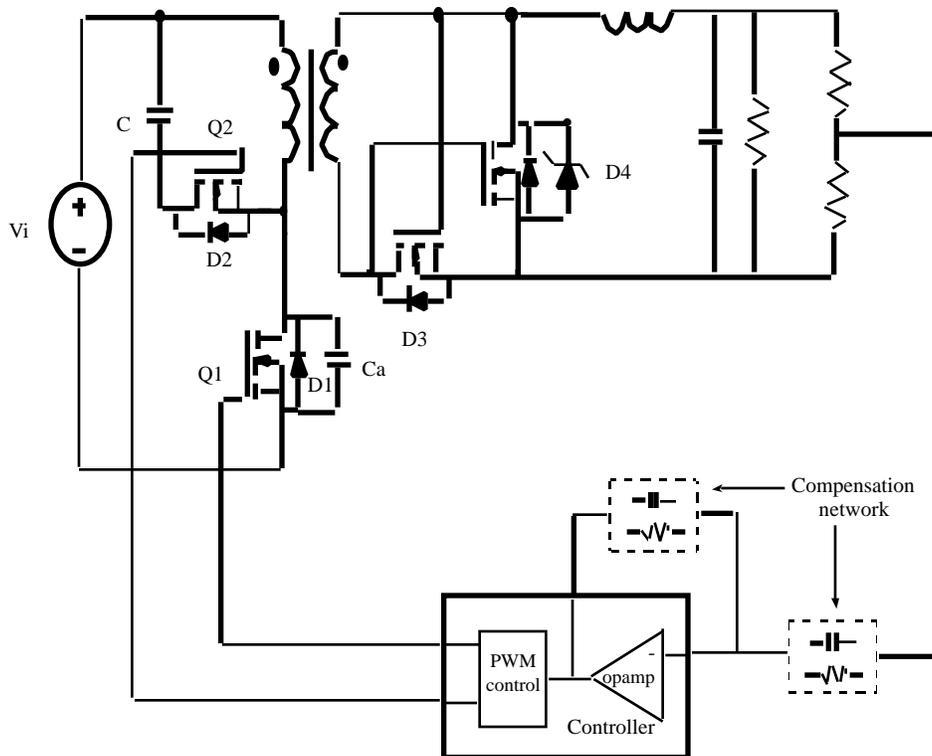


Figure 2.5 Forward active clamp converter and the PWM control chip

2.2 System Design of the Control Chip

Two control signals for the two switches are needed for the converter's operation. The converter's input voltage is 48 V, output voltage is 3.3 V, and the output power is 100 W. The delay time requirement between the two switches is shown in Figure 2.6 with 270 ns t_{d1} 300 ns, t_{d2} 170 ns. The delay time between the switches' transitions ensures that two switches don't conduct at the same time, and helps to achieve zero voltage transitions for the switches. Switches used in the converter are power MOSFETs from International Rectifier, the low side switch is IRFP250, high side switch is IRF640. Switching frequency is around 500 kHz.

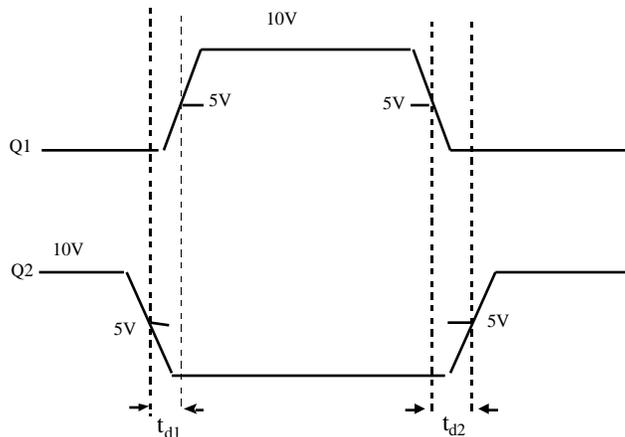


Figure 2.6 Delay time requirement for the two switches

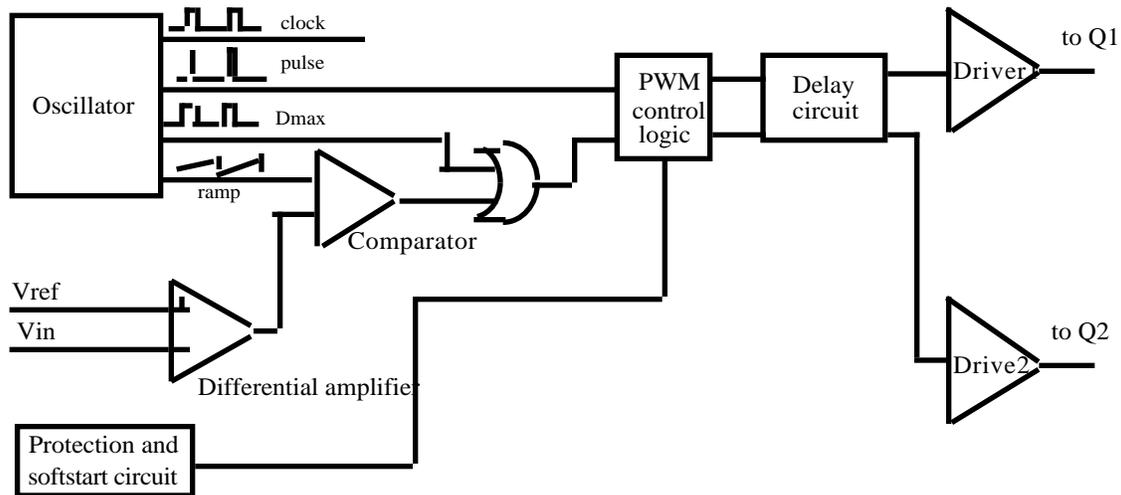


Figure 2.7 Block diagram of the control chip

The functional circuit diagram of the control chip is shown in Figure 2.7. The oscillator section generates four signals, a clock signal which sets the switching frequency, a pulse signal, a ramp signal and a maximum duty ratio signal, all of which are used in PWM control logic. PWM logic section realizes PWM control by setting up the duty ratio of the main switch at the beginning of each switching cycle with the pulse signal. Then the amplified differential signal is compared with the ramp signal and a duty ratio is derived. This duty ratio is input to an OR gate with the maximum duty ratio signal, the output of the OR gate decides the actual duty ratio of the main switch, which cannot exceed the maximum duty ratio. Two complementary duty ratio signals from the PWM logic section are sent to the delay section. The delay section delays the rising edge of each of the two duty ratio signals for the amount of time specified, but doesn't affect the falling edge of each of these signals. The delayed duty ratio signals then go to the driver section to provide enough current capability to drive the power switches. An OPERational AMPLifier (Opamp) is used to generate the differential signal and performs compensation in closed loop. Reference voltage to the Opamp's input is generated on chip by voltage reference circuit. Protection function can be realized with voltage or temperature sensing, and when error occurs, shutdown the control chip by setting a shutdown terminal to zero. The shutdown terminal is normally high, and has no effect on PWM logic. When shutdown is low, the duty ratio output is disabled. The soft-start circuit performs the soft start function at power up.

2.3 Design of The Control Chip Building Blocks

2.3.1 Oscillator Section

A. Initial Design

The oscillator section generates a clock signal which sets the switching frequency, and three other signals, pulse, ramp and maximum duty ratio, all of which are based on the clock signal.

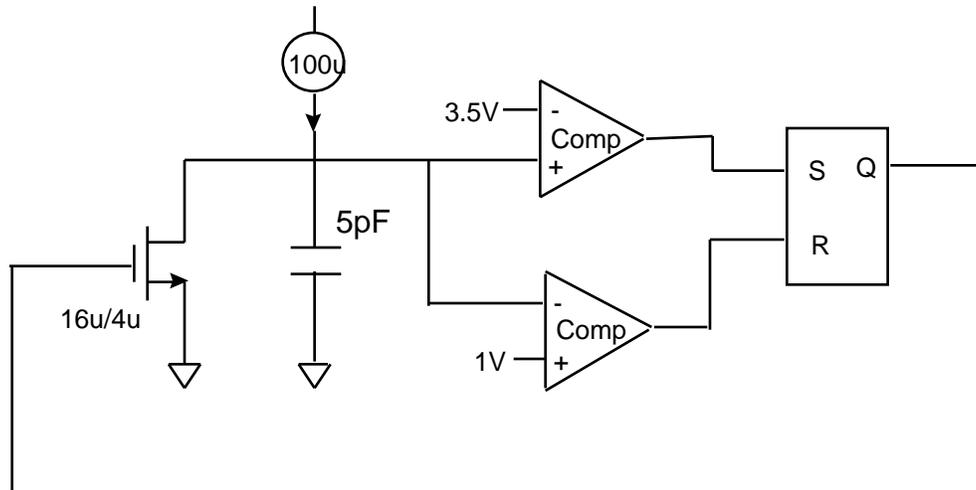


Figure 2.8 Block diagram of the clock generator

To generate the clock signal, a scheme such as that shown in Figure 2.8 is first considered. It uses a constant current to charge a capacitor, two comparators are used to compare the voltage across the capacitor with two reference voltages, and the reference voltages are set to 3.5 V and 1 V. A MOSFET is connected across the capacitor, and is turned on intermittently to discharge the capacitor when the capacitor's voltage exceeds 3.5 V, and is turned off when capacitor's voltage is less than 1 V. Charging up of the capacitor is linear with time, and discharging of the capacitor is fast compared to one clock period. The voltage across the capacitor is therefore the ramp signal with 2.5 V peak to peak amplitude to ensure good noise margin for the PWM control. The output of the flip-flop is the clock signal.

Discharging time of the capacitor should be small enough so that a maximum duty ratio can be reached. The maximum duty ratio is usually 80%-100%, and 80% is chosen in this design. The discharging time should be less than 20% of one clock cycle. Simulation waveforms using Cadence's Spectra is shown in Figure 2.9. The top waveform is the ramp signal and the bottom waveform is the output of the RS flip-flop. Clock period is 1.7 μ s, discharging time is about 6% of one clock cycle.

The high and low level of the ramp signal is slightly higher than 3.5 V and lower than 1 V, at about 3.54 V and 0 V respectively. This is caused by the loop delay which includes the delay of the comparators, RS flip-flop, and the discharging MOSFET. The capacitor is implemented with two polysilicon layers, which has an unit capacitance of 0.43 fF/ μ m².

The current source in the oscillator uses a Wilson current mirror as shown in Figure 2.10. Wilson current mirror has high output impedance and good current matching, but the output's highest voltage is limited by $V_{dd} - 2V_{ds}$, where V_{ds} is the saturation voltage of the PMOS. Design must ensure that the highest output voltage is greater than the upper bound of the ramp signal which is 3.6 V. Hence a maximum output voltage of 4 V was designed. Reference current is set by a resistor implemented using the N-well layer which has a sheet resistance of 4.6 k Ω / \square . The resistor value can be calculated in first order from the equations:

$$RI_{REF} + 2V_{gs} = V_{dd}, \text{ and}$$

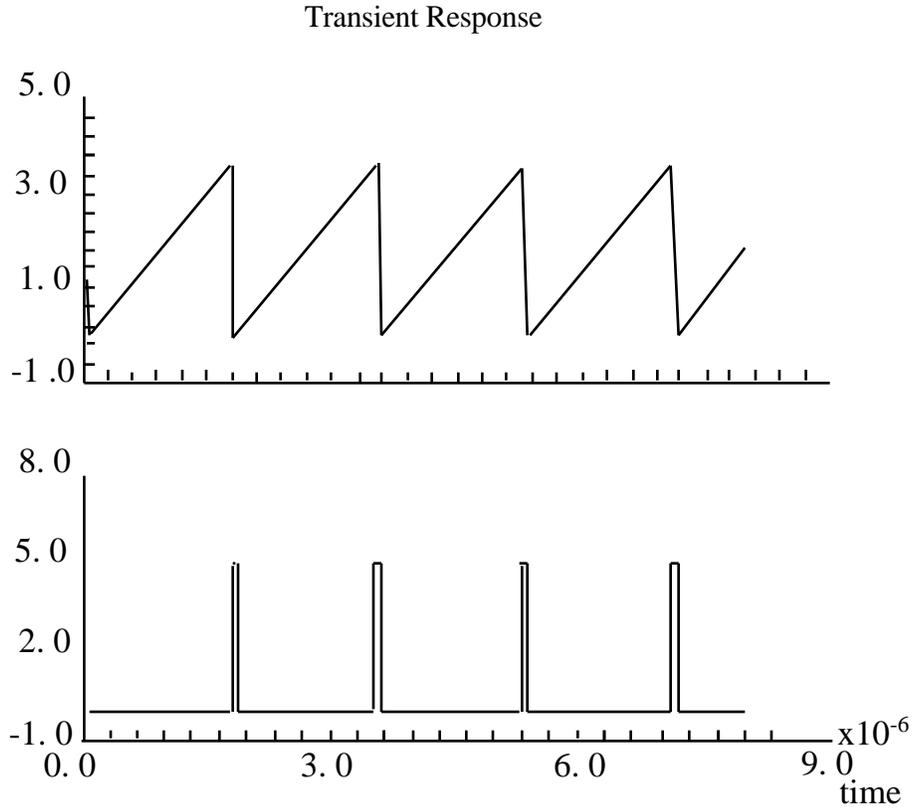


Figure 2.9 Simulation result of the clock generator

$$\frac{pW}{2L} (V_{gs} - V_{th})^2 = I_{REF}$$

After simulation, a value of 160 k is chosen. Layout implementation of the resistor uses a winding structure to save area. The layout of the current source is shown in Figure 2.11.

Schematic diagram of the RS flip-flop is shown in Figure 2.12, two inverters and two NAND gates are used instead of two NOR gates, since NAND gate has faster response. The transistors use minimum size which is typical for digital circuits. Layout of the RS flip-flop is shown in Figure 2.13.

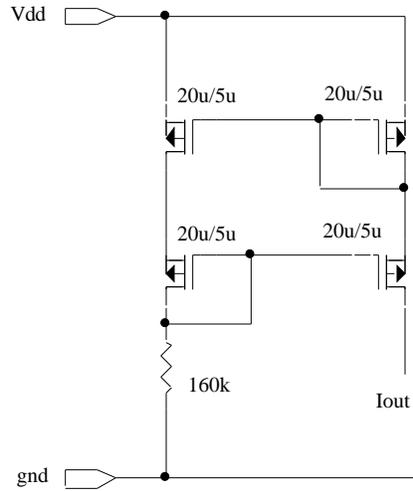


Figure 2.10 Schematic diagram of the current source

Figure 2.11 Layout of the current source(tif, 14k,curr.tif)

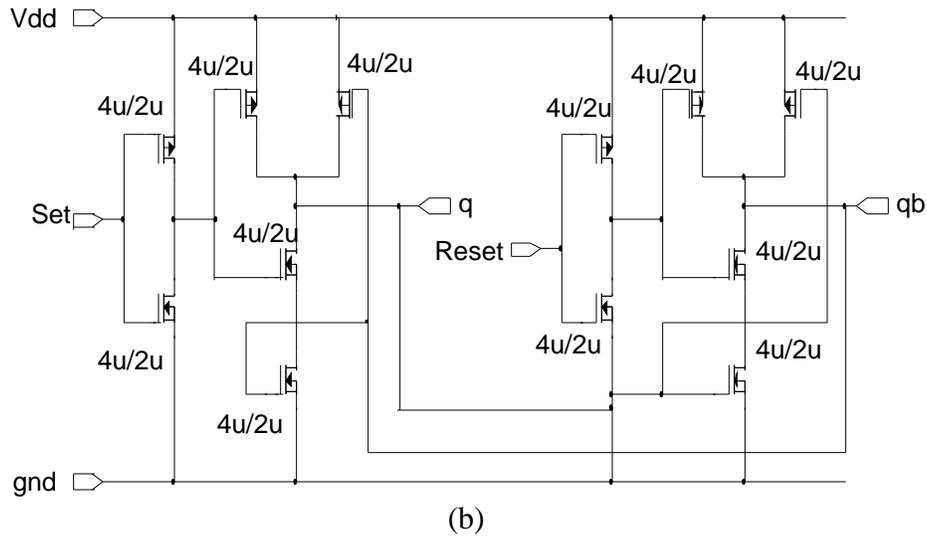
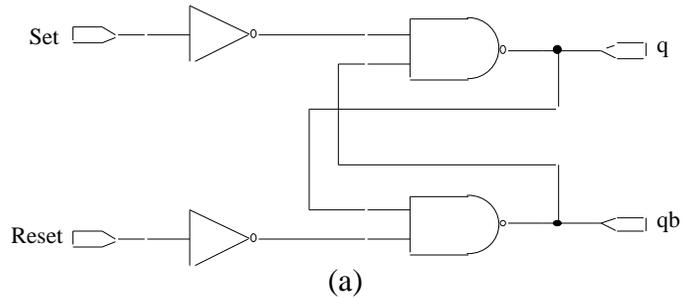


Figure 2.12 Schematic diagram of the RS flip-flop (a) gate level (b) transistor level

The comparator is shown in Figure 2.14, it has a DC gain of 51 dB and an unit gain bandwidth of 210 MHz. The -3dB point is at 1.9 MHz. Layout of the comparator is shown in Figure 2.15. Layout of the clock generator is shown in Figure 2.16.

Figure 2.13 Layout of the RS flip-flop(tif,31K, flipflop.tif)

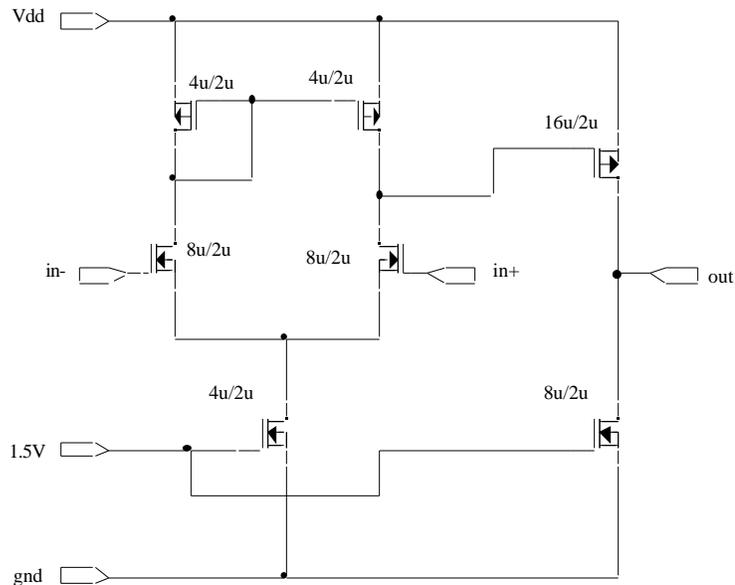


Figure 2.14 Schematic diagram of the comparator

Figure 2.15 Layout of the comparator(tif,39K,comp_o.tif)

Figure 2.16 Layout of the clock generator(tif,56K,clock_o.tif)

B. Final Design

The highest oscillating frequency of the above scheme is limited by the total loop delay, and because of the large delay of the comparators, the oscillating frequency usually can't be higher than several hundred kilohertz, another drawback is that the N-well resistor has a large process variation of 15%, and occupies large area, so eventually the design was changed to circuit shown in Figure 2.17, in which comparators are substituted by a simple schmitt trigger. An external resistor is used to set the reference current. The loop delay is decreased to the sum of several gate delays, higher clock frequency can therefore be reached, and the frequency is adjustable by choosing different resistors.

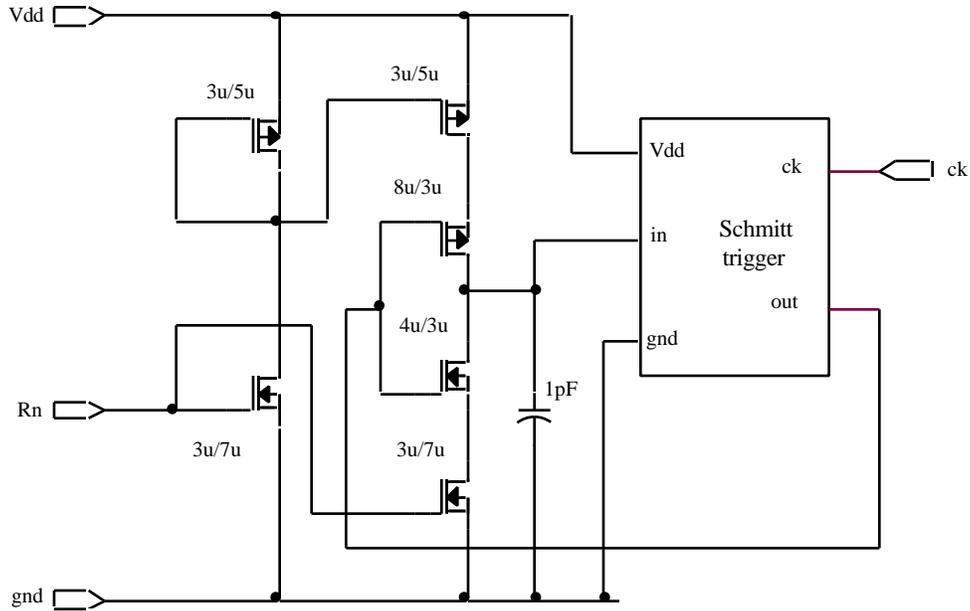


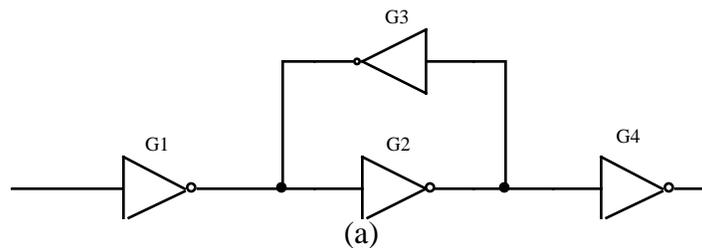
Figure 2.17 Schematic diagram of clock generator with schmitt trigger

Schematic diagram of the schmitt trigger is shown in Figure 2.18, it is a bistable circuit that uses a positive feedback. Gate G1 should have much larger drive capability than gate G3, so the output state is determined by input of G1 no matter what the previous output was. DC transfer curve of the schmitt trigger from simulation is shown in Figure 2.19. The thresholds of schmitt trigger are designed to be 1.5 V and 3 V respectively.

The charging and discharging current of the clock generator is $1.5 \mu\text{A}$, C_p is 1 pF ,

the clock period is $T = \frac{C(V_+ - V_-)}{I_{ch}} + \frac{C(V_+ - V_-)}{I_{dis}} = 2\mu\text{s}$, $f = 500 \text{ kHz}$. Simulation result of

the clock generator is shown in Figure 2.20. It is clear that the simulation result is close to the calculation. Layout of the clock generator is shown in Figure 2.21.



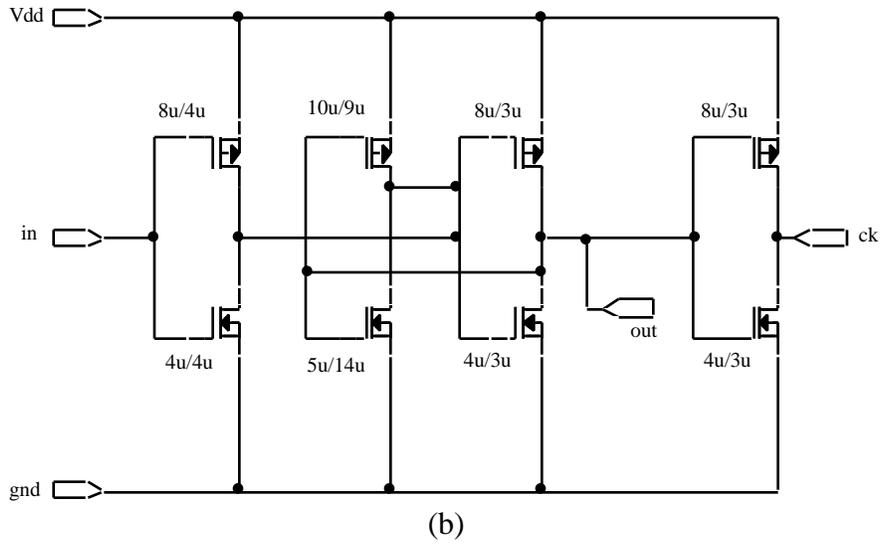


Figure 2.18 Schematic diagram of the schmitt trigger (a) gate level (b) transistor level

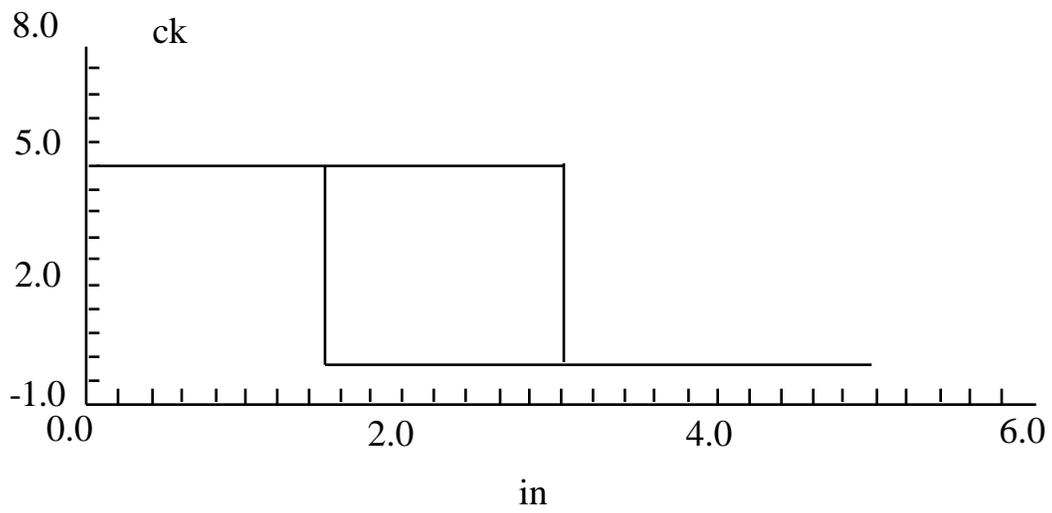


Figure 2.19 DC transfer curve of the schmitt trigger

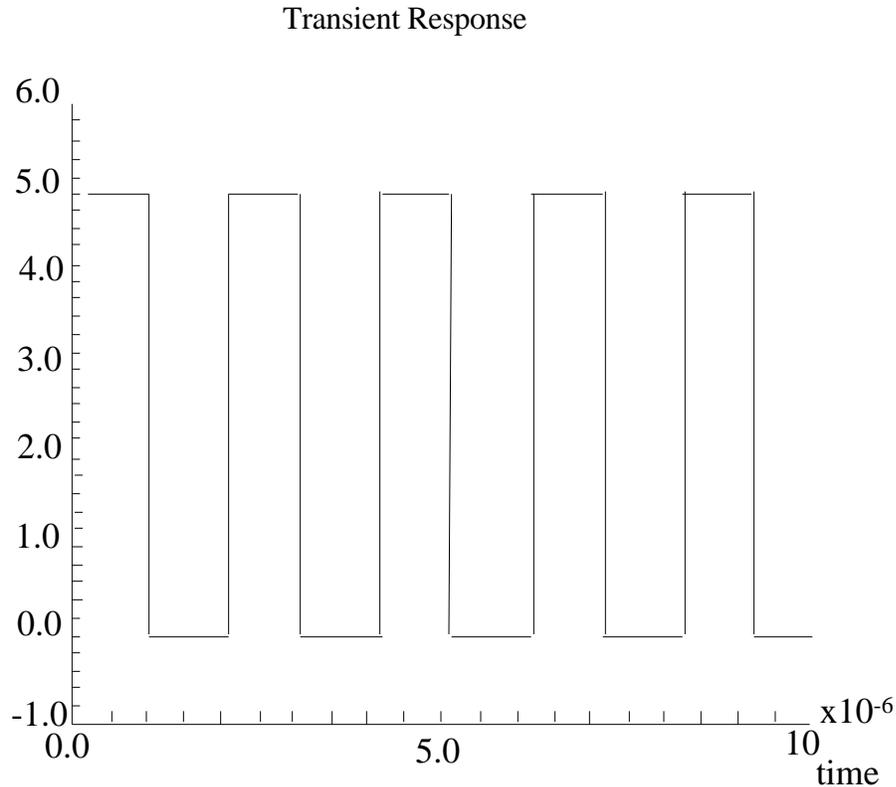


Figure 2.20 Simulation result of the clock generator with schmitt trigger

Figure 2.21 Layout of the clock generator with schmitt trigger(tif,33K,clock.tif)

Pulse generator generates short pulses to set up the duty ratio at the start of each switching cycle, the pulse should be long enough to be able to set the RS flip-flop, but should be as short as possible, since after setting of the flip flop, it must allow the control signal to reset the flip flop if small duty ratio is needed. If minimum duty ratio is specified, this can be realized by set the pulse width to the minimum on time. Schematic diagram of the pulse generator is shown in Figure 2.22. The pulse width is equal to five gate delays. The “fast” input to the NAND is tied to the NAND gate input that has the least coupling capacitance to the output node, this minimizes the charge injection. Transistor M1 is used to cancel the charge injected by the fast input. Simulation result of the pulse generator is shown in Figure 2.23, the pulse width obtained is 40 ns which sets a minimum duty ratio of $40/2000 = 2\%$. Layout of the pulse generator is shown in Figure 2.24.

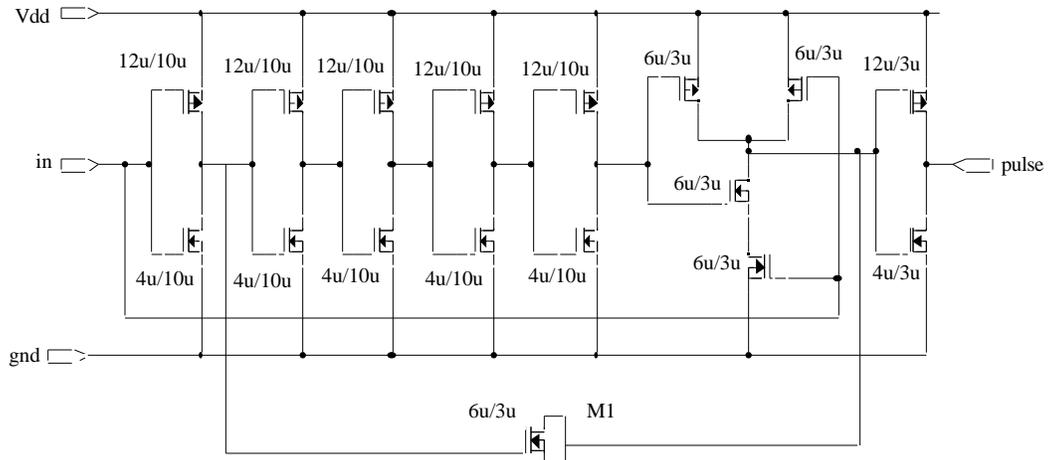


Figure 2.22 Schematic diagram of the pulse generator

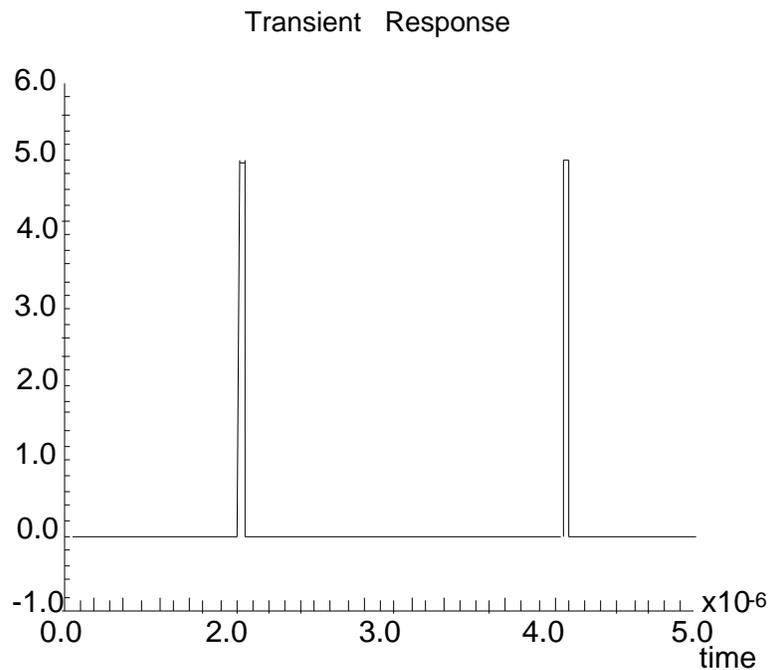


Figure 2.23 Simulation result of the pulse generator

Figure 2.24 Layout of the pulse generator(tif,35K,pulse.tif)

Ramp signal is generated by charging a capacitor with a current source as shown in Figure 2.25, followed by a level shifter which shifts the input signal from 0~2.6 V to 1~3.6 V. Simulation result is shown in Figure 2.26 and designed layout is shown in Figure 2.27.

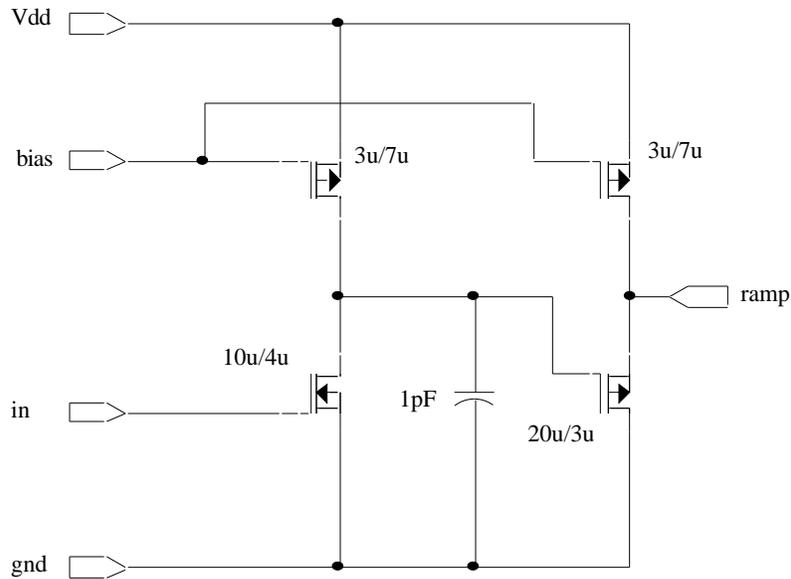


Figure 2.25 Schematic diagram of the ramp generator

Transient Response

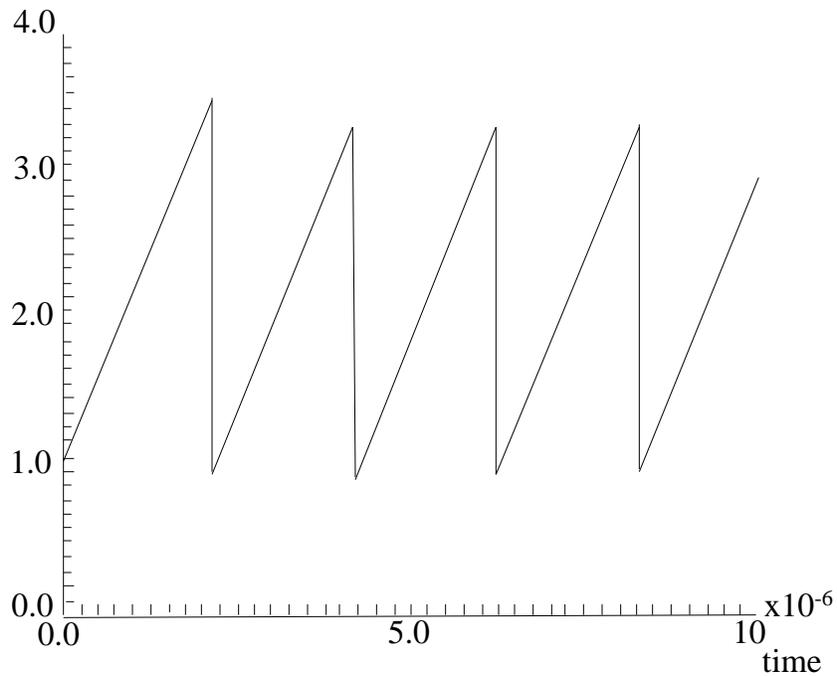
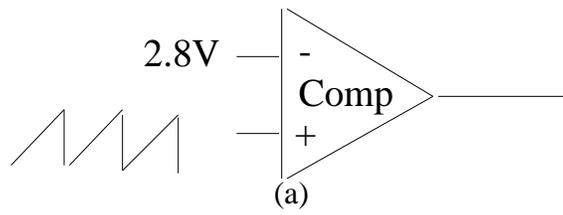


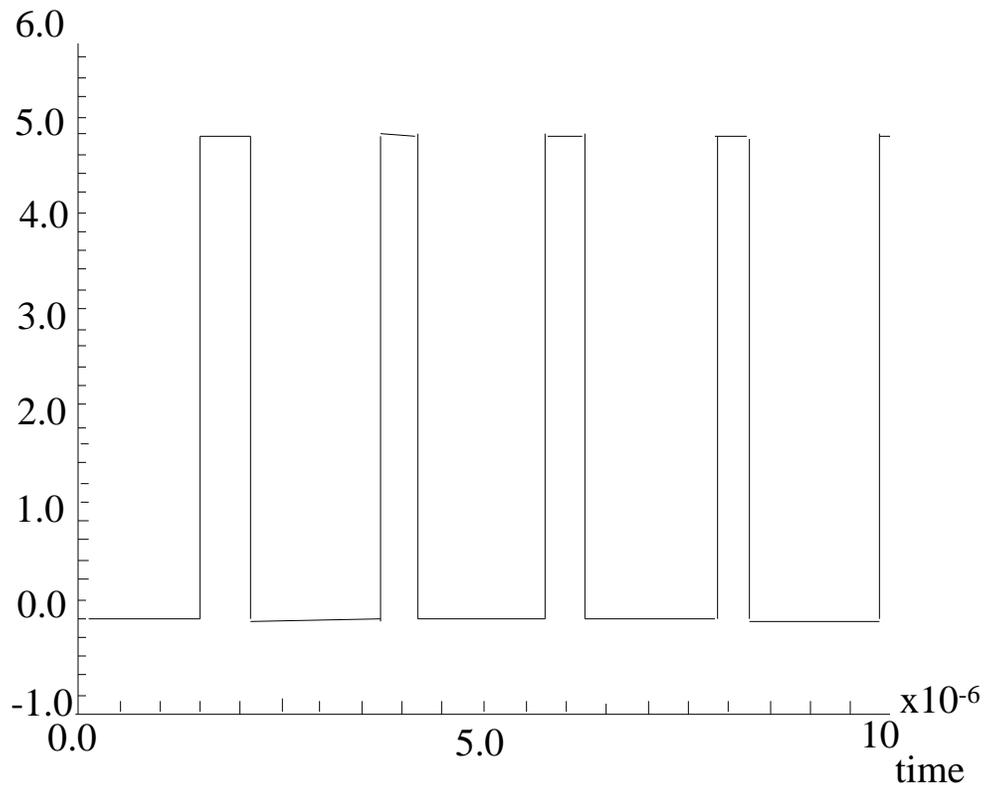
Figure 2.26 Simulation result of the ramp generator

Figure 2.27 Layout of the ramp generator(tif,32K,ramp.tif)

Maximum duty ratio is derived by comparing the ramp signal with a reference voltage. A reference value of 2.8 V is chosen to yield $D_{max} = 90\%$. The circuit diagram and simulation result are shown in Figure 2.28. Layout of the circuit is shown in Figure 2.29.



Transient Response



(b)

Figure 2.28 Maximum duty ratio generator (a) circuit diagram (b) simulation result

Figure 2.29 Layout of the dmax generator(tif,39K,dmax.gif)

The layout of the initial designed oscillator is shown in Figure 2.30, its area is $633 \mu\text{m} \times 330 \mu\text{m}$. The layout of the final design of the oscillator is shown in Figure 2.31, its area is $606 \mu\text{m} \times 234 \mu\text{m}$.

Figure 2.30 Layout of the initial designed oscillator(tif,56K,osc_o.tif)

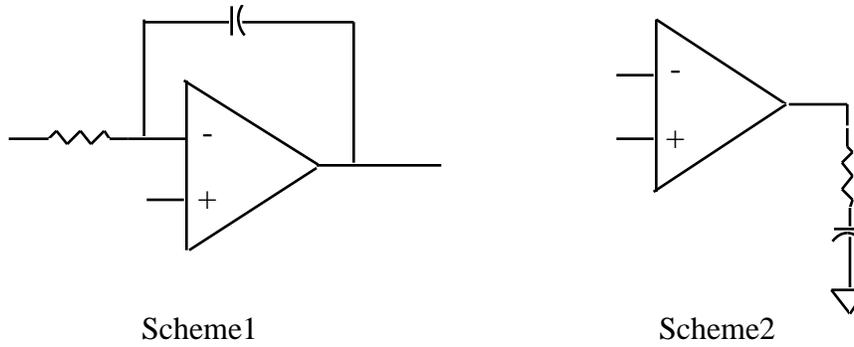


Figure 2.34 Compensation schemes for the Opamp

B. Final Design

Since the common mode input voltage is $(V_{ref}+V_i)/2$, where V_{ref} is 2.5 V , V_i is from 0 to 3.3 V normally, the common mode input voltage range will be 1.2 V ~ 2.9 V, common mode input voltage range requirement can be relaxed. The Opamp design is changed to that of Figure 2.35, an output stage is added to a two-stage transconductance Opamp, to get low output impedance and large output current. The design procedure for the Opamp can be summarized as follows: Since the input signal varies very slowly relative to the switching frequency, the unit gain bandwidth is set to 1 MHz, this is a good trade-off between high speed and low power dissipation, the slew rate is chosen to be 2 V/ μ s, for good large signal characteristic. The phase margin should be greater than 70° for small ringing in a step response. The output voltage swing should be greater than the ramp's peak to peak value which is 1 V to 3.54 V. Internal compensation uses a 4 pF capacitor in series with a 16 k resistor. Simulation shows a good compensation result over typical process variations.

Since $BW = \frac{gm_1}{C_c}$, $SR = \frac{I_B}{C_c}$, $I_{B1} = 12\mu A$, so $gm_1 = 4 \mu A/V^2$, For common mode input voltage range of 0.5 V to 3.6 V, V_{gs1} is chosen to be 1.5 V, the $(W/L)_1 = 100 \mu/5 \mu$. I_{B2} for the second stage is 44 μA , I_{B3} for the output stage is 210 μA . The DC transfer curve of the Opamp is shown in Figure 2.36, and the AC response is shown in Figure 2.37. Layout of the Opamp is shown in Figure 2.38. Cross-coupled input transistors are used to minimize input offset voltage of the Opamp.

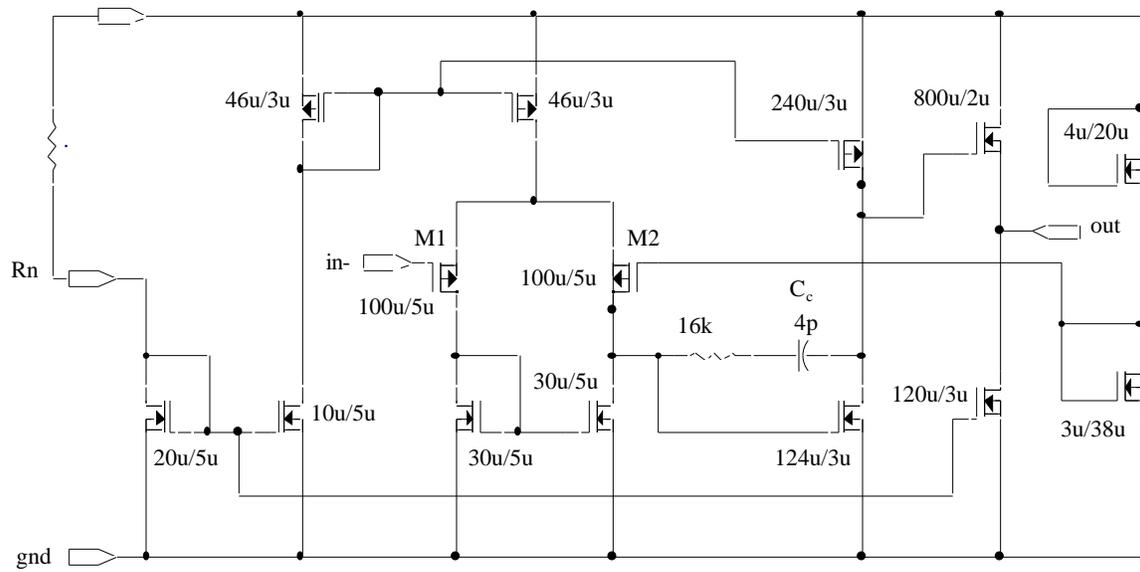


Figure 2.35 Schematic diagram of the Opamp with an output stage

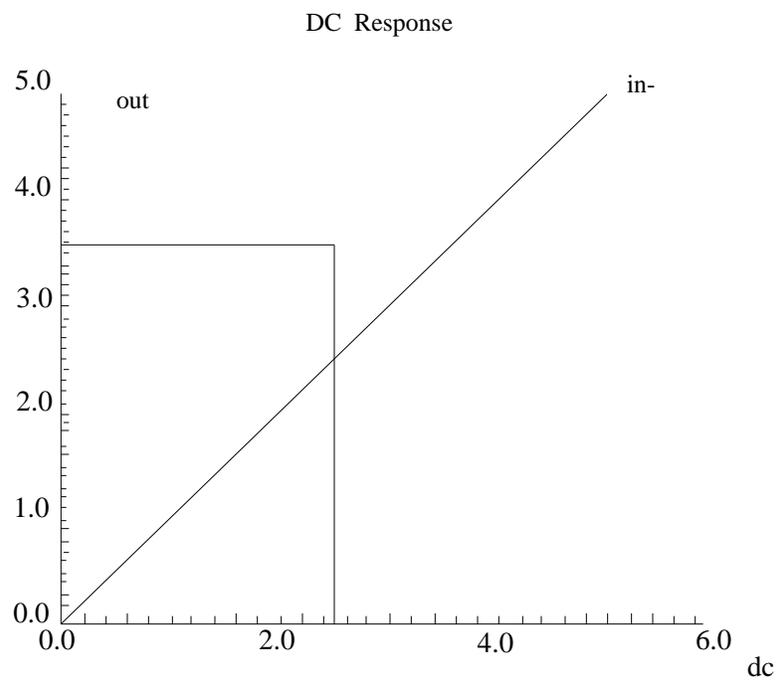


Figure 2.36 DC transfer characteristic of the Opamp in Figure 2.35

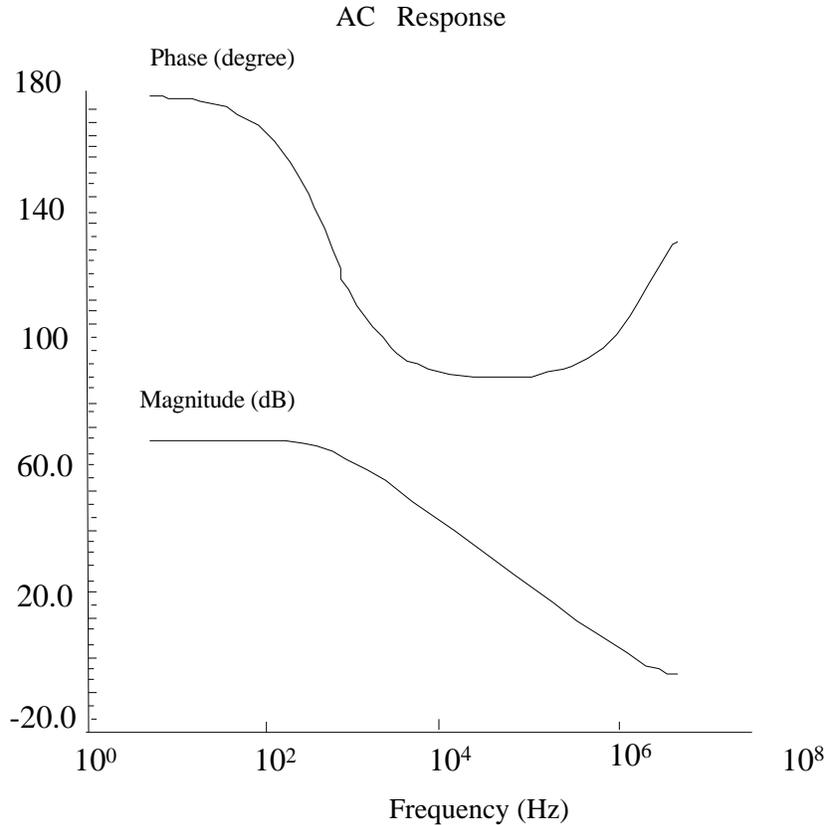


Figure 2.37 AC transfer curve of the Opamp in Figure 2.35

Figure 2.38 Layout of the Opamp in Figure 2.35(tif,56K,opamp.tif)

2.3.3 Voltage Reference

A. Initial Design

First design of the reference voltage uses a bandgap voltage reference and the designed circuit is shown in Figure 2.39.

When MOS transistors are operated at very low current, the channel which exists under the gate is extremely shallow and contains very few free carriers. This region of operation of the device is called weak inversion or subthreshold region, and the corresponding device currents are typically on the order of < 10nA per mil of channel width. In this region, the drain current exhibits an exponential dependence on the gate source

voltage as $I_d = \frac{W}{L} I_{D0} \exp \frac{V_{GS}}{nkT/q}$, instead of $I_d = \frac{W}{L} (V_{GS} - V_{th})^2$. Under

subthreshold conditions, the voltage drop difference between two MOS transistors with current source bias is nearly proportional to the absolute temperature T. Since the Vbe of bipolar transistor has a negative temperature coefficient, these two can be canceled out by proper choice of the design parameters. The temperature coefficient of Vref can be kept to

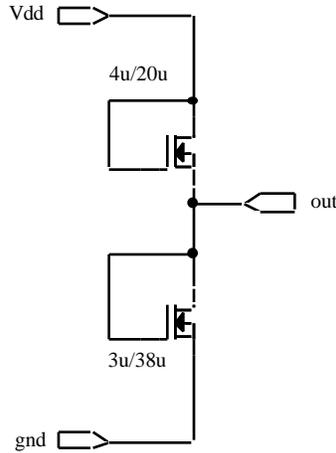


Figure 2.41 Voltage reference circuit diagram

2.3.4 Comparator

Comparator is an important element in PWM control, the performance of a comparator can be characterized by its (1) resolving capability or threshold sensing, (2) input offset voltage, (3) speed or propagation delay time, and (4) input common-mode range. The resolving capability V , can be expressed as $V = \frac{V_{OH} - V_{OL}}{A_v}$, as A_v becomes

large, the resolving capability approaches ideal. The input offset voltage, V_{os} is the value of the voltage applied between the inputs to make V_{out} equal to zero when V_p and V_n are connected together. The propagation time of the comparator is a measure of how quickly the output changes states after the input threshold has been reached. This parameter is very important since it determines how many comparisons the comparator can make per unit of time. The propagation delay generally varies as a function of the slope, the amplitude of the input, and its common mode value. A larger input or a steeper slope will generally result in a smaller delay time.

The common mode input range of the comparator is the range of voltages over which the comparator continues to sense the difference between applied input voltages. The resolving capability and input offset voltage are a function of the common mode input voltage.

Comparator can be implemented by three methods: use of a high-gain differential amplifier, use of positive feedback, and charge balancing. In this work, an Opamp structure is chosen, the key attribute of the differential amplifier is its ability to amplify the difference between inverting and non-inverting inputs over a wide common-mode range. As a result, the threshold point, or trip point, can be made independent of process and supply variations to a first order.

The design of the comparator is similar to the design of an Opamp, the differences are a comparator works in open loop, and no compensation is needed. While linearity is important for Opamp's design, a comparator's operation need not be linear, and speed is more important. The resulting circuit is shown in Figure 2.42. Since the load of the comparator is on chip circuits with small capacitance, an output stage is not needed.

Simulated AC transfer curve is shown in Figure 2.43. Layout of the comparator is shown in Figure 2.44.

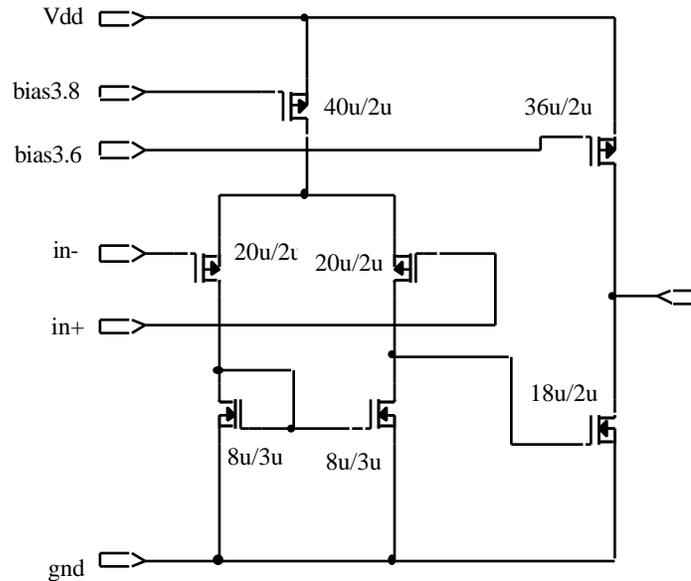


Figure 2.42 Schematic diagram of the comparator

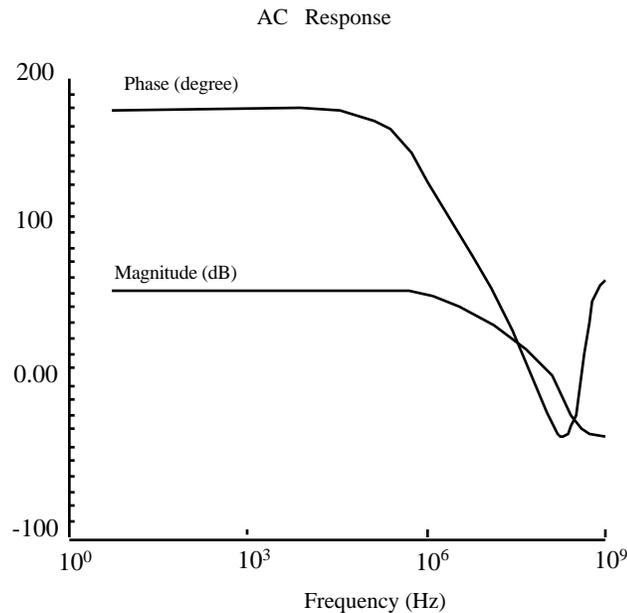


Figure 2.43 AC transfer curve of the comparator

The input offset voltage of the differential amplifier is due to mismatches in the devices. Mismatches of this type are unavoidable and result from imperfections in the process. Offsets can be minimized by using cross-coupled input transistors in layout. It is also desirable to keep the number of bends and corners in the layout to a minimum for the two devices that must match. Typical offsets in the differential amplifier range from 5 to 15

mV for CMOS. The input offset voltage can be reduced by using large areas for the devices and by keeping the gate source voltage small.

Figure 2.44 Layout of the compartor(tif,39K,comp.tif)

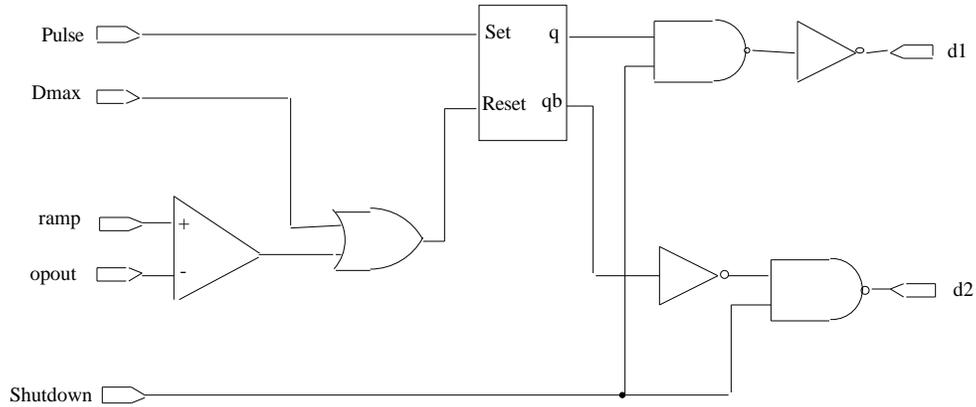


Figure 2.45 Schematic diagram of the PWM logic

2.3.5 PWM Logic

Design of the PWM logic part is straight forward, since all are digital logic, the transistors use minimum size, the schematic diagram is shown in Figure 2.45. The simulation result is shown in Figure 2.46 and the layout is shown in Figure 2.47.

Transient Response

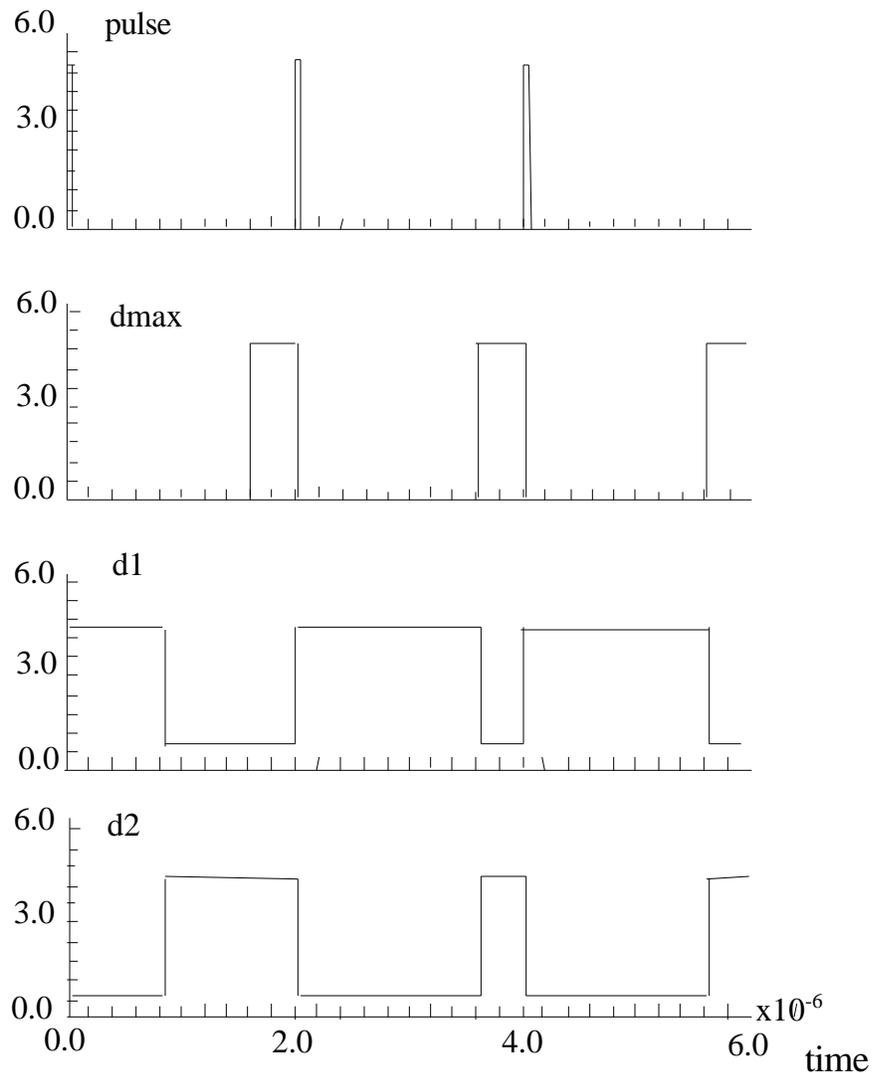


Figure 2.46 Simulation result of the PWM logic

Figure 2.47 Layout of the PWM logic(tif,48K,pwm.tif)

2.3.6 Delay Circuits

A. Initial Design

To delay the rising edge of two switches' on signals, the first design is shown in Figure 2.48. A RC constant delays the rising of the input signal, and the diode makes the falling edge unaffected. The inverter stage converts the 5 V logic to 10 V before it goes to the driver section. Since there is no simple diode implementation in the process, a diode

which uses nwell, nplus and pplus layer is designed. The delay time varies due to Capacitance's process variations. Layout of the initial design is shown in Figure 2.49.

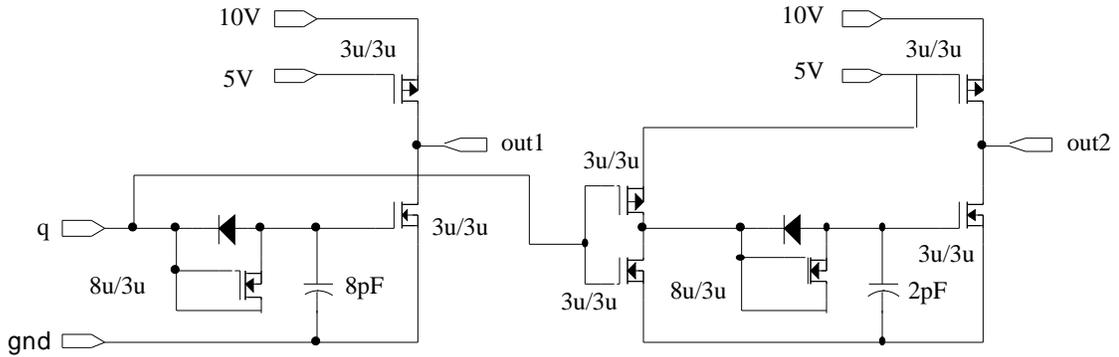


Figure 2.48 Schematic diagram of the delay circuit using RC constant

Figure 2.49 Layout of the delay circuit using RC constant(tif,31K,delay_o.tif)

B. Final Design

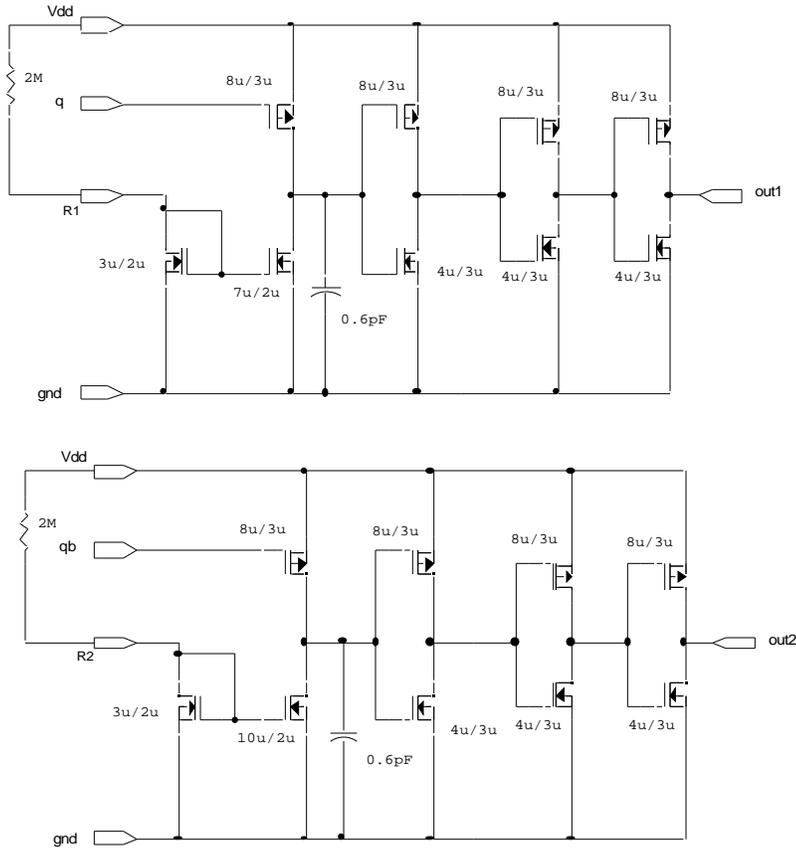


Figure 2.50 Schematic diagram of the delay circuit with constant discharge current

The delay circuit is modified to that shown in Figure 2.50. When input goes from low to high, a constant current discharges a capacitor, the rising edge is delayed by CV_{inv}/I , where V_{inv} is the threshold of the output inverter. When input goes from high to low, the capacitor is charged up rapidly, so the delay for the falling edge is very small. Discharging current is set by external resistor R1 and R2, and can be adjusted to obtain different delays. For a resistor value of $2\text{ M}\Omega$, the discharging currents are $9\mu\text{A}$ and $13\mu\text{A}$ respectively. The simulation results are shown in Figure 2.51. Simulation shows that the delay between the turn off of Q2 and the turn on of Q1 is 280 ns , and the delay between the turn off of Q1 and the turn on of Q2 is 180 ns . Layout of the delay circuit is shown in Figure 2.52.

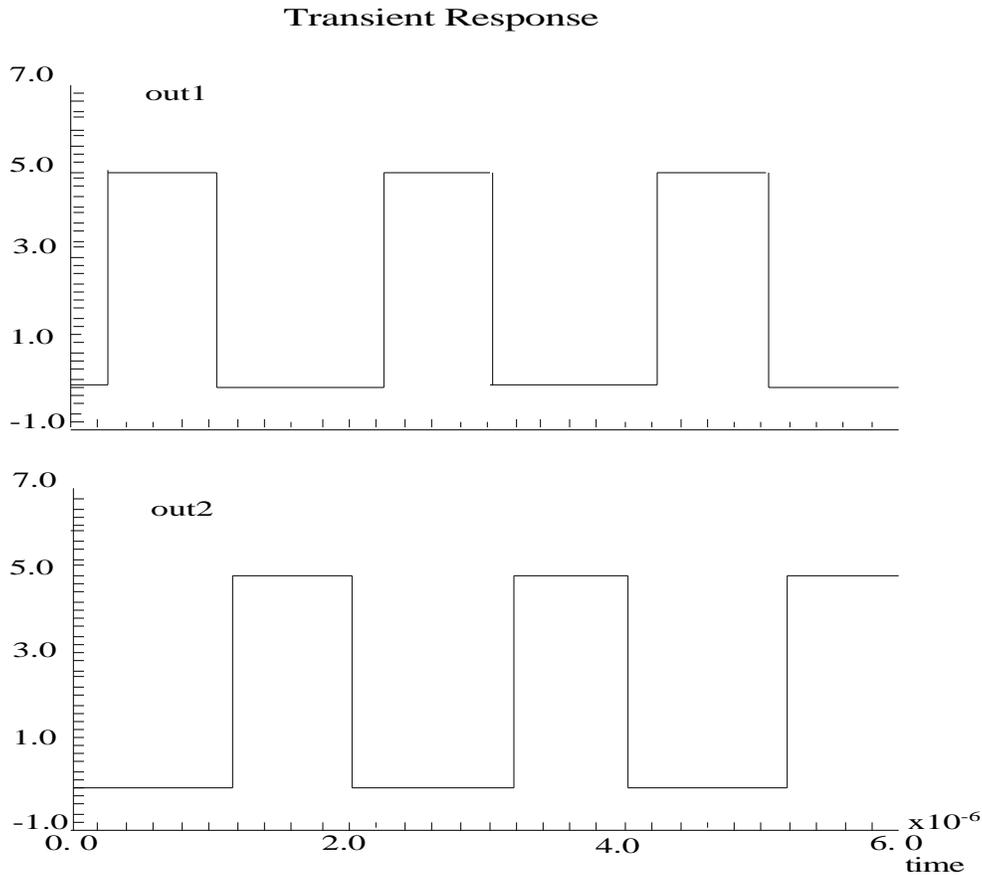


Figure 2.51 Simulation results of the delay circuit in Figure 2.50

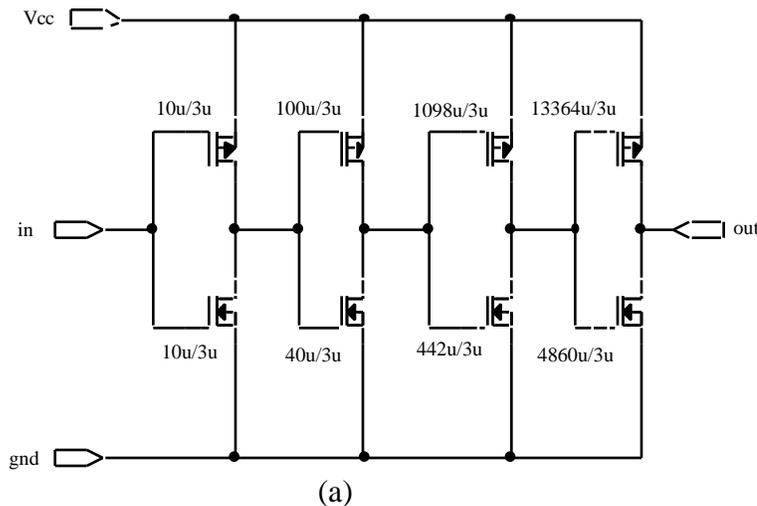
Figure 2.52 Layout of the delay circuit in Figure 2.50(tif,48K,delay.tif)

2.3.7 Drivers

The driver stage uses a series of cascaded inverters, with each inverter stage being progressively larger to achieve a lower driving impedance. If a simple RC model of the inverter is used, a scaling factor for minimum delay can be calculated to be 2.7 [10]. The

power dissipation of the circuit includes static power dissipation, dynamic power dissipation, and short-circuit power dissipation. Static power dissipation of CMOS inverters is mainly the substrate leakage current which is very small. Dynamic power dissipation equals to $P_d = V_{dd}^2 f C$, where V_{dd} is the supply voltage, f is the switching frequency, and C is the load capacitance. Short-circuit power dissipation is due to the fact that during switching, two transistors will both be in conduction for some time, there will a short-circuit current flowing from supply to ground. Dynamic power dissipation and short-circuit power dissipation all increase with frequency, so these buffer circuits need extra attention to obtain minimum power dissipation. Analysis shows that the short-circuit power dissipation will be less if the input rise and fall times are less than or equal to the output rise and fall time [11]. In this work, since the load is a large capacitance, the output rise and fall time will be much larger than the input rise and fall time. The ratio between two adjacent stages for minimum power dissipation is decided by V_{dd} , C , required signal rise and fall times and some process parameters. Based on the analysis and since the sensitivity of delay to changes in scaling factor is not particularly strong, a slightly larger scaling factor can be used instead of 2.7 to get the minimum power dissipation and less stages. Too many stages will also result in more power dissipation among these stages. Scaling factor chosen in the design is 9, and four stages are used.

Load capacitance is about 2800 pF and 1300 pF when directly driving two power MOSFETs. If 30 ns rise and fall time is required, assuming a triangular charging current waveform, the peak current is $2CV/t$ $r = 1.87$ A and 0.87 A respectively. Average current over one cycle is $I_p \times 30 / 2000 = 28$ mA and 13mA respectively. In layout of the driver stage, since the gate capacitance is large for the large transistors, the signal should be distributed as equally as possible to the paralleled transistors, large delay differences can make the short-circuit current larger. The gate capacitance and source-drain capacitance are large for the last stage, load capacitance of these stages should be give a 10% margin for design calculations. Metal connection of the driver to output, V_{cc} and ground should be wide enough, since large surge current will flow through, if too much current density is placed on the metal, there may be a problem of metal migration. Current density allowed for DC current for metal1 layer is 0.5 mA/ μ m and 1 mA/ μ m for metal 2. In layout the metal connections are made as wide as possible and no less than 240 μ m, the output of the last stage is connected in parallel to several pads for good conduction, this also minimized the inductance in the loop. The driver stage should be far from the sensitive analog part on the chip, like the voltage reference and Opamp. Layout of the Driver is shown in Figure 2.54.



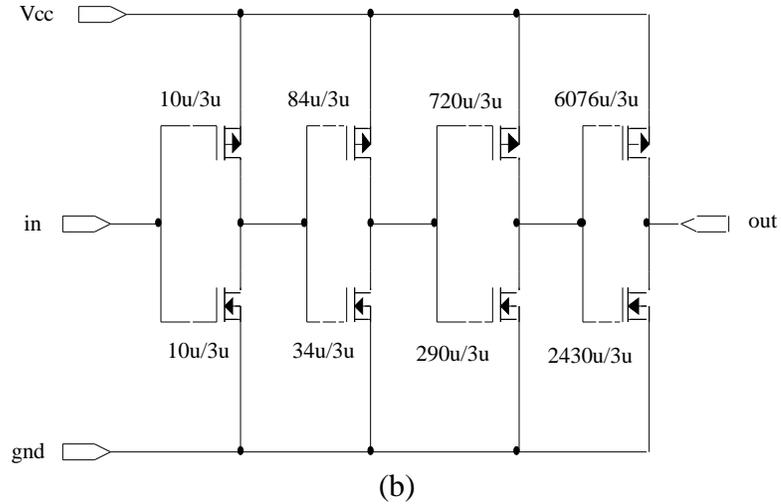


Figure 2.53 Schematic diagram of the driver circuits (a) driver 1 (b) driver 2

Figure 2.54 Layout of the drivers driver 1(tif,139K,drm.tif)

2.3.8 Soft-start Circuit

The soft-start circuit is shown in Figure 2.55. The operation of the circuit can be explained as follows: before power up, node 1's voltage is zero. After power up, PMOS M1 goes into conduction, since its gate source voltage is greater than its threshold, this pulls down node 2's voltage to just a threshold higher than that of node 1, so the Opamp's output is disabled. With the constant current charging up node 1, the voltage at node 2 also increases. After some time, when the voltage of node 1 is high enough, the difference between node 1 and Opamp's normal output voltage is smaller than PMOS's threshold, PMOS will turn off, the Opamp's output takes effect and determines the voltage of node 2. This implements the soft-start function in which the duty ratio increases gradually to the designed value. Charging current is $9 \mu\text{A}$. Soft-start time is determined by $t = C(V_{op} - V_{thp})/9\mu$, where C is an external capacitor connected to SS terminal. Layout of the soft-start circuit is shown in Figure 2.56.

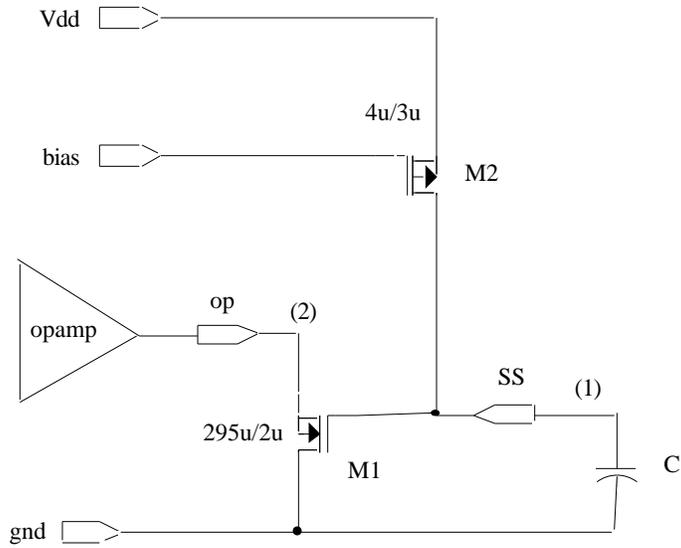


Figure 2.55 Schematic diagram of the soft-start circuit

Figure 2.56 Layout of the soft-start circuit(tif,28K,soft.tif)

The layout of the control chip of the initial design and the final design are shown in Figure 2.57 and Figure 2.58 respectively.

Figure 2.57 Layout of the control chip for initial design(tif,136K,whole_o.tif)

Figure 2.58 Layout of the control chip for final design(tif,266K,whole.tif)

Chapter 3

VLSI Realization

3.1 IC Design Overview

IC design goes from system level design to transistor level design and physical design. Because of the complexity involved in VLSI, Computer Aided Design (CAD) is indispensable in the IC design process from schematic capture, simulation to layout and design rule checking. A typical IC design flow is shown in Figure 3.1.

3.2 IC Design Procedure

There are three kinds of IC designs, full-custom, semi-custom and standard. In full custom design, all circuits are designed specifically for the system, this gives the most efficient design, and is usually the method for ASIC designs, but involves big design effort and long design cycle. Semi custom design uses some programmable cells, and standard design is done by interconnecting standard cells to realize the function. These may not be efficient for the designs, but involves less design effort. The PWM control chip discussed in Chapter 2 is a full custom design. The design starts at system level, top down or bottom up method can be adopted for system level design. Bottom up design is used for designing with standard cells. In this design, top down method is used. System level design should take into considerations of issues such as what kind of circuits will be implemented at lower level, and an architecture that can effectively implement these circuits should be chosen. The system level design is then partitioned into sub-blocks, the interfaces between the blocks are defined. If the system is very complex, the partition may go on for several times. Simulation is carried at all levels with behavioral model, structure model and spice models.

Each block, like Opamp or voltage reference, is then designed at transistor level, their specifications are derived from the operation of the system. A proper topology is selected which can meet these specs. Biasing current is chosen and transistor sizes are designed by calculation and simulation. The analog simulators used in this design include PSPICE and Spectra from Cadence. Spice models are provided by the fabrication foundry, in this case MOSIS level 3 MOSFET model is used. For some cases, different models may be used to characterize different devices.

Layout design is performed after transistor level circuit design and translates the circuit to the physical layers of the fabrication foundry. These layers correspond to different masks used in the process, i.e. diffusion, metal or polysilicon deposition, etc. Layout design may be done manually or use standard layout libraries if available. Automatic generation of layout is possible, but is usually used for digital circuits. For analog circuits, since layout appears to be non-uniform, and the circuit's performance is largely affected by the layout design, usually experienced manual design provides more efficient solutions. The design should abide certain design rules set by the foundry. For example, the MOSIS design rules are listed in the Appendix A. These rules ensure proper design of the devices and adequate yield of the chip.

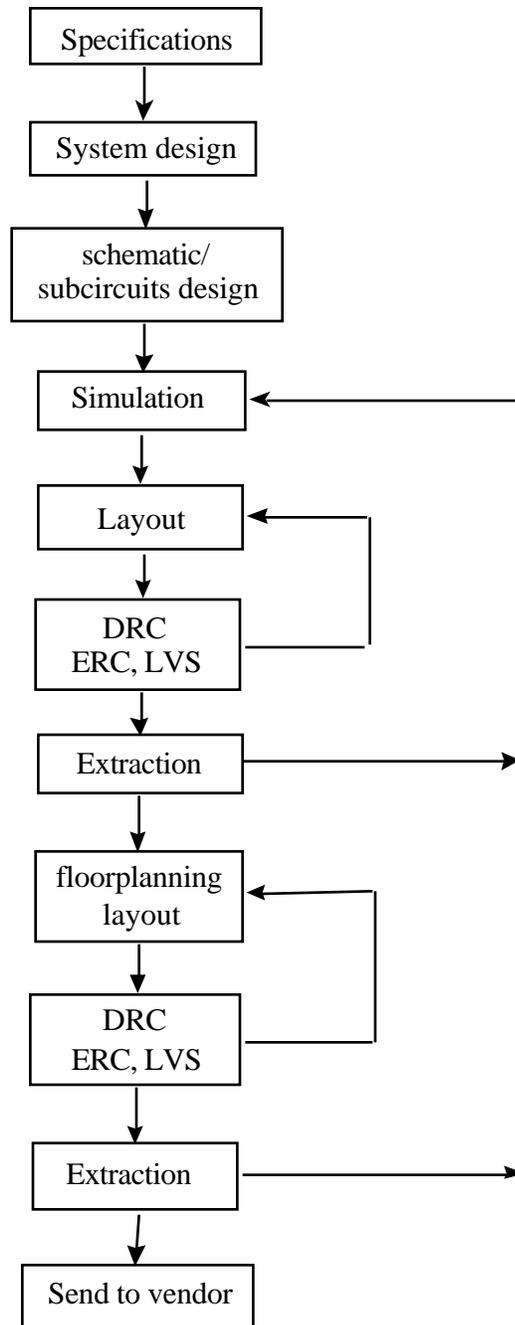


Figure 3.1 IC design flow

3.3 DRC, ERC, LVS Checking

The designed layouts must pass several steps of checking which are important for a successful design, these are DRC, ERC and LVS checking. Design Rule Checking (DRC) checks the layout for design rules violation. Electrical Rule Checking (ERC) checks that

electrical rules are met, such as V_{dd} is not floating, etc. Layout Versus Schematic (LVS) checks the circuit implemented by layout is the same as the designed schematic. In a LVS checking, a schematic is first extracted from the layout, devices and their connections are identified, then the netlist generated from the extracted layout is compared with the netlist generated from the original schematic. Below shows a typical LVS checking and ERC checking output file from Cadence.

LVS checking output file

```
LVS version 4.3.4 Mon Aug 28 23:47:55 PDT 1995 (cmrd2)
Library is 9601
Path is /cad/ldaLibrary/standards/4.3/opusLib/analogLib /user/dongwei/usr3/mosis/PennLib
/user/dongwei/usr3/cadence_local ~ ./cad/9502/tools.sun4/dfII/etc/cdslib
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
```

Net-list summary for /home2/huangale/usr3/vsp9601/LVS/layout/netlist

```
count
  6      nets
  5      terminals
  2      mosn
  2      mosp
```

Net-list summary for /home2/huangale/usr3/vsp9601/LVS/schematic/netlist

```
count
  6      nets
  5      terminals
  2      mosn
  2      mosp
```

Terminal correspondence points

```
  1      gnd!
  2      in1
  3      in2
  4      out
  5      vdd!
```

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4
	nets	
un-matched	0	0
merged	0	0
pruned	0	0

active	6	6
total	6	6
	terminals	
un-matched	0	0
total	5	5

ERC checking output file

ERC version 4.3.4 Wed May 31 19:03:13 PDT 1995 (cmrd2)
Warning: Net name 'vss!' in user input, not in netlist.
Warning: Device type "npn" used in "path" definition not found. Ignoring information.
Warning: Device type "npn" used in "path" definition not found. Ignoring information.
Found 0 bad net errors.
Found 0 bad device errors.
Found 0 bad connection errors.

All the checking is done by computer, rules can be input or modified for different foundries. DRC rules are implemented by logical operation of different layers. LVS rules are implemented by first defining composite layers, then defining devices based on these layers' geometrical sizes.

In Cadence, these are defined in a technology file. Part of the file can be seen below which defines some of the DRC, ERC, LVS rules.

Example of a technology file

```
drcExtractRules(ivIf!(switch "ORB20")
(Nwell = geomOr("Nwell"))
(Pselect = geomOr("Pselect"))
(Nselect = geomOr("Nselect"))
(Active = geomOr("Active"))
(ActX = geomOr("ActX"))
(Poly1 = geomOr("Poly1"))
(P1Con = geomOr("P1Con"))
(Poly2 = geomOr("Poly2"))
(P2Con = geomOr("P2Con"))
(P2Active = geomAnd(geomNot(Poly1) Active))
(Metal1 = geomOr("Metal1"))
(Metal2 = geomOr("Metal2"))
(ViaX = geomOr("ViaX"))
(Glass = geomOr("Glass"))
(XP = geomOr("XP"))
(ngate = geomAndNot(geomAnd(NActive Poly1) NotTran))
(pgate = geomAndNot(geomAnd(PActive Poly1) NotTran))
(gate = geomOr(ngate pgate))
geomConnect((via ViaX Metal1 Metal2)
(via P1Con Poly1 Metal1)
(via P2Con Poly2 Metal1)
(via ActX NSD PSD Metal1)
(via ActX base Metal1))
```

```

(via NTap Nwell1 NSD)
(via PTap Pwell PSD)
(via ActX NTapNWRes NTapNDRes PTapPDRes
  Metal1
)
(label "text" Metal1 Metal2 Poly1
  Poly2 Resistor Capacitor
)
)
ivIf((switch "drc?") then

  (K1 = geomAndNot(Poly1 Active))
  (K2 = geomSize(K1 0.5 edges))
  (K4 = geomAnd(gate K2))
  (K5 = geomAndNot(Active Poly1))
  (K6 = geomSize(K5 0.5 edges))
  (K7 = geomOr(geomOr(geomOr(geomEnclose(gate K4
    (keep == 1)
  )
    geomOutside(gate K4)
  )
    geomEnclose(gate K6
    (keep == 1)
  )
    geomOutside(gate K6)
  ))
)
drc(Nwell1
  (sep < 6) sameNet "Well separation at same pot. must be at least 6 (Mosis rule
1.3)"
)
drc(Nwell Pbase
  (enc < 6) "Nwell must overlap Pbase by 6"
)
(emitter = geomAnd(Pbase NSD))
(emc = geomAnd(ActX
  geomAnd(Pbase Nselect)
))
(baseact = geomAnd(Pbase
  geomAndNot(Active Nselect)
))
drc(emitter emc
  (enc < 3) "Emitter active must overlap contact by 3"
)
drc(baseact emitter
  (sep < 4) "Base and Emitter actives must be 4 apart"
)
drc(Active
  (width < 3) "Active width must be at least 3 (Mosis rule 2.1)"
)
drc(Active
  (sep < 3) "Active separation must be at least 3 (Mosis rule 2.2) "
)

```

```

)
(A1 = geomAnd(Nwell Active))
(A2 = geomAndNot(Active Nwell))
drc(A1 A2
  (sep < 1) "Active should not overlap well edge"
)
(nsource = geomAnd(geomAnd(Active Nselect)))
(psource = geomAnd(geomAnd(Active Pselect) Nwell))
drc(Nwell nsource
  (sep < 5) "Sourcedrain active must be at least 5 from well edge (Mosis rule 2.3)"
)

ivIf(((switch "ORB20") ||
  (switch "VTI20")) then
  (GP1 = geomStretch(Glass 6))
  (GP2 = geomSize(GP1 6 edges))
)
ivIf((switch "extract?") then
  ivIf(((switch "ORB20") ||
  (switch "VTI20")) then
    (lambda = 1.0)
    (lambdaSq = (lambda * lambda))
    extractDevice(ngate
      (Poly1 "G")
      (NSD "S" "D")
      (Pwell "B") "mosn symbol"
    )
  )
  (NGateWidth = measureParameter(length
    (ngate coincident Poly1) 0.5
  ))
  (NGateLength = measureParameter(length
    (ngate inside Poly1) 0.5
  ))
  (ScaledNGW = calculateParameter((NGateWidth * lambda * 1e-06)))
  (ScaledNGL = calculateParameter((NGateLength * lambda * 1e-06)))
  saveParameter(ScaledNGW "w")
  saveParameter(ScaledNGL "l")
  (NDrainArea = measureParasitic(area
    (NSD not_over Nwell) figure
  ))
  (NDrainPeri = measureParasitic(perimeter
    (NSD not_over Nwell) figure
  ))
  (ScaledNAD = calculateParasitic((NDrainArea * lambdaSq * 1e-12)))
  (ScaledNPD = calculateParasitic((NDrainPeri * lambda * 1e-06)))
  attachParasitic(ScaledNAD
    ("as" "S")
    ("ad" "D") ngate
  )
  attachParasitic(ScaledNPD
    ("ps" "S")

```

```

        ("pd" "D") ngate
    )
    saveRecognition(ngate "Poly1")
)

lvsRules(procedure((compareMOS m1 m2)
    prog((x y)
        if((((m1->l) != nil) && ((m2->l) != nil)) then
            (x = ((m1->l) * 1000000.0))
            (y = ((m2->l) * 1000000.0))
            if((abs((x - y)) > 0.001) then
                sprintf(errorL "Gate length mismatch: %g != %g" x y)
                return(errorL)
            )
        )
        if((((m1->w) != nil) && ((m2->w) != nil)) then
            (x = ((m1->w) * 1000000.0))
            (y = ((m2->w) * 1000000.0))
            if((abs((x - y)) > 0.001) then
                sprintf(errorW "Gate width mismatch: %g != %g" x y)
                return(errorW)
            )
        )
    )
    return(nil)
)
)

ercRules(setPower("vdd!")
    setGround("vss!" "gnd!")
    oneWayPath("npn" "C" "E")
    oneWayPath("npn" "B" "E")
    twoWayPath("mosn" "D" "S")
    twoWayPath("mosp" "D" "S")
    checkFloatingDevices()
    checkFloatingNets()
    checkOneNetDevices()
    checkOneTerminalNets()
    checkConnected("mosn" "B" "vdd!")
    checkConnected("mosp" "B" "gnd!")
)

```

After these checkings, a parasitic parameter extraction of the layout can also be performed for a more accurate circuit simulation.

3.4 Parasitic Parameter Extraction

After DRC, ERC, LVS checking, an extraction of layout parasitics may be performed, since in circuit design simulation, parasitics are not considered. In reality, there are parasitic resistors and capacitors associated with interconnect and diffusions. For some critical circuits, the parasitics may lower the performance of these circuits significantly. These parasitics generate additional delays, deteriorate signal levels, sometime can even cause oscillation and malfunction of the circuits. As device's dimensions continue to scale down, the parasitic of interconnections becomes the major issue in deep submicron design.

For some other circuits, these parasitic may not be very important, depending on the performance required.

For parasitic extraction, the parasitic parameters of different layers are initially given and stored in the technology file, then an extraction of layout is performed, which extracts the parasitic components along with the devices. The generated netlist is simulated in Spectra to verify if it still meets the requirement. If not, the layout should be modified or the circuit itself needs to be modified. This process may be iterated. For example, Figure 3.2 shows the extraction of one of the drivers which illustrates the influence of parasitics.

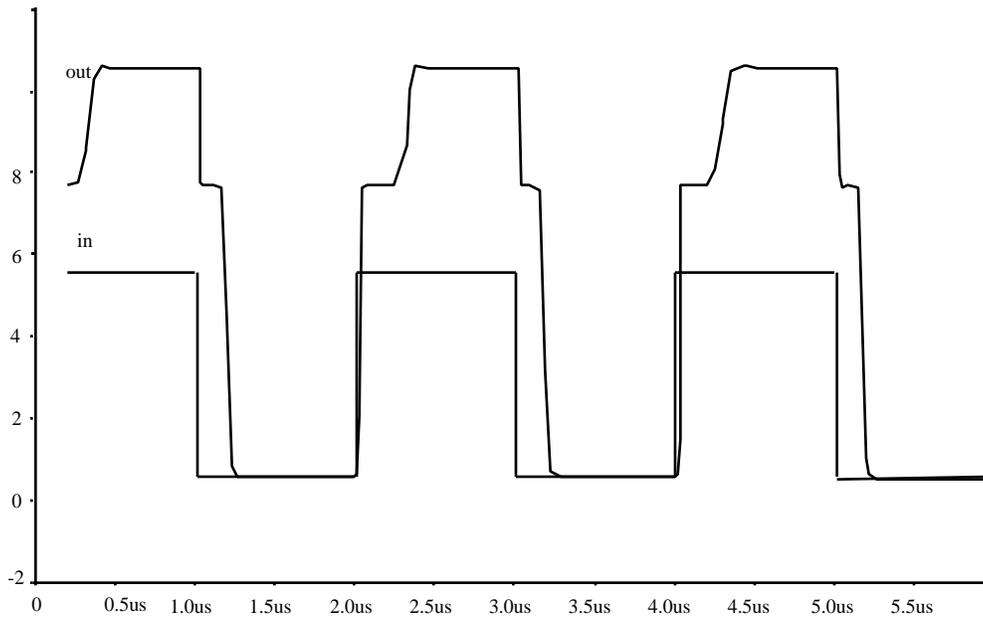
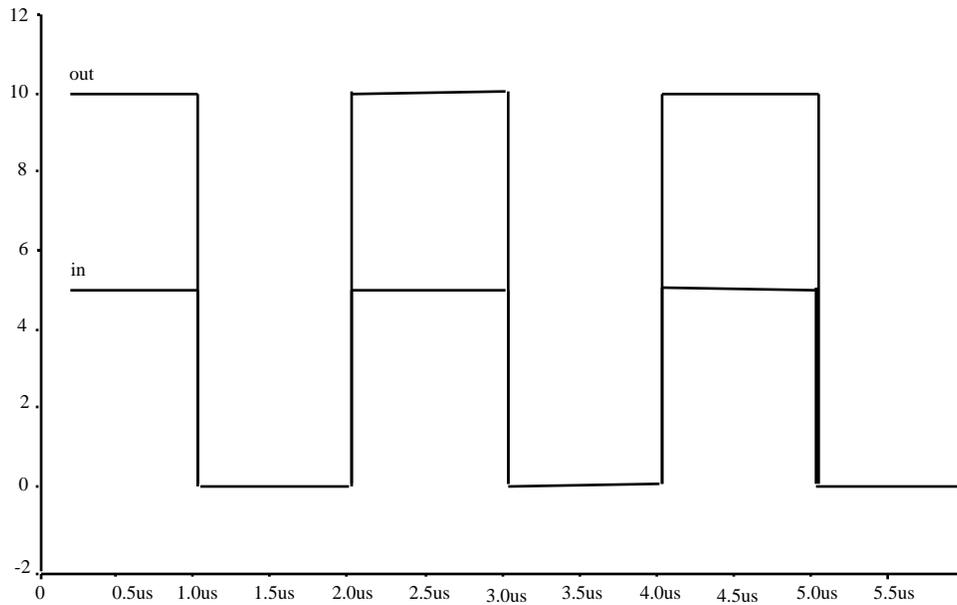


Figure 3.2 Simulation result of driver 2 (a) without parasitic (b) with parasitic

3.5 Chip Level Design

After checking and extraction to make sure all circuits will work properly, system level floor planning is performed, which integrates the individual blocks on the chip. Considerations include how to distribute the power line, ground line, clock, etc., and the placement of each block. Analog and digital part should be separated and have separate grounds. For small system, this can be done manually. For big system, computer aided floor-planning is used. After this, interconnection of all the sub-blocks is performed and connected to the pads. Then DRC, ERC, LVS checking is performed at the chip level. If needed, extraction and simulation will be performed, especially for critical signal path in high speed circuit. In the current PWM control chip design, since the chip is relatively small and the circuits are not operating at very high speed, the effect of parasitics is pretty much predictable, extraction is not performed. At this stage the design is completed, then the layout is transferred to MOSIS in standard format (GDS or CIF), in our case CIF, for wafer level fabrication. MOSIS will return the packaged chips in six to ten weeks. The detailed system diagram of the ASIC control chip is shown in Figure 3.3.

3.6 Experimental Results

Two versions of design were fabricated by MOSIS. The final chip has a total area of 2.2 mm×2.2 mm, and a power dissipation of about 100 mW. It is packaged in a standard 40 pin package from MOSIS. The chip is shown in Figure 3.4. Preliminary tests show the oscillator of the first design can operate at 200 kHz, this is smaller than designed

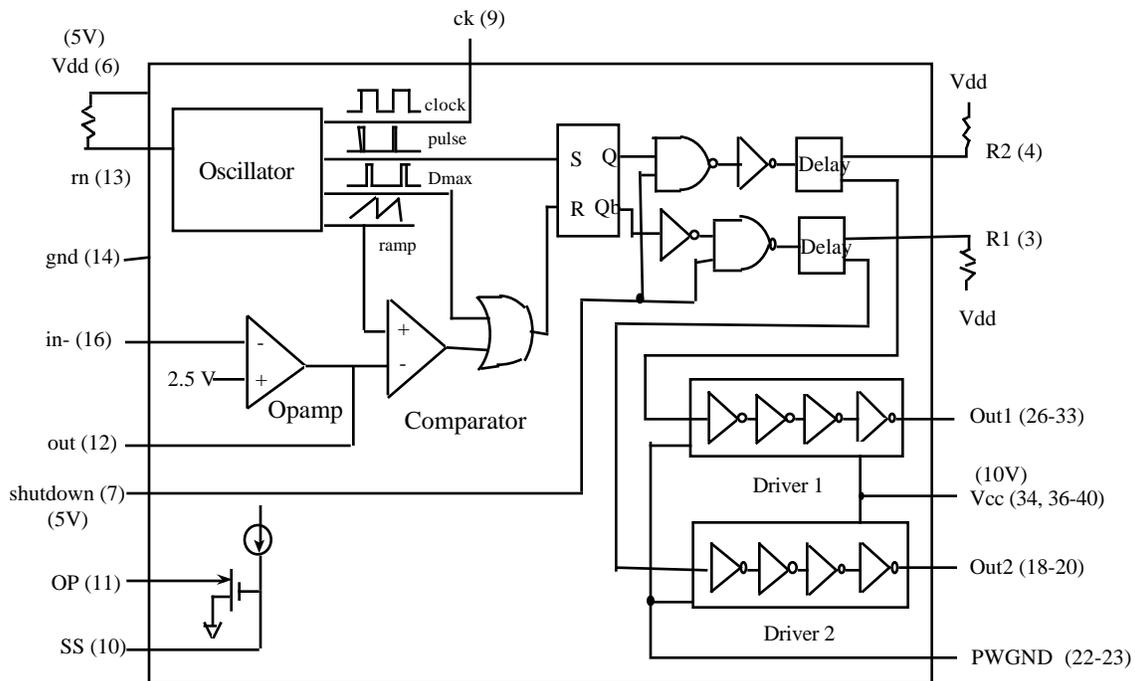


Figure 3.3 System diagram of the ASIC control chip

because of a larger loop delay. The ramp signal and Dmax signal operating at 25 kHz from the oscillator of the first design is shown in Figure 3.5, and the ramp signal operating at 200 kHz is shown in Figure 3.6. The final design can operate above 500 kHz, the clock signal from the oscillator section of the final design and the 20% and 70% duty ratio control signals output for the auxiliary switch are shown in Figure 3.7 and Figure 3.8. The two control signal outputs for the main switch and the auxiliary switch are shown in Figure 3.9, the top waveform is the control signal output from the driver for the main switch's duty ratio, the bottom waveform is the control signal output for the auxiliary switch's duty ratio, both of the drivers are connected with a load capacitor of 300 pF. The delay time between the turn-off of the auxiliary switch and the turn-on of the main switch is about 280 ns, and the delay time between the turn-off of the main switch and the turn-on of the auxiliary switch is about 200 ns. The designed chip can operate at duty ratio higher than 60%, and the delay time between the switches can be adjusted to optimize the performance of the converter. When driver 1 for the main switch drives a load capacitor of 300 pF from 0 to 10V, the output waveform is shown in Figure 3.10, the rise time is about 8 ns, so the charging current capability can be calculated roughly to be 0.8 A peak value. The driver's driving capability will be limited by the metal interconnection layers, bonding pads and package. More information can be obtained by testing the PWM control chip with the power stage to see the driving performance of the drivers when driving power MOSFETs.

Figure 3.4 PWM control chip(tif,31K,p34.tif)

In order to get high-performance high-density hybrid converter assemblies, there is considerable advantage to be gained from developing specialized components for specific applications. This is particularly true of control/drive IC's, where many external components are required in conjunction with general purpose IC's. For this reason, a library of controller/driver integrated subcells needs to be developed so that application-specific designs can be rapidly implemented. CMOS is an ideal technology for this development because of the subcell methodology used by very large scale integration (VLSI) designers, the scalability of the designs, the standardization of CMOS processes,

Figure 3.5 Ramp and Dmax at 25 kHz(tif,53K,p35.tif)

Figure 3.6 Ramp signal at 200kHz(tif,118K,p36.tif)

Figure 3.7 20% duty ratio output for the auxiliary switch and the clock signal(tif,63K,p37.tif)

Figure 3.8 70% duty ratio output for the auxiliary switch and the clock signal(tif,63K,p38.tif)

Figure 3.9 Duty ratio output for the main switch and the auxiliary switch(tif,62K,p39.tif)

Figure 3.10 Output waveform from driver 1 for the main switch when driving a 300 pF capacitor(tif,61K,p310.tif)

and the intrinsically low-power dissipation. The research presented in this paper shows the possibility of implementing wide variety of control and drive schemes for power circuits with CMOS technology. This work is only a beginning, there are many high-performance analog control blocks that need to be developed to provide a comprehensive library of controller/driver subcells.

Part II

NOVEL INTEGRATABLE LATERAL POWER DEVICES

Chapter 4

Overview of Lateral Power Devices

4.1 Motivations

Power Integrated Circuits (PIC) are ICs that include both power devices and low-voltage circuits on the same chip. PIC has many applications, some examples are listed in Table 4.1. As seen from the table, there is a big potential market for PICs.

Printer/Fax	Smart power drivers for motors & solenoids
Telephone	Hook switch Single-chip telephone
Automotive	Smart motor & solenoid drivers Multiplex switches
Disk Drives	Spindle motor Read/write head positioners
TV/Monitor	Deflection power ICs Audio power amplifiers
CO/PABX	Slic Solid-state relay
Power Supply	Monolithic switch mode supplies High-voltage bridges
Lighting	Lamp ballast

Table 4.1 Applications of PICs

Possible components in a PIC chip include input interfaces, signal processing and power supply as shown in Figure 4.1, all on the same chip.

In PIC designs, a wide variety of power devices will be needed for different applications, it is important to investigate different kinds of power devices that can be integrated. Design of these devices should optimize the device's performance, without introducing too much complexity in the process at the same time, to make it circuit wise efficient, and at relatively low cost. Discrete vertical power devices have evolved from bipolar devices to power MOSFETs, to IGBTs and MCTs. Lateral power devices also undergo similar development cycle from bipolar to MOSFET, to MOS controlled bipolar devices. In this part, several novel lateral MOS controlled power devices are analyzed, including lateral IGBT, lateral MCT, and double gate lateral MCTs.

Possible Components in a Complex PIC Chip

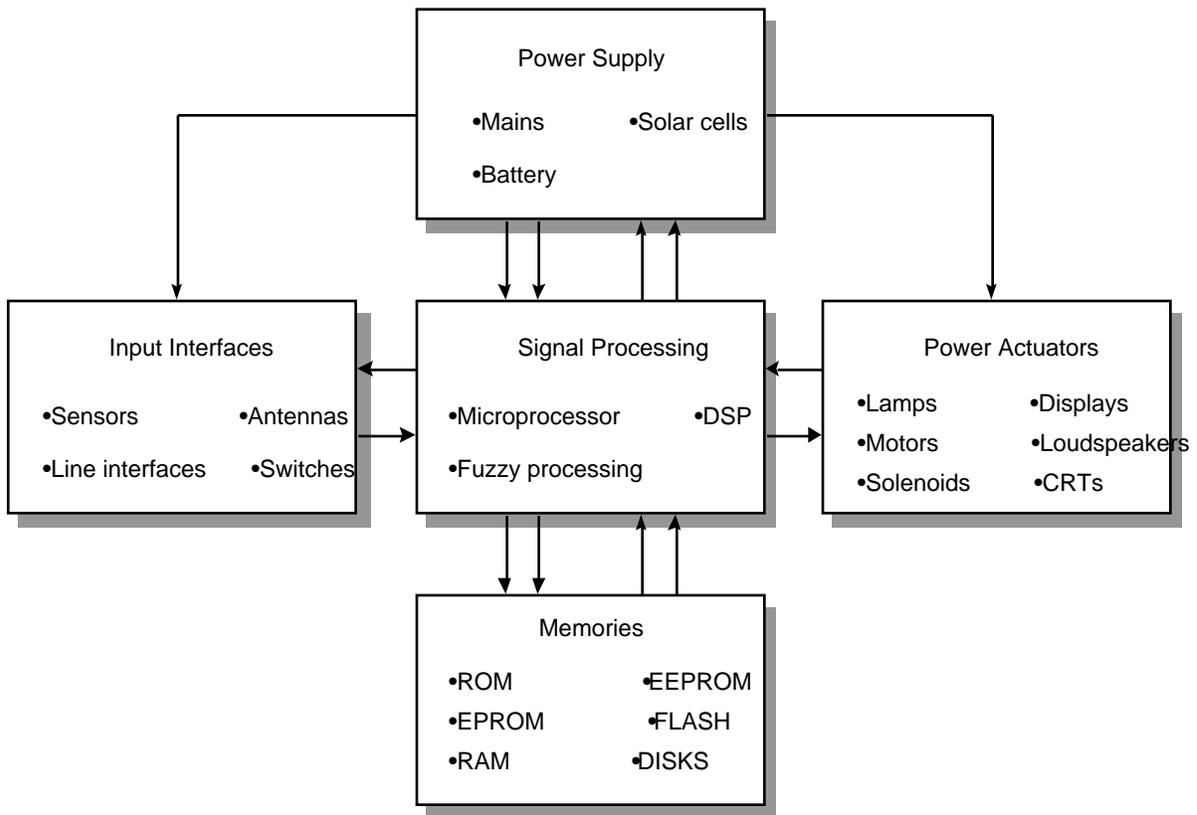


Figure 4.1 Components in a PIC chip

4.2 Overview of Lateral Power Device Techniques

Power devices are needed in PICs for various applications, e.g. to substitute the relay switch in the telephone subscriber loop. Lateral power devices are usually used in PIC processes instead of vertical power devices so as to be compatible with low-voltage IC circuits. Several additional process steps can be added to the low-voltage circuit process for power device's fabrication. In order to control these lateral power devices, MOS-gated power devices are deemed attractive. MOS-gated devices can be further partitioned as either work in a continuous mode of operation or in an interrupted mode of operation. In the continuous mode, the gate voltage not only switches the device 'on' and 'off', but also controls the flow of current within the devices continuously. In the case of interrupted mode of operation, the gate is used only to turn the device either 'on' or 'off' and the current is not controlled by the gate. MOS-gated devices can also be classified according to current conduction mechanism, either majority carrier or both majority and minority carriers, and the type of minority carrier injector, i.e. pn junction or Schottky contact. Figure 4.2 shows a classification of MOS-gated power devices.

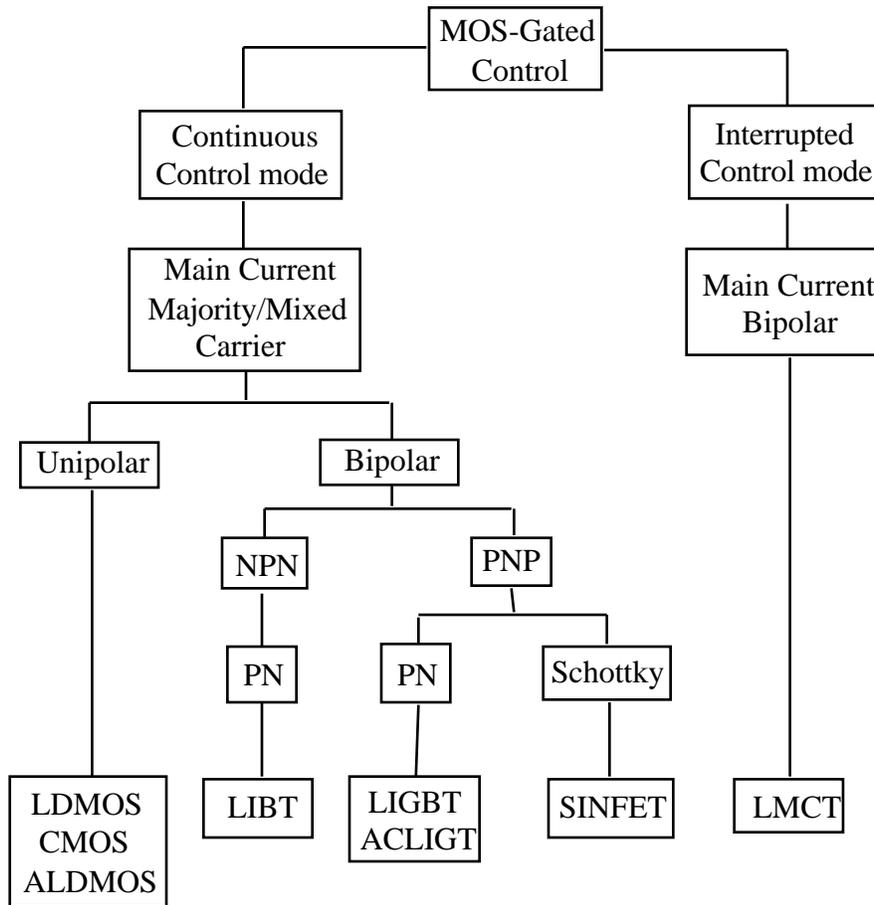


Figure 4.2 MOS-gated power devices overview

Usually the power devices are used as switches, and the requirements for them include: low on-state voltage drop to minimize conduction loss; high current density for low die cost; high input impedance for ease of drive; fast turn off to minimize switching loss; controlled turn on to reduce electromagnetic interference (EMI), diode recovery and voltage overshoots; and finally a large SOA. To design power devices with these characteristics, proper device design and optimization are needed. Some techniques used to aid lateral power device designs include REDuced SURface Field principle (RESURF), double diffusion and field plate.

RESURF Principle

RESURF principle utilizes lightly doped substrate along with a thin epitaxial layer to block high voltage. Figure 4.3 shows a cross section view of a RESURFed diode structure.

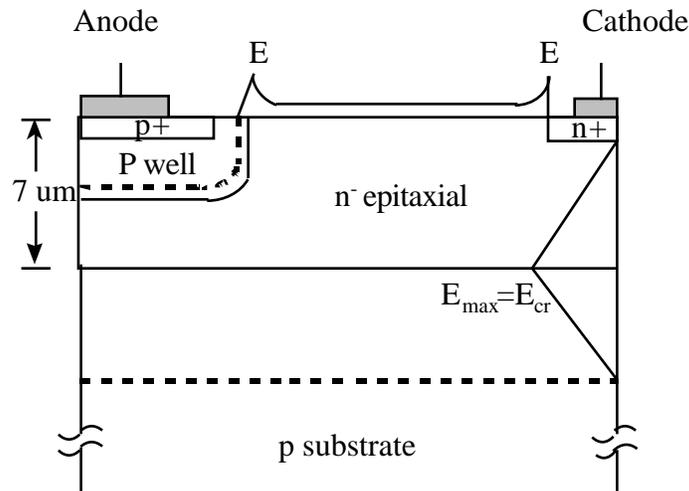


Figure 4.3 Cross section of a diode

When a positive voltage is applied to the n+ ohmic contact, the depletion layer on the side of the epitaxial drift region is increased from both X and Y directions by reverse biasing the junctions formed between the P-well and n- epitaxial region and that between the p substrate and n- epitaxial layer. Since the P-well is heavily doped, the depletion region spreads mostly into the lightly doped epitaxial layer side, while the substrate is lightly doped, the depletion region spreads on both sides of the horizontal junction. When this latter depletion region moves towards the surface, it will interact with the depletion region of the P-well – n- junction, and the total effect is that the depletion edge will be seen moving faster towards the n+ region, leading to a strong reduction in the surface electric field. This condition is true if the length of the drift region is much larger than the thickness of the drift region. So the applied reverse voltage is laterally and equally distributed along the surface and the peak electric field is forced to be in the bulk junction, and the breakdown can therefore be achieved when the horizontal junction breaks down. This makes it possible for lateral power devices to block high voltage even with a thin epitaxial layer.

Double diffusion and field plate

Double diffusion is the process used to diffuse Phosphorus and Boron sequentially from the same window opening. The difference between the lateral junction depth of the two diffusions determines the channel length. By this method, a relatively short channel can be obtained without submicron design rule. Figure 4.4 shows the concept of double diffusion.

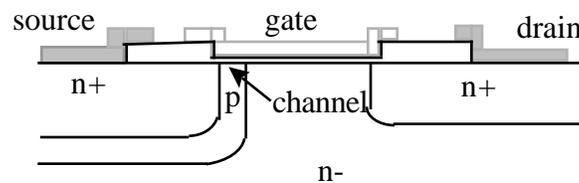


Figure 4.4 Double diffusion

Field plate technique is used in PIC to enhance the voltage blocking capability of the power device. Figure 4.5 shows a reverse-biased junction with a field plate. The curvature of the junction is large for shallow diffusion which is conventional for PIC process. The larger the curvature, the higher the electrical field, and the lower the breakdown voltage. Field plate

is therefore added to extend the peak electric field point away from the junction, effectively reducing the junction curvature, and increasing the blocking voltage at the surface.

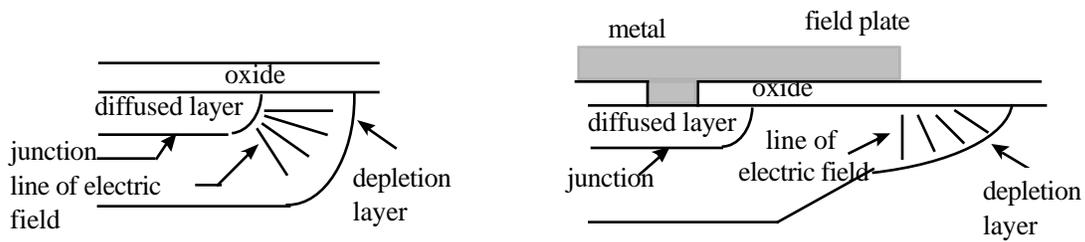


Figure 4.5 Field plate

Isolation

Electric isolation is a key requirement for monolithic PICs. There are basically three isolation methods used in PICs: self-isolation, junction isolation and dielectric isolation.

In self-isolation, the separation of low voltage and high voltage components is achieved by layout of the circuit and the nature of the bias. CMOS technology itself is an example of self-isolation, as shown in Figure 4.6. Because the P substrate is grounded, so all body diodes are reverse biased, which provides the isolation needed. A high voltage region can exist in this technology if the high field region is restricted to a closed-loop region.

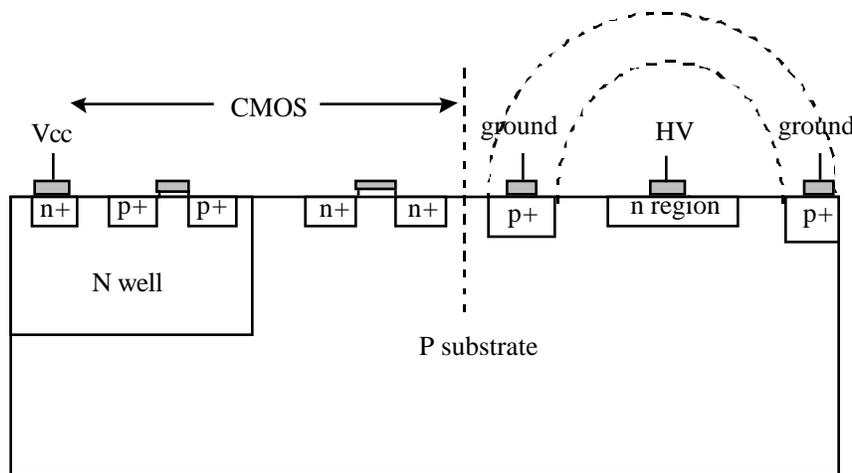


Figure 4.6 Self-isolation

Junction isolation uses designated layer of reverse biased junction for isolation, it's cost is higher than that of the self-isolation, but comparable with standard bipolar process. Figure 4.7 shows the junction isolation technique.

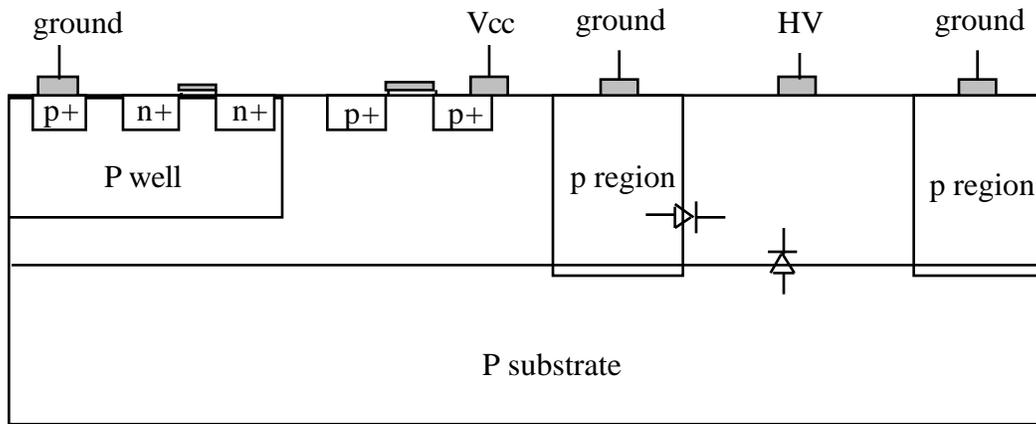


Figure 4.7 Junction isolation

Dielectric isolation uses a dielectric layer for isolation, e.g. SiO_2 , Figure 4.8 shows the dielectric isolation. SOI (silicon on insulator) process is also based on this technique.

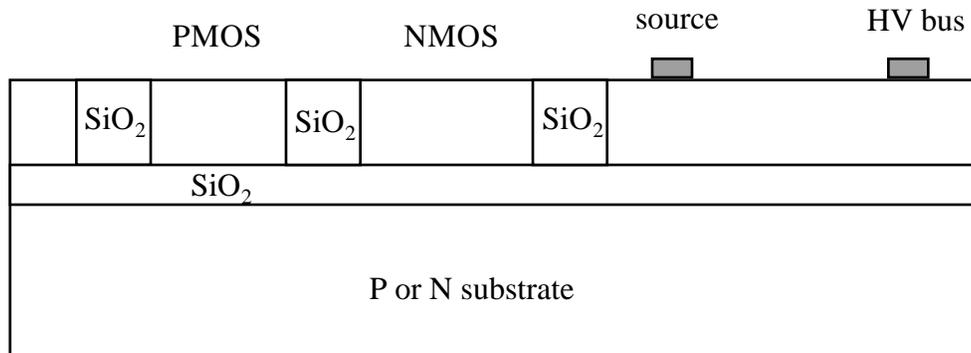


Figure 4.8 Dielectric isolation

Traditionally, bipolar junction transistor and lateral DMOS (LDMOS) have been the dominant power devices in PIC process. With the development in power devices, there are emerging devices such as lateral IGBT and lateral MCT, which seem to be good candidates for PIC applications. In Chapter 5, several of these new lateral devices are discussed with an emphasis on their static and dynamic performance. Numerical device simulators, e.g. Silvaco softwares [12], are used to compare the performance of different devices.

Chapter 5

CMOS Compatible, Integratable Lateral Power Devices

5.1 Lateral IGBT

In this chapter, several novel CMOS compatible lateral power devices are discussed. In the past, LDMOS is the most frequently used power device in PIC. The major limitation of the LDMOS is its relatively high specific on-resistance due to the majority-carrier conduction mechanism. Lateral IGBT and lateral MCT are proposed to be used in PICs because they can handle higher currents than the LDMOS. This could result in smaller and cheaper PIC chips for a given application. Figure 5.1 shows the structure of an N-channel lateral IGBT (LIGBT). For a 600-V LIGBT, it typically has an n⁻ epitaxial layer of 7 μm thick, and a drift region length of about 50 μm. RESURF technology is used to achieve this breakdown voltage. All other devices discussed in this chapter have similar drift region parameters. There is no substrate contact in these devices, and the substrate is modeled as floating in the simulations performed.

The structure of the LIGBT is similar to that of a LDMOS, the gate is formed by double diffusion and has a channel length of 2 μm. The difference is that at the anode, a p⁺ diffusion ohmic contact is used for the LIGBT instead of an n⁺ diffusion ohmic contact for the LDMOS. Also an N⁺ buffer layer is added at the anode for the LIGBT, and a p⁺ sinker is added at the cathode, whose purpose will be explained later.

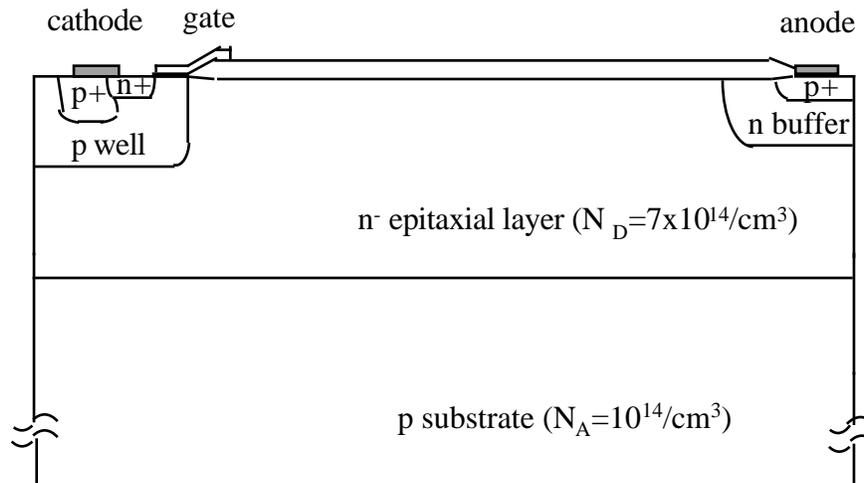


Figure 5.1 Structure of the LIGBT

In the LIGBT, a p-n junction is used to inject minority carriers into the drift region and thereby modulates its conductivity. This results in devices with specific on-resistance that is lower by about a factor of 5 to 10 than that of LDMOS for a similar device size. The degree of on-resistance lowering depends on the amount of injected minority carriers and thus the type of injector.

A positive voltage is applied to the p⁺ anode with respect to the cathode during its normal state of operation. With a gate to cathode voltage large enough, a low resistive N channel is created and electrons flow from the cathode towards the p⁺ anode contact via the drift region. When the forward voltage across the p⁺ anode/n⁺ buffer region exceeds the built-in potential of this junction, minority carriers are injected into the drift region, the

amount of holes injected into the drift region increases with the gate voltage. As the anode forward bias increases, more voltage appears across the inversion channel and the electron current increases to compensate for the injected hole concentration which then exceeds the

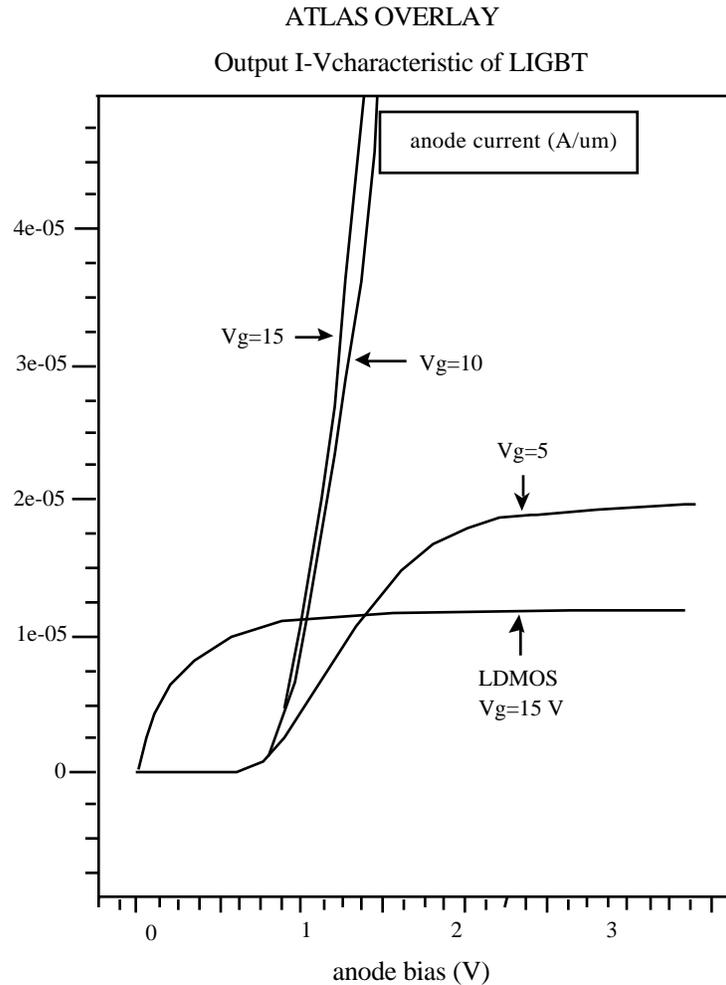


Figure 5.2 Output I-V characteristic of the LIGBT

background doping concentration of the n^- drift region. The holes also flow towards the substrate and the P-well region. The presence of the n^+ buffer region around the anode decreases the injection efficiency of the anode. The function of the n^+ buffer layer is to prevent punch through breakdown between the anode and the substrate. The injection efficiency of the LIGBT can be improved by using an n^+ buried layer instead of the n^+ buffer layer. A typical forward I-V characteristics of LIGBT is shown in Figure 5.2, based on two-dimensional simulations. Its output characteristics exhibit a diode drop before turn-on, this produces an additional nonlinearity in the current-voltage characteristics. However, in switching applications, this does not pose a limitation except for setting a lower limit to the voltage drop across the device in the on-state. Forward I-V characteristic of LIGBT in terms of current density is shown in Figure 5.3. Current flow lines in the forward biased LIGBT is shown in Figure 5.4.

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I-V characteristic of LIGBT

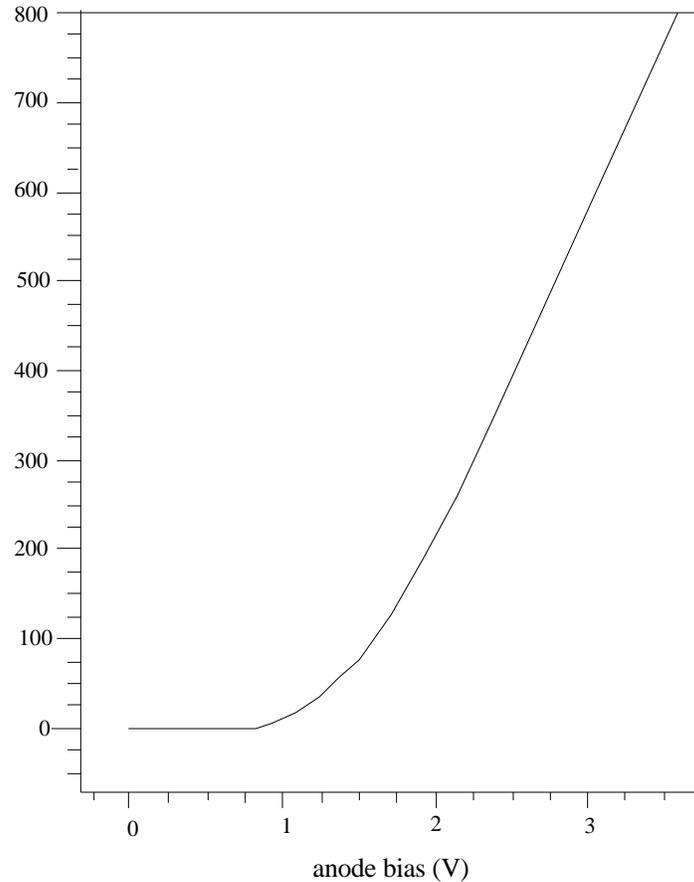


Figure 5.3 Forward I-V characteristic of the LIGBT

Figure 5.4 Current flow lines in the forward biased LIGBT(tif,13K,light_c.tif)

When the gate to cathode voltage is reduced to zero, the device is switched from its on state to off state, the current will fall to a fraction of the steady state value due to the cut-off of the electron current. This will be followed by a slow decay of the anode current over a long period of time. In the second phase, the carriers are removed mainly by electron-hole recombination as there is no more efficient way to extract the minority carriers from the drift region. Turn-off time therefore depends on the lifetime of the minority carrier.

Breakdown characteristic of LIGBT

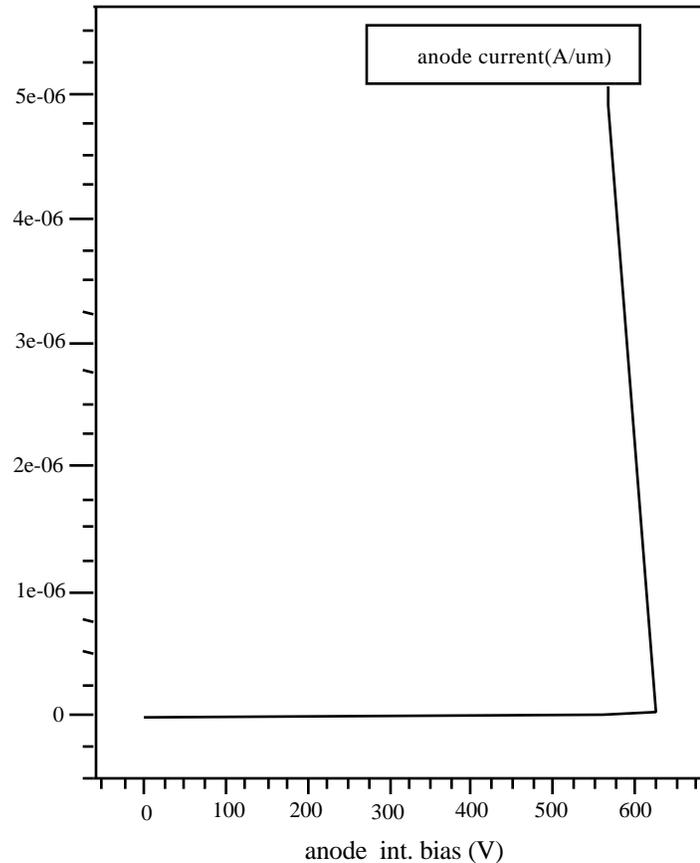
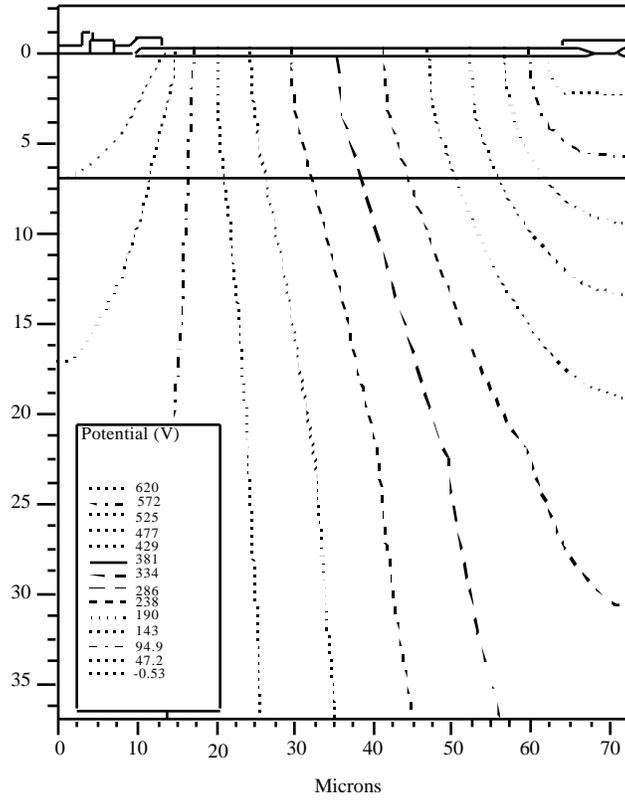


Figure 5.5 Breakdown characteristic of the LIGBT

The LIGBT uses RESURF principle and achieves a breakdown voltage of 640 V. The breakdown characteristic and breakdown structure are shown in Figure 5.5 and Figure 5.6. These results are also obtained via two dimensional numerical simulations. It is seen that the peak electrical field is at the P-well junction. For an optimally designed drift region, the breakdown should occur at the p substrate–n⁻ epitaxial junction. If the epi-layer's charge is not optimized, the breakdown may occur at the drain because of the depletion of the epitaxial layer, or may occur at the P-well because of field crowding at the P-well. Besides the avalanche breakdown behavior determined by RESURF principle, there are other breakdown mechanisms in lateral power devices. Because of short channels, thin epitaxial layers and the inclusion of gate oxide, punch through breakdown

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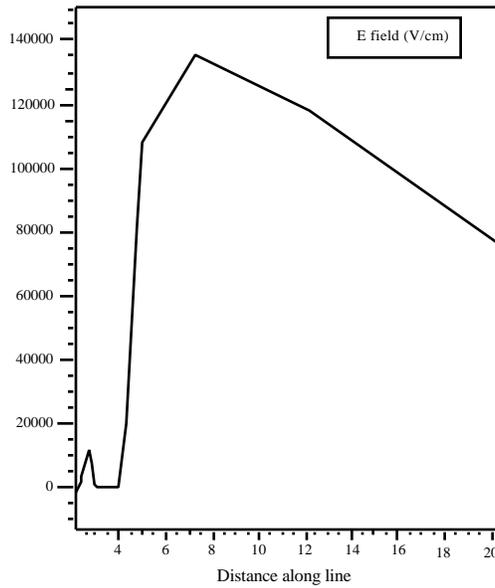
Potential in breakdown structure of LIGBT



(a)

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E field along y axis in breakdown structure of LIGBT



(b)

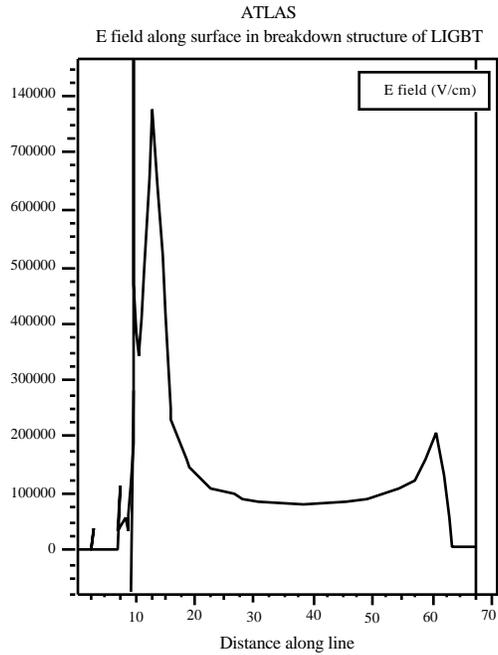


Figure 5.6 Breakdown structure of LIGBT (a) potential (b) electrical field along y axis (c) electrical field along surface

and gate oxide breakdown also become important in lateral MOS controlled high voltage devices. Punch through breakdown occurs when the depletion region of the P-well–n⁺ epitaxial junction reaches the depletion region of the n⁺ cathode and P-well junction, this punch-through breakdown voltage depends on the peak concentration of the P-well, the concentration of the drift region and the length of the channel region. The punch-through breakdown voltage can be increased by using a longer channel or increasing the P-well concentration. N⁺ buffer layer used here is also to prevent vertical punch-through which occurs when the depletion region of the substrate–n⁺ epitaxial junction reaches the drain contact. It also reduces the effective base width of the lateral p-n-p transistor. Gate oxide breakdown is more likely to happen in process which uses a thick epitaxial layer. In RESURF technology, the avalanche breakdown at the surface is usually avoided because of the interaction between the vertical and horizontal depletion regions. The breakdown of the gate oxide depends on the thickness and doping concentration of the epitaxial layer, doping concentration of the substrate and the P-well, as well as the length of the gate oxide extension into the drift region. As a design rule, these values are chosen in such a way that the drift region near the P-well pinches off before the peak electric field under the gate oxide exceeds its dielectric strength. The LIGBT structure shown in Figure 5.1 guarantees these breakdowns don't happen.

Turn-off of the LIGBT is simulated using the Silvaco's Atlas simulator in mixed-mode simulation. The circuit used to simulate turn-off of all the devices in this chapter is shown in Figure 5.7, all the devices use a lifetime of 1 μs for both electrons and holes. Turn-off of the LIGBT at 40 A/cm², 300 V with an inductive load is shown in Figure 5.8. The injection of minority carriers in the LIGBT results in increased turn-off delay than LDMOS due to storage-time effect. Turn-off speed is determined by the recombination of minority carriers in the conductivity-modulated region and is in the range of 1-3 μs. Improvement in the turn-off time of the LIGBT can be achieved by incorporating a shorting n⁺ diffusion at the anode to create a so called shorted-anode structure. The addition of this shorting diffusion results in more efficient removal of electrons thereby decreasing the turn-

off time. Shorted anode devices exhibit output characteristics with several distinct regimes. Namely, DMOS, bipolar and thyristor-like current-voltage characteristics. It typically has a larger on-resistance than pure LIGBT and the reverse blocking capability of the anode is also lost because of the short. If a Schottky diode is used to inject minority carriers, since the Schottky barrier supplies a limited number of minority carriers, it does not result in significant storage time, the resulting device therefore demonstrates a higher speed but also higher on-resistance.

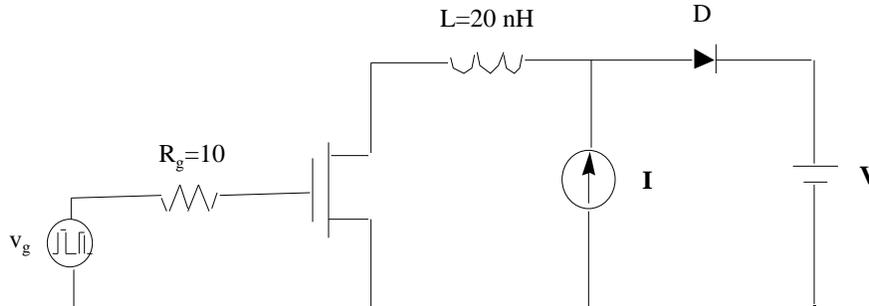


Figure 5.7 Circuit for turn-off simulation

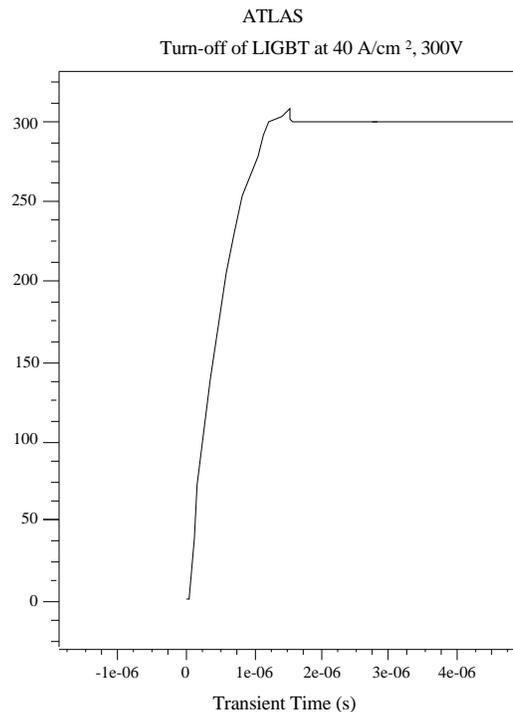


Figure 5.8 Turn-off of the LIGBT at 40 A/cm², 300 V

LIGBTs are susceptible to latch-up in the same way as discrete IGBTs because of an inherent parasitic p-n-p-n thyristor in the device. At high current level, voltage drop across the cathode-body junction is sufficient to turn the parasitic n-p-n transistor on. The collector current of the n-p-n transistor forms the base current for the lateral p-n-p transistor. When the sum of current gain of the two transistors reaches unity, latch-up occurs and gate control is lost. In RESUF device, a parasitic vertical p-n-p transistor is also formed by substrate, n⁻ layer and P-well which diverts some of the current and the latch-up threshold is increased. Other methods to suppress latch-up are aimed at lowering the gain of the n-p-n transistor by using a p⁺ buried layer and a deep p⁺ sinker[13]. In Figure 5.1's LIGBT, a deep p⁺ sinker is used. The N buffer layer can also be used to limit charge

injection by controlling the anode emitter efficiency. This increases both latch-up current and switching speed and provides a convenient way to trade off speed and forward voltage drop.

Latch-up can be either static, as discussed above, or dynamic, i.e., during switching. Dynamic latching occurs because of a rapid increase in the displacement current and the change in the ratio between vertical and lateral currents. Consequently, the rate at which the device is turned ‘on’ is critical to dynamic latch-up. Analysis of dynamic latch up can be found in [14].

In junction isolated PIC technologies, substrate leakage current due to injection of carriers to other neighboring devices is an important concern. Using shorted anode LIGBTs with buried layers and deep isolation diffusions provides a promising method to overcome this problem. An alternative approach is to use dielectric isolation to completely eliminate substrate current injection.

5.2 Lateral MCT

Lateral MCT (LMCT) is a MOS gated thyristor[15] which works in interrupted-gate-control mode, with the gate controls the turn-on or turn-off of the device. LMCT exhibits the highest current-carrying capability per unit area, or minimum on-resistance. A typical LMCT structure is shown in Figure 5.9.

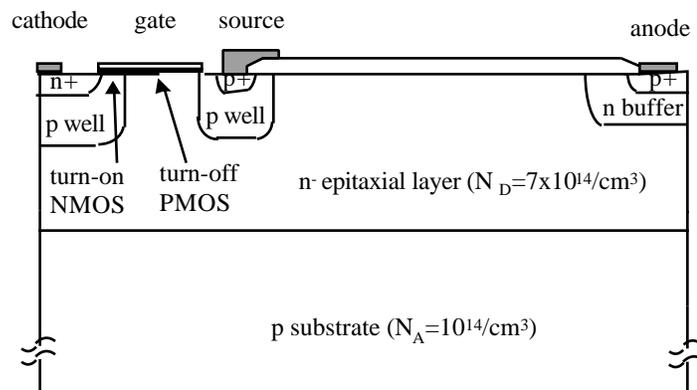


Figure 5.9 Structure of the LMCT

The LMCT has a four-layer p-n-p-n structure, with cathode connected to ground. The turn-on and turn-off gates are under the same gate electrode. Turn-on gate is an NMOS, formed by the double diffusion of the P-well and n^+ of the cathode, and the turn-off gate is a PMOS, formed between the P-well of the anode and P-well of the source. The channel created is determined by the bias voltage on the gate electrode. In the forward blocking or ‘off’ state, for a cathode voltage $V_K=0$, the gate voltage must be less than the threshold V_T of the turn-off FET. Positive anode voltages are then blocked by the source P-well– n junction exactly like that of an LIGBT. Leakage currents are limited to junction generated currents until the avalanche point. In the ‘on’ state, a positive voltage greater than 0.7 V is applied to the p^+ anode with respect to cathode, and gate to cathode voltage is increased to be greater than the threshold voltage of the turn-on NMOS. An N channel is created and electron current flows from cathode towards the drift region, this provides the base current for the PNP transistor. Carrier transport in the conductivity-modulated base regions is primarily by diffusion, as a result, hole transport to the cathode end of electrons is favored over diffusion to the p^- substrate. Regenerative operation occurs if the sum of the n-p-n, p-n-p’s common-base current gains exceeds one, then the thyristor is turned on and latches up. Like other thyristors, once firing has occurred the switch latches on and the gate terminal has no effect on the high current characteristic. The forward I-V characteristic

shown in Figure 5.10 is therefore only one curve independent of the applied gate voltage as long as the gate voltage is greater than the threshold voltage. The gate voltage does have an effect on the anode current I_T at which triggering takes place. The current flow lines in the forward biased LMCT is shown in Figure 5.11.

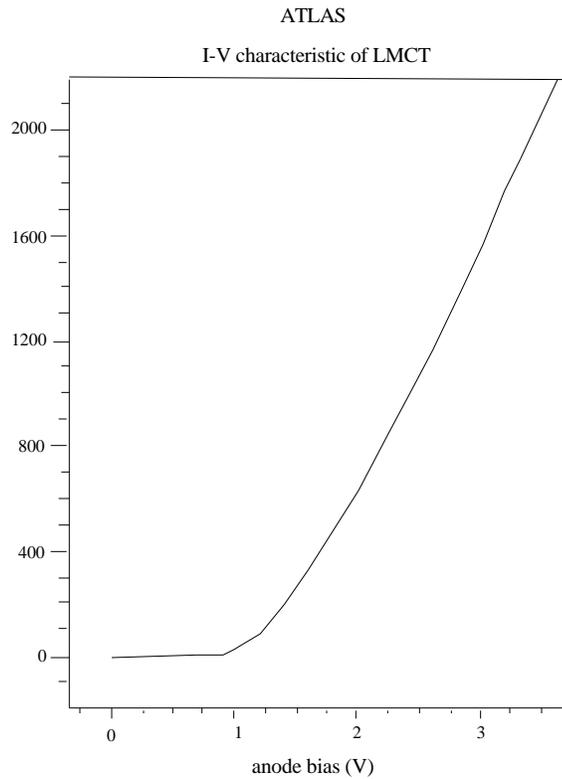


Figure 5.10 Forward I-V characteristic of the LMCT

Figure 5.11 Current flow in the forward biased LMCT(tif,13K,lmct_c.tif)

The p^+ source forms a p channel MOSFET with the base of the NPN transistor. A P-well is added at the source in addition to the p^+ contact to prevent premature breakdown at the source because of its small junction curvature. Breakdown characteristic of the LMCT is shown in Figure 5.12, with more than 600 V breakdown voltage. The potential contour at the breakdown point of the LMCT can be seen from Figure 5.13.

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Breakdown characteristic of LMCT

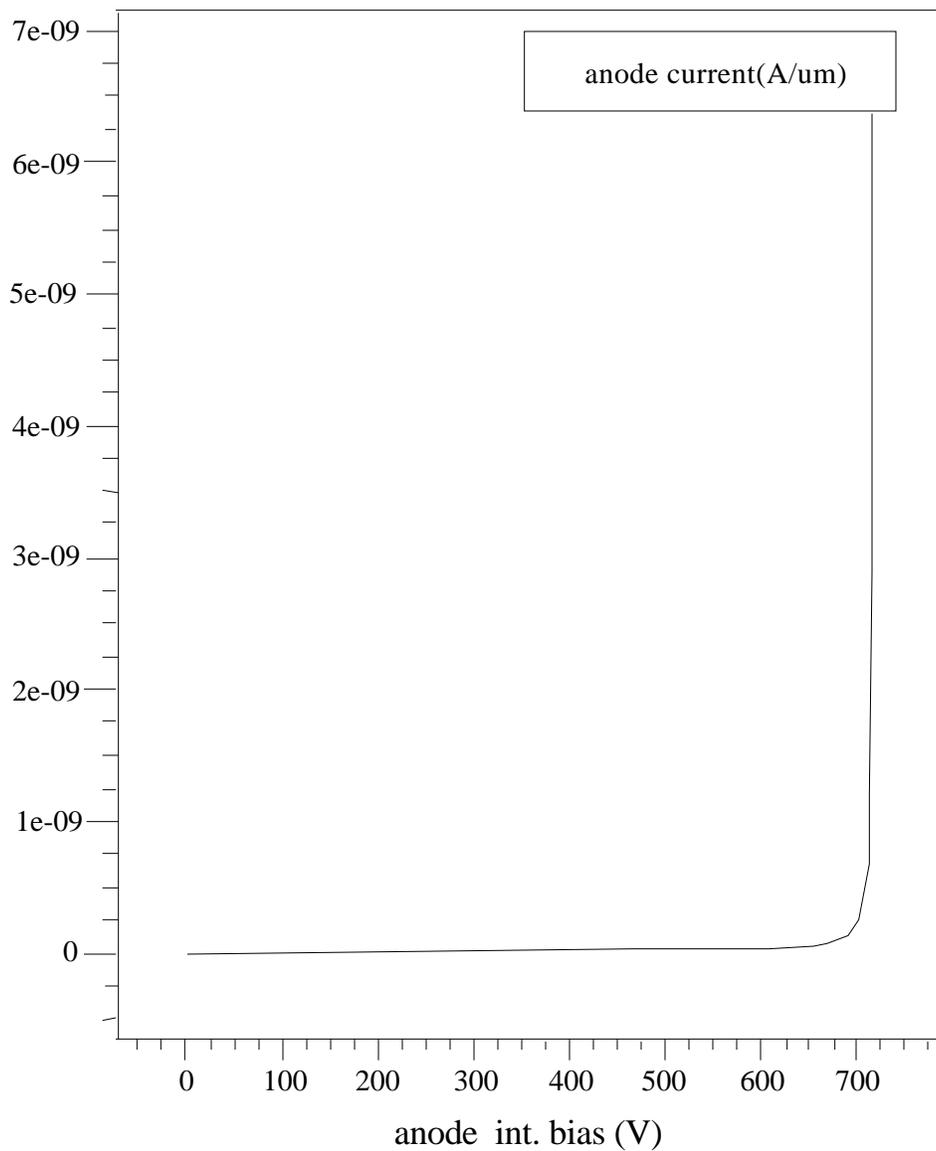


Figure 5.12 Breakdown characteristic of the LMCT

Figure 5.13 Potential contours in the breakdown structure of the LMCT(tif,15K,lmct_p.tif)

The key to accomplish turn-off function of the LMCT is to raise the thyristor's holding current which is normally dictated by p-base resistivity and the emitter short density, with low short density giving the lowest forward drop and holding current[16]. Two prime concerns in MOS-gated thyristors are the maximum turn-off current capability and the turn-off time. The turn-off capability is measured by the maximum controllable current, which is the maximum current in the on-state above which the device cannot be turned off. The current density that can be turned off depends on the density and effective resistance of the turn-off FET. Turn-off time is dictated internally by the recombination life-time,

primarily in the lightly doped region, device thickness and externally by the load and power supply slew rates, while turn-on speed and di/dt rating depend on the initial turn-on area which, in turn, depends on the density of the on-FET.

Turn-off of the LMCT is achieved by shorting the emitter junction to get the n-p-n out of saturation. When a negative voltage is applied to the gate relative to cathode, the N channel first disappears, and a P channel is formed that shorts the n-p-n's p base to the p⁺ source which is connected to ground., Since the cathode is also connected to ground, this shorts the emitter junction of the main thyristor. Holes are removed from the p-base region of the thyristor into the source region through the p-channel MOSFET. This is equivalent to reducing the base resistance R_b, which results in raising the holding current of the thyristor above the operating current level. Consequently, the forward bias on the emitter-base junction is reduced, breaking the regenerative action and causing the thyristor to turn off. Once the turn-off is initiated, the anode current decays in a finite time decided by the removal of minority carrier stored in the drift region.

The maximum anode current density that can be turned off is limited by the channel resistance of the p-channel MOSFET. The first order approximation of the maximum turn-off current I_{TGQM} for the MOS-gated thyristor is given by $I_{TGQM} = V_j / (\beta_{PNP} R_s)$, where V_j is the maximum voltage to maintain the n-emitter/p-base junction forward biased, β_{PNP} is the current gain of the pnp transistor, and R_s is the overall emitter shorting resistance. A smaller value of channel length reduces the on-resistance of the p-channel MOSFET, but the reduction in channel length causes an increase in the resistance of the JFET region between the p-base

Turn-off of LMCT at 40 A/cm², 300V

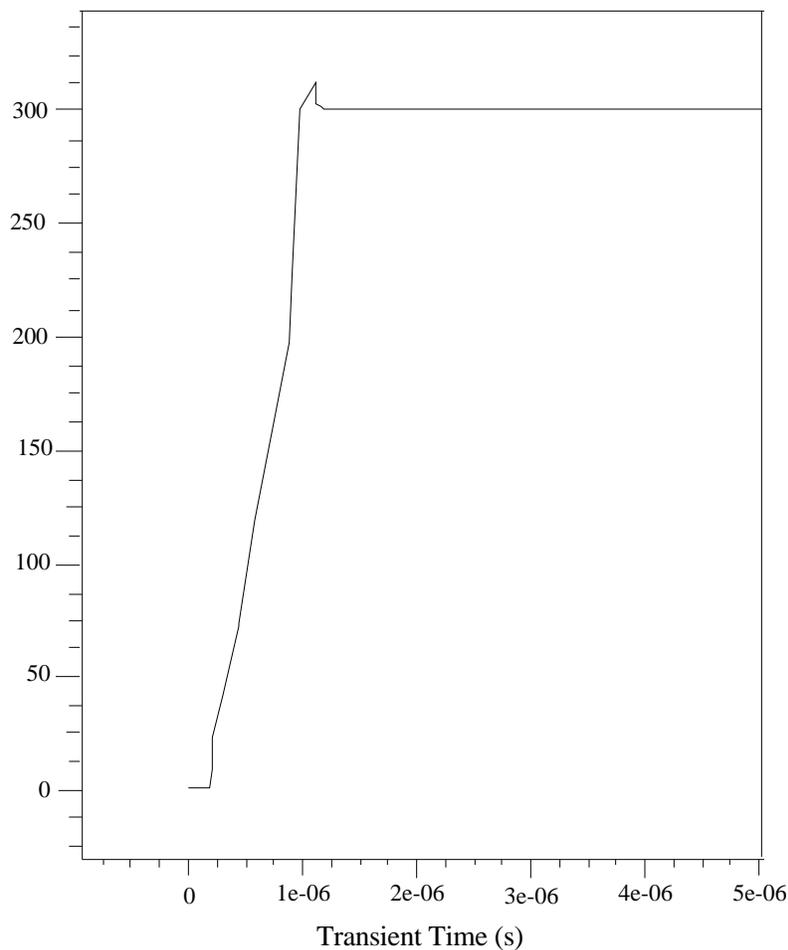


Figure 5.14 Turn-off of the LMCT at 40 A/cm², 300 V

and p⁺ source regions, through which the turn-on electron current flows into the N drift region during the turn-on process. The increased JFET region resistance can therefore adversely affect the turn-on behavior of the device. So a relatively long PMOS channel length is needed, this therefore affects the turn off capability. Larger anode currents can be turned off by decreasing the emitter width, because this reduces the amount of hole charge in the p base. Turn-off of the LMCT at 40 A/cm², 300 V is shown in Figure 5.14.

A number of factors limit the performance of the LMCT. First, the device has a parasitic lateral p-n-p transistor that is formed by the p⁺ anode, n⁻ base, and the p⁺ source. A large fraction of the injected anode hole current is collected by the parasitic p-n-p transistor without contributing to the thyristor action, which results in an increase in the on-state voltage drop and therefore reduces the device's efficiency. Removing the source to the left side of the cathode will help improve forward current carrying capability, but adversely affect the turn-off capability since this decreases the source's ability to collect holes. Secondly, during turn-off the hole current shunted through the PMOS channel via the base of the n-p-n transistor flows laterally under the n⁺ emitter, which keeps it on and further reduces turn-off capability. Finally, the use of conventional lateral PMOS transistor to turn the device off severely limits its maximum turn-off current capability because of the PMOS transistor's relatively higher channel resistance. A large-area PMOS transistor is needed in order to achieve high controllable current.

Improvement in the turn-off capability can also be achieved by using double-gate LMCTs (DG-LMCT). In the DG-LMCTs, another turn-off gate is used to improve the device's maximum turn-off current capability. In the forward conduction state, the second gate should not be turned 'on', so the DG-LMCT has a similar on-state performance as that of a single gate LMCT. During turn-off of the device, the second gate is turned on to help turn off larger anode current. Using a second gate during turn-off also makes the device turn off at a faster speed, hence reducing the turn-off loss. There are many kinds of double gate lateral MCTs[17], two of these are studied here.

5.3 Double Gate Lateral MCT (type 1)

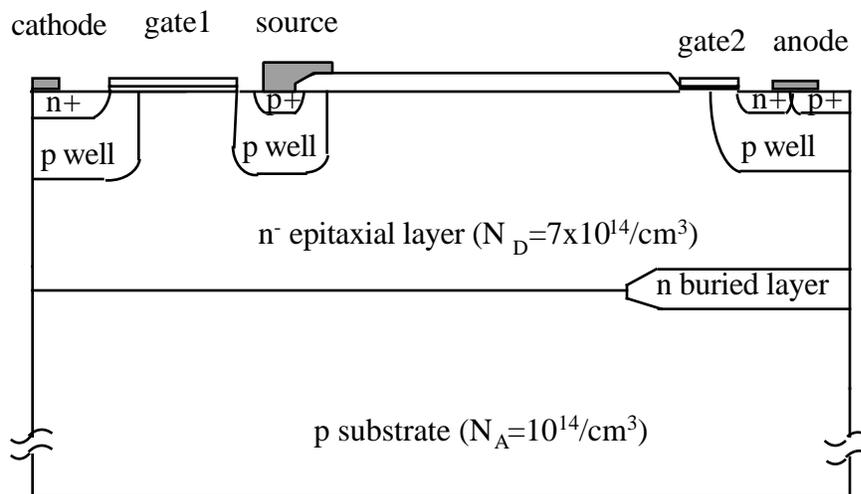


Figure 5.15 DG-LMCT (type 1)

One novel DG-LMCT structure is shown in Figure 5.15, in which gate 2 is added in addition to gate 1 to aid the turn-off process. In the structure of the DG-LMCT, a second gate is formed at the anode side by double diffusion of the P-well and the n⁺ diffusions, and

there is no N⁺ buffer layer in this structure. Turn-on of the device is the same as single gate LMCT when gate 2 is at the same potential as the anode. Turning off the device with only gate 1 is also similar to the turn-off in single gate LMCT. Single gate LMCT suffers from lower gate controllable current density because of the lower carrier mobility in the PMOS turn-off element. In the DG-LMCT (1), gate 2 can be used to assist turn-off. When its voltage is increased to 15 V higher than the anode voltage, an N channels is created under gate 2 which shorts the n⁺ of anode to the n⁻ drift region. Since the p⁺ and n⁺ of anode is shorted, this shorts the anode junction of the thyristor. By shorting both the emitter and anode junctions of the thyristor, the maximum turn-off current is increased. The structure under gate 2 is similar to the channel region of a LDMOS. The use of gate 2 control also improves the speed of the DG-LMCT, because it provides an efficient path for electron removal during turn-off.

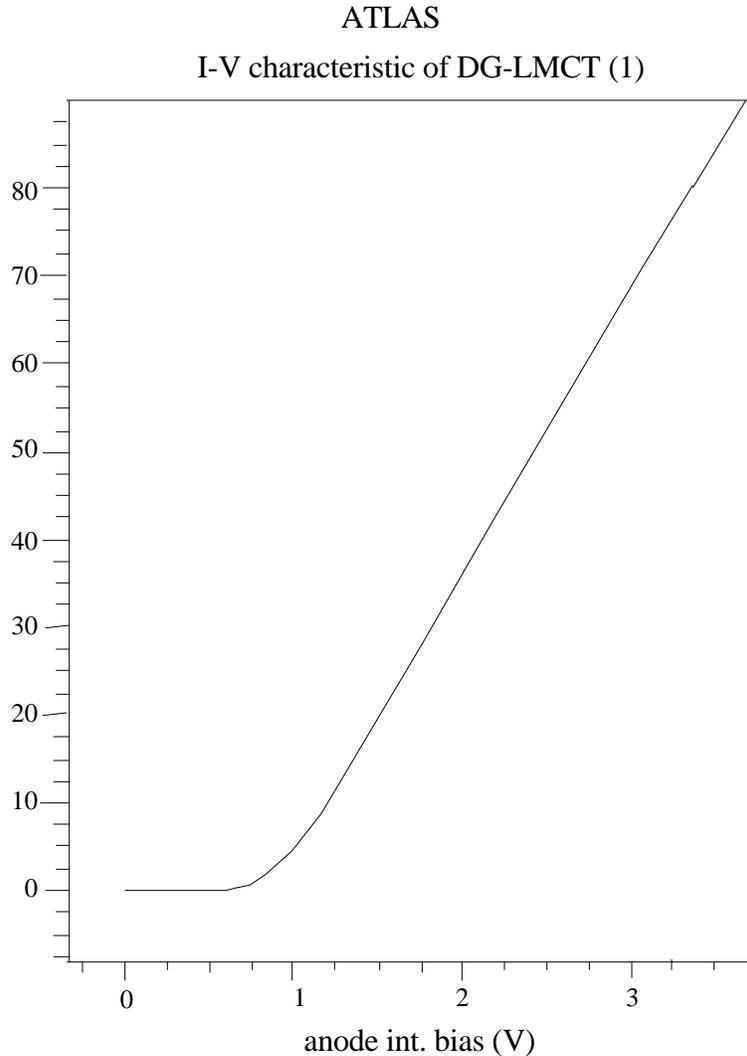


Figure 5.16 Forward I-V characteristic of the DG-LMCT (1)

Figure 5.17 Current flow in the DG-LMCT (1)(tif,14K,dg1_c.tif)

An n⁺ buried layer is used in the DG-LMCT (1) to prevent vertical punch through which occurs when the depletion region of the P-well-n⁻ epitaxial junction reaches the

depletion region of the substrate– n^- epitaxial junction, since no N buffer can be used. This somehow reduces the minority carrier injection efficiency because a lot of injected holes will be collected by the n^+ buried layer. Like the LMCT, there are also parasitic vertical p-n-p and lateral p-n-p transistors. There is also a parasitic vertical n-p-n formed by n^+ anode, P-well and the n^+ buried layer. All these factors affect the forward voltage drop of the device. Figure 5.16 shows the forward I-V characteristics of the DG-LMCT. Figure 5.17 shows the current flow in the DG-LMCT (1).

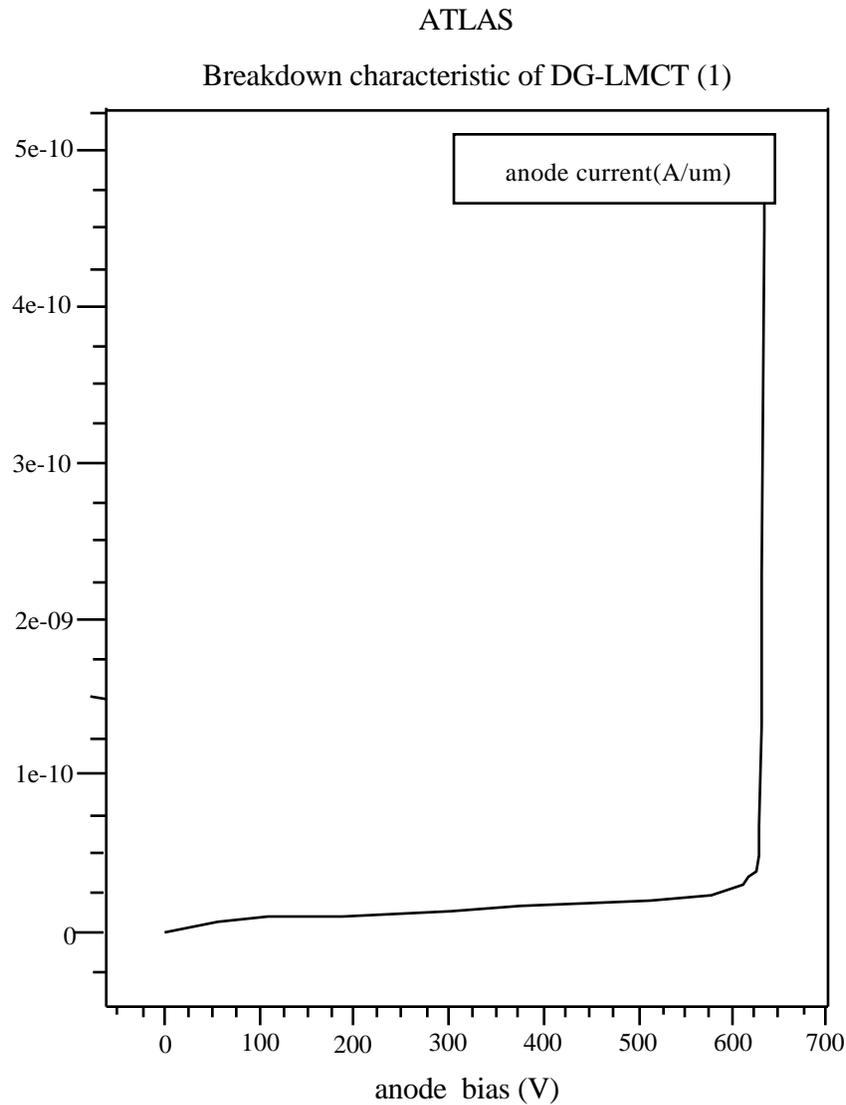


Figure 5.18 Breakdown characteristic of the DG-LMCT (1)

Breakdown characteristic of the device is shown in Figure 5.18, and the potential in the breakdown structure is shown in Figure 5.19. Turn-off speed with only gate 1 used is similar to that of single gate LMCT. Turn off with both gate 1 and gate 2 is faster. Simulation of the DG-LMCT (1) turning-off at 40 A/cm², 300 V is shown in Figure 5.20.

Figure 5.19 Potential in the breakdown structure of the DG-LMCT (1)(tif,16K,dg1_p.tif)

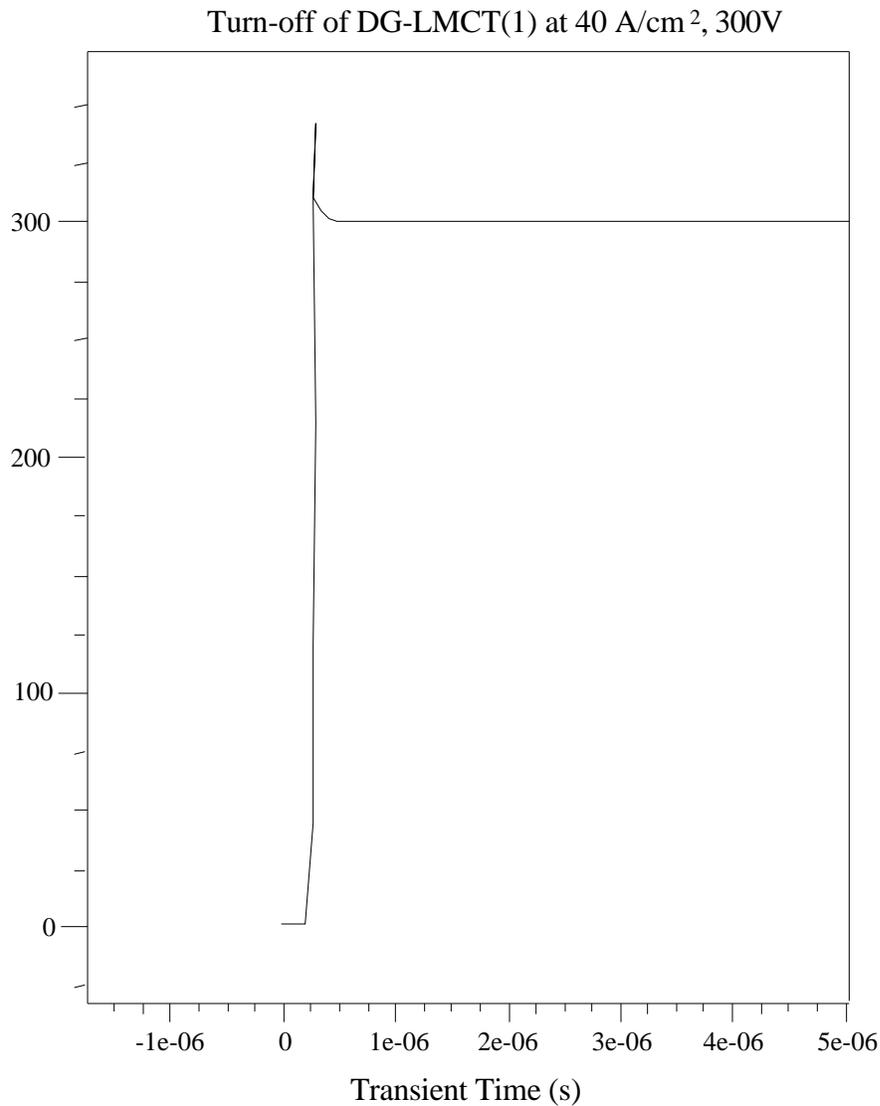


Figure 5.20 Turn-off of the DG-LMCT (1) at 40 A/cm², 300 V with both gates

5.4 Double Gate Lateral MCT (type 2)

Another type of DG-LMCT structure is shown in Figure 5.21. A floating metal (emitter) connecting the anode of the thyristor and the drain layer of a p channel MOSFET is formed in the N buffer region. The gate of the p channel MOSFET is the second gate that can be used to help turn off the device. The operation of the device is similar to type-1 DG-LMCT. Turn-on is achieved by a positive voltage on gate 1 with gate 2 and anode at the same potential. Turn-off is achieved by shorting both the emitter junction and the anode junction of the thyristor, with the anode junction shorting performed by turning on the PMOS at the anode with a negative 15 V voltage applied to gate 2 relative to the anode. Since a PMOS is used instead of a LDMOS, a n⁺ buffer is used instead of a n⁺ buried layer, the forward I-V characteristic is therefore improved. The I-V curve is shown in Figure 5.22. The current flow in the DG-LMCT (2) is shown in Figure 5.23.

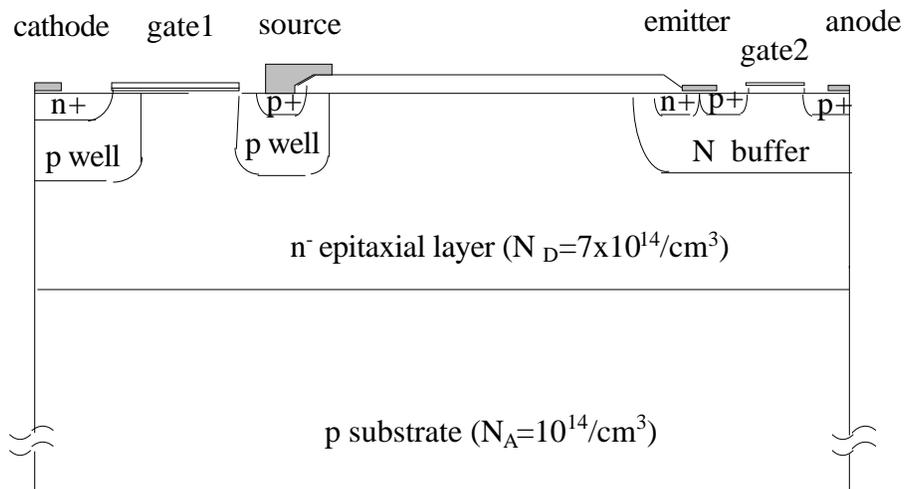


Figure 5.21 DG-LMCT (type 2)

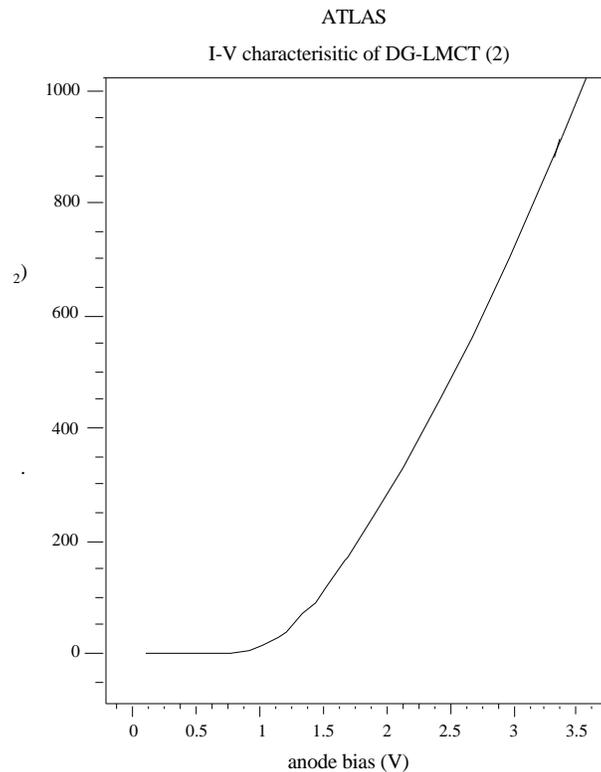


Figure 5.22 Forward I-V characteristic of the DG-LMCT (2)

Figure 5.23 Current flow in the DG-LMCT (2)(tif,13K,dg2_c.tif)

Breakdown characteristic is shown in Figure 5.24 with a breakdown voltage of 600 V. The potential contour in the breakdown structure is shown in Figure 5.25. Turn-off of the device at 40 A/cm², 300 V with both gates is shown in Figure 5.26.

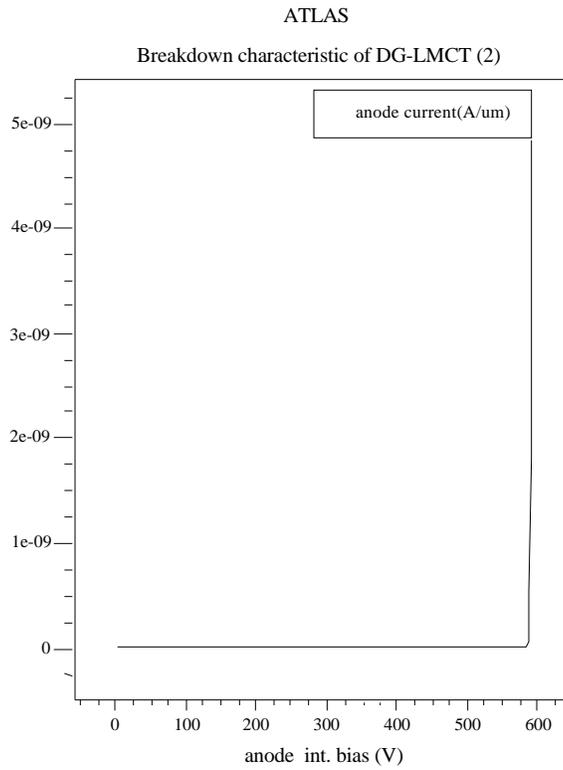


Figure 5.24 Breakdown characteristic of the DG-LMCT (2)

Figure 5.25 Potential in breakdown structure of the DG-LMCT (2)(tif,17K,dg2_p.tif)

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Turn-off of DG-LMCT(2) at 40 A/cm², 300V

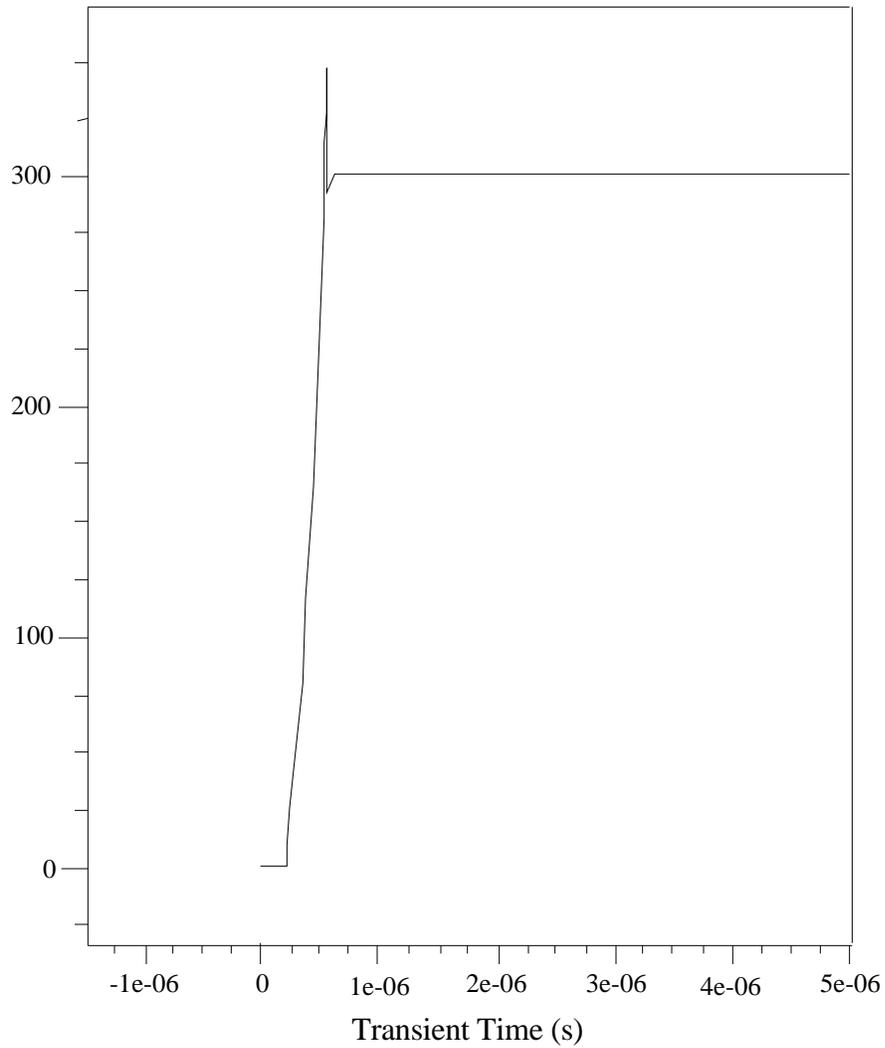


Figure 5.26 Turn-off of the DG-LMCT (2) at 40 A/cm², 300 V with both gates

5.5 Conclusions

The performance of these novel lateral power devices can be compared from the main characteristics of the devices.

A: Forward I-V Characteristics

ATLAS

Forward I-V characteristic

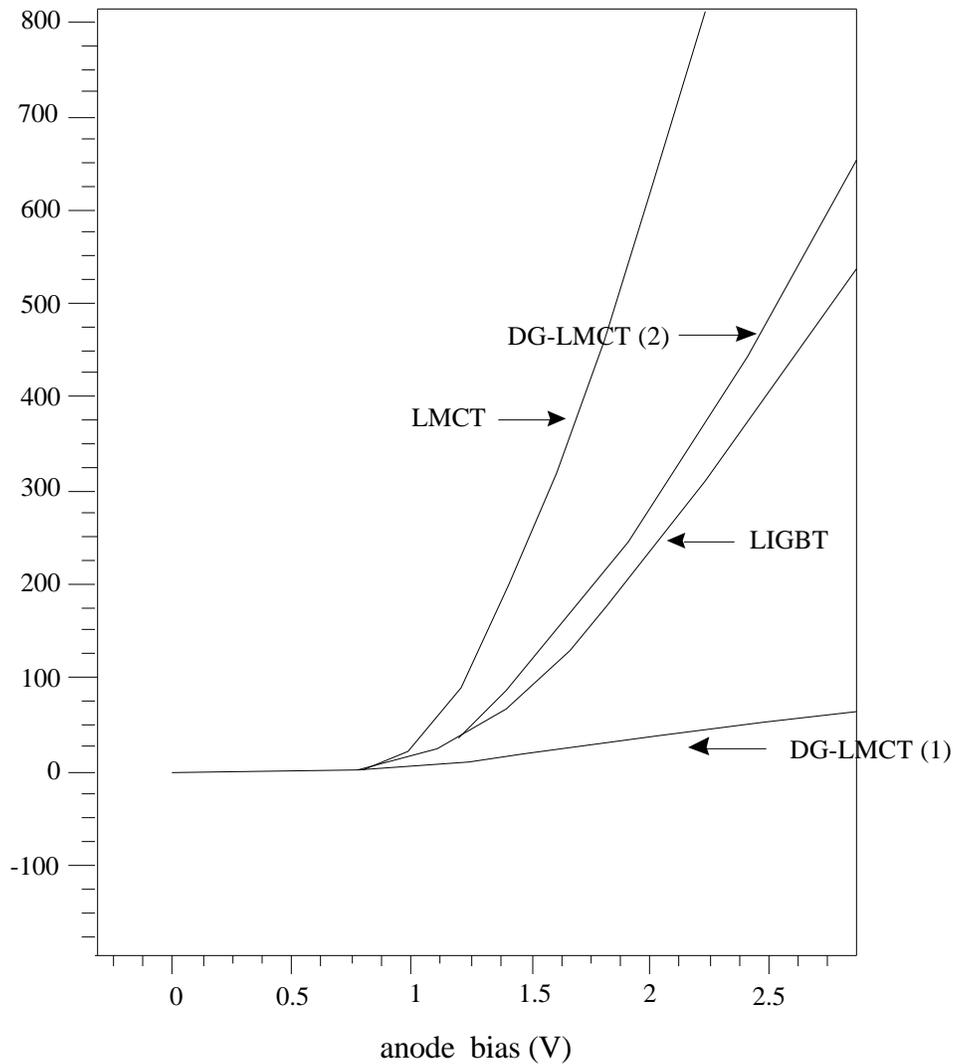


Figure 5.27 Forward I-V characteristics of the four devices

The forward I-V characteristic of the devices are shown in Figure 5.27. LMCTs have the highest current-carrying capability per unit area due to the positive feedback which is an inherent part of four-layer latching devices and the conductivity modulation of lightly doped regions that occurs in them because of minority-carrier injection. The on-state of a LMCT is approximately a 50-fold improvement on the standard lateral DMOS device and offers consequent savings in size and parasitic capacitance without sacrifice of current capacity, voltage drop, or insulated-gate control. Despite the parasitic p-n-p transistor in single gate LMCT which reduces the device's efficiency, it still has the highest current density among the four devices. The type-2 DG-LMCT has the second highest current density. The current density of type-1 DG-LMCT is less than that of LIGBT, mainly because of the n^+ buried layer which decreases the injection efficiency of the device, while type-2 DG-LMCT doesn't need the buried layer, and can achieve a higher current density.

B: Breakdown Voltage

Breakdown characteristics of the four devices are shown in Figure 5.28, since RESURF principle is used, they all have a breakdown voltage greater than 600 V. Breakdown occurs at the drain, when the drift region is completely depleted, so the breakdown voltage depends mainly on the length of the drift region. Here the four device all have a drift region length of about 50 μm .

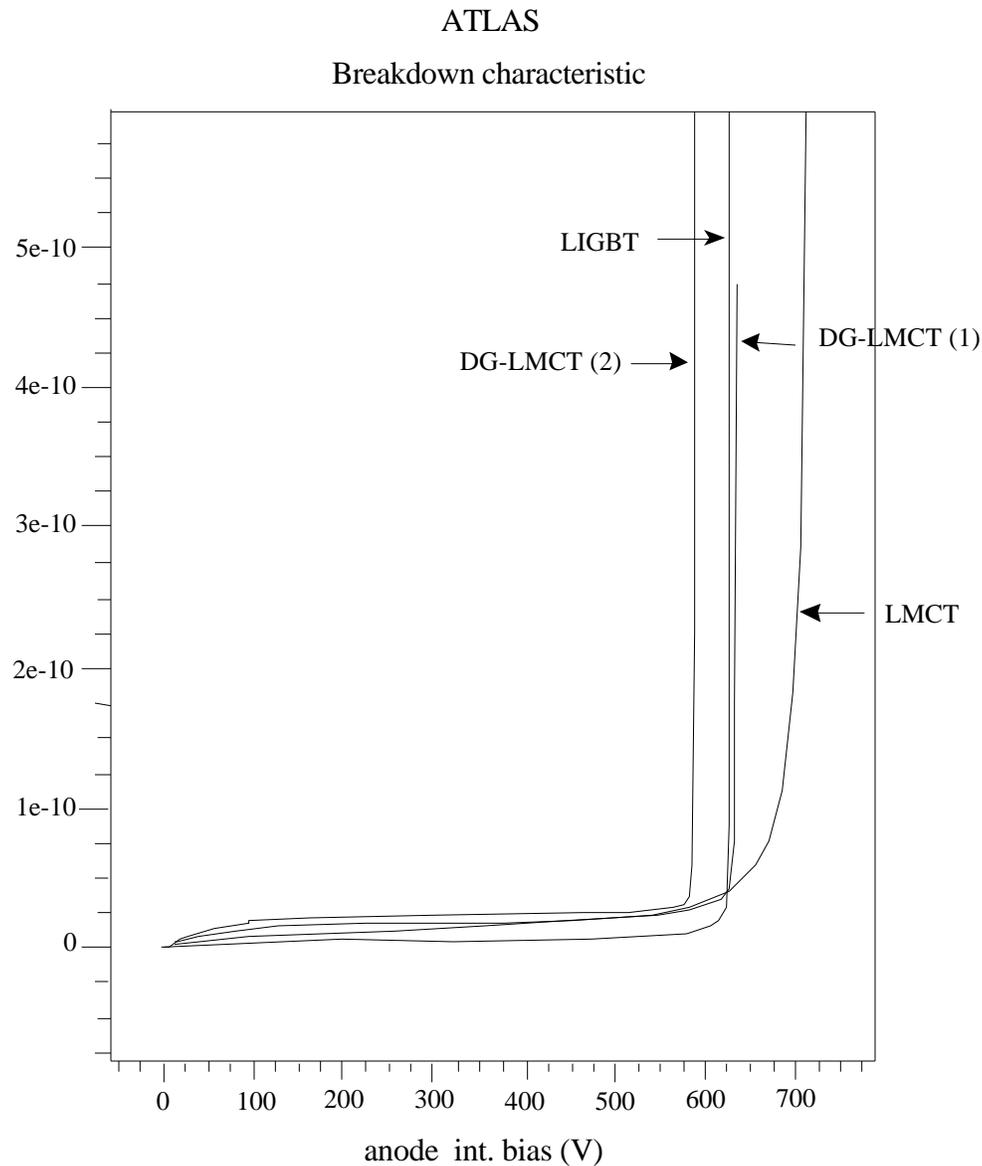


Figure 5.28 Breakdown characteristics of the four devices

C: Switching speed

Turn-off and turn-on of the four devices at 40 A/cm^2 , 300 V is shown in Figure 5.29. DG-LMCTs apparently have the highest switching speed.

ATLAS

Turn-off at 40 A/cm², 300V

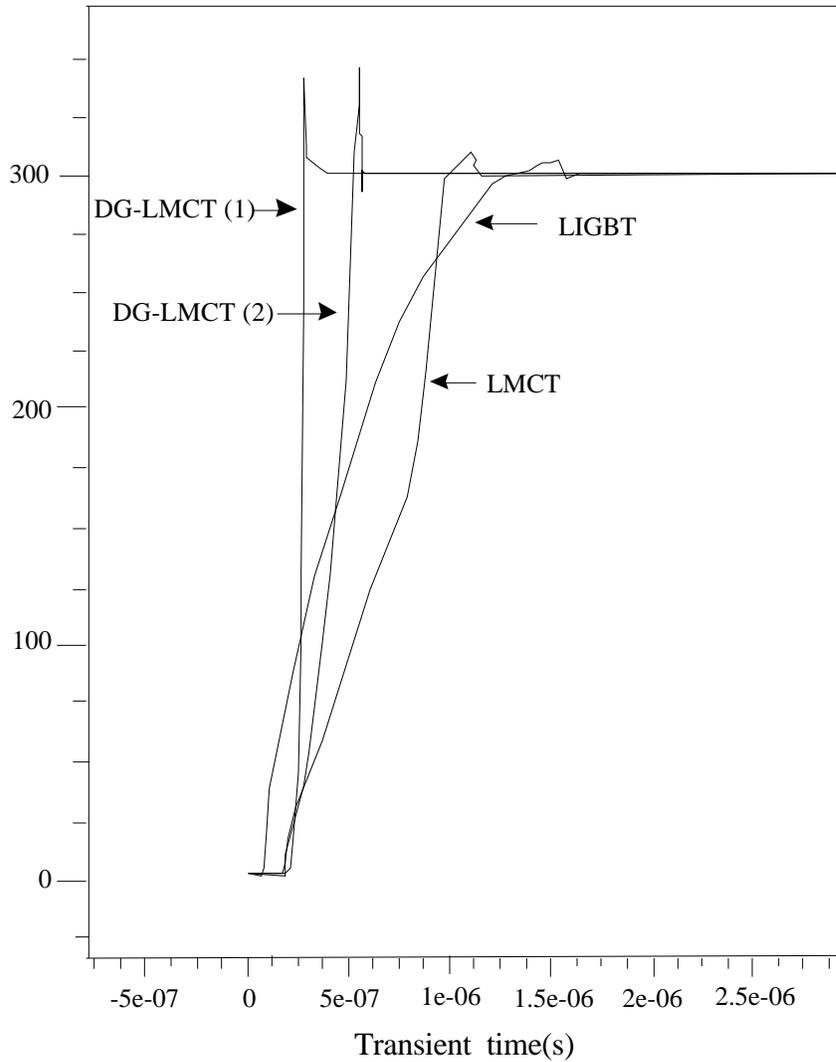


Figure 5.29 Turn-off of the four devices at 40 A/cm², 300 V

The anode current waveform during turn-off of these devices are shown in Figure 5.30, the DG-LMCT (1) has the fastest fall of anode current, with DG-LMCT (2) the second, LMCT the third, and LIGBT the slowest. Since the turn-off loss is the integral of anode voltage and anode current product, it can be seen that DG-LMCT (1) and DG-LMCT (2) has the smallest turn-off loss, which is a good feature for switch's operation.

ATLAS

Turn-off at 40 A/cm², 300V

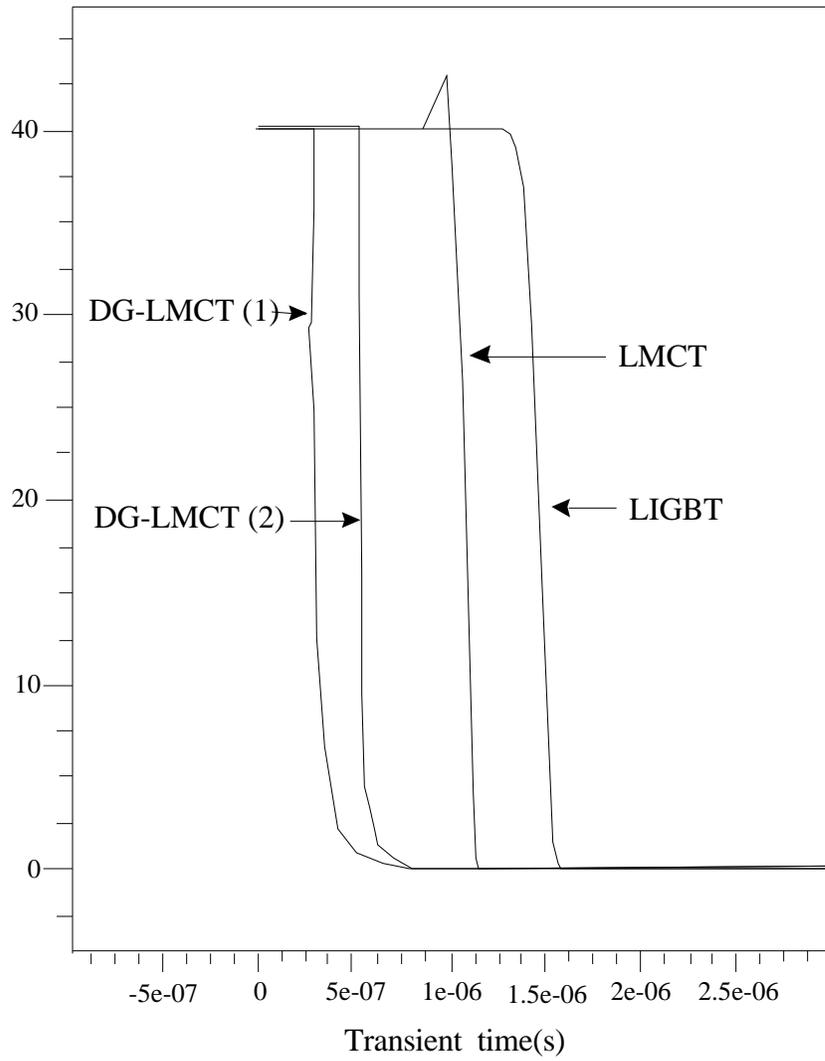


Figure 5.30 Anode current during turn-off

D: SOA(Safe Operating Area)

RBSOA of LIGBT, LMCT, DG-LMCT (1)

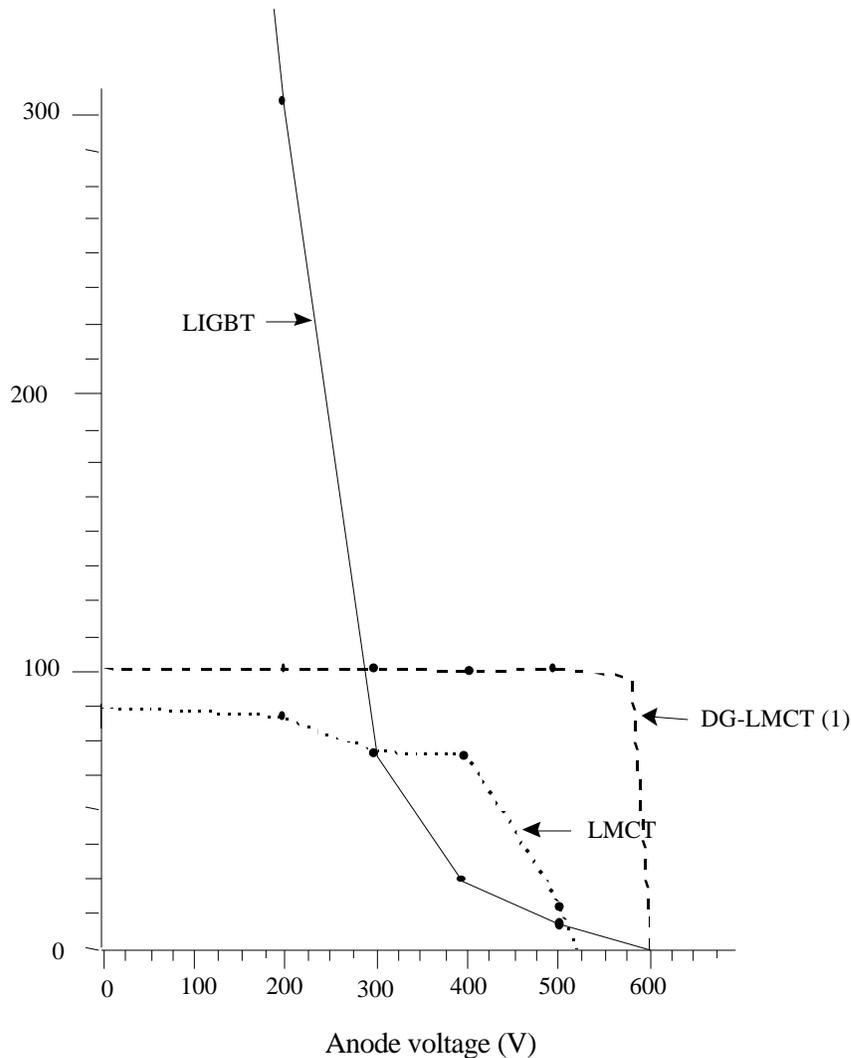


Figure 5.31 RBSOA of the LIGBT, LMCT

The Reverse Biased SOA (RBSOAs) of these devices are also compared and shown in Figure 5.31. Type-2 DG-LMCT has a similar RBSOA to type-1 DG-LMCT. Type-1 DG-LMCT has the largest RBSOA since when turn-off, it uses both a PMOS and a LDMOS for turn-off. Type-2 DG-LMCT has the second largest RBSOA, since it also uses double gate for turn-off, it has a larger RBSOA than that of the LMCT, but smaller than type-1 DG-LMCT since the turn-off gate2 uses a PMOS while type-1 uses a LDMOS. The disadvantage of double gate LMCT is that their gate 2 should be driven relative to the anode potential, which is normally a floating voltage point.

From the above comparison, it is seen that LIGBT is a good candidate for PIC, due to its large turn-off capability. LMCTs are also good candidates for future implementation, since they have a much higher current density. The maximum turn-off current depends on the device design. DG-LMCTs have both a good current density and a large RBSOA, and are therefore promising devices for PIC's applications.

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Appendix A

MOSIS Scalable CMOS Design Rules

Well (CWN, CWP)	
1.1 Minimum width	10
1.2 Minimum spacing between wells at different potential	9
1.3 Minimum spacing between wells of different type	0 or 6
1.4 Minimum spacing between wells of different type	0
Active (CAA)	
2.1 Minimum width	3
2.2 Minimum spacing	3
2.3 Source/drain active to well edge	5
2.4 Substrate/well contact active to well edge	3
2.5 Minimum spacing between active of different implant	0 or 4
Poly(CPG)	
3.1 Minimum width	2
3.2 Minimum spacing	2
3.3 Minimum gate extension of active	2
3.4 Minimum active extension of poly	3
3.5 Minimum field poly to active	1
Select (CSN, CSP)	
4.1 Minimum select spacing to channel of transistor to ensure adequate source/drain width	3
4.2 Minimum select overlap of active	2
4.3 Minimum select overlap of contact	1
4.4 Minimum select width and spacing (Note: P-select and N-select may be coincident, but must not overlap)	2
Simple Contact to Poly (CCP)	
5.1.a Exact contact size	2x2
5.2.a Minimum poly overlap	1.5
5.3.a Minimum contact spacing	2
Alternative Contact to Poly (CCP)	
5.1.b Exact contact size	2 x 2
5.2.b Minimum poly overlap	1
5.3.b Minimum contact spacing	2
5.4.b Minimum spacing to other poly	4
5.5.b Minimum spacing to active (one contact)	2
5.6.b Minimum spacing to active (many contacts)	3
Simple Contact to Active (CCA)	
6.1.a Exact contact size	2 x 2
6.2.a Minimum active overlap	1.5
6.3.a Minimum contact spacing	2
6.4.a Minimum spacing to gate of transistor	2
Alternative Contact to Active (CCA)	
6.1.b Exact contact size	2 x 2
6.2.b Minimum active overlap	1

6.3.b	Minimum contact spacing	2
6.4.b	Minimum spacing to diffusion active	5
6.5.b	Minimum spacing to gate of transistor	2
6.6.b	Minimum spacing to field poly (one contact)	2
6.7.b	Minimum spacing to field poly (many contacts)	3
6.8.b	Minimum spacing to poly contact	4
Metal (CMF)		
7.1	Minimum width	3
7.2.a	Minimum spacing	3
7.2.b	Minimum tight metal spacing	2
7.3	Minimum overlap of poly contact	1
7.4	Minimum overlap of active contact	1
Vial (CVA)		
8.1	Exact size	2 x 2
8.2	Minimum overlap by metal	3
8.3	Minimum spacing to contact	1
8.4	Minimum spacing to poly or active edge	2
8.5	Minimum spacing to poly or active edge	2
Metals (CMS)		
9.1	Minimum width	3
9.2.a	Minimum spacing	4
9.2.b	Minimum tight metal spacing	3
9.3	Minimum overlap of vial	1
Overglass (COG)		
10.1	Minimum bonding pad width	100 x 100
10.2	Minimum probe pad width	75 x 75
10.3	Minimum probe pad width	6
10.4	Minimum pad spacing to unrelated metals	30
10.5	Minimum pad spacing to unrelated metal, poly, electrode or active	15
Electrode for Capacitor (CEL - Analog Option)		
11.1	Minimum width	3
11.2	Minimum spacing	3
11.3	Minimum poly overlap	2
11.4	Minimum spacing to active or well edge	2
11.5	Minimum spacing to poly contact	3
Electrode for Transistor (CEL -Analog Option)		
12.1	Minimum width	2
12.2	Minimum spacing	3
12.3	Minimum spacing	2
12.4	Minimum spacing	1
12.5	Minimum spacing	2
12.6	Minimum spacing to poly or active contact	3
Electrode Contact (CCE -Analog Option)		
13.1	Exact contact size	2 x 2
13.2	Minimum contact spacing	2
13.3	Minimum electrode overlap (on capacitor)	3
13.4	Minimum electrode overlap (not on capacitor)	2
13.5	Minimum spacing to poly or active	3

Via2(CVS - Triple Metal Option)	
14.1 Exact size	2 x 2
14.2 Minimum spacing	3
14.3 Minimum overlap by metal2	1
14.4 Minimum spacing to via1	2
Metal3 (CMT - Triple Metal Option)	
15.1 Minimum width	6
15.2 Minimum spacing to metal3	4
15.3 Minimum overlap of via2	2
NPN Bipolar Transistor (CBA -Analog Option)	
16.1 All active contact	2 x 2
16.2 Minimum select overlap of emitter contact	3
16.3 Minimum pbase overlap of emitter select	2
16.4 Minimum spacing between emitter select and base select	4
16.5 Minimum pbase overlap of base select	2
16.6 Minimum select overlap of base contact	2
16.7 Minimum nwell overlap of pbase	6
16.8 Minimum spacing between pbase and collector active	4
16.9 Minimum active overlap of collector contact	2
16.10 Minimum nwell overlap of collector active	3
16.11 Minimum select overlap of collector active	2
Capacitor Well (CWC -Linear Capacitor Option)	
17.1 Minimum width	10
17.2 Minimum spacing	9
17.3 Minimum spacing to external active	5
17.4 Minimum overlap of active	3
Linear Capacitor (Linear Capacitor Option)	
18.1 Minimum width	3
18.2 Minimum poly extension of active	1
18.3 Minimum active overlap of poly	3
18.4 Minimum poly contact to active	2
18.5 Minimum active contact to poly	4
Buried Channel CCD (CCD -Analog Option)	
19.1 Minimum CCD channel active width	4
19.2 Minimum CCD channel active spacing	4
19.3 Minimum CCD implant overlap of channel active	2
19.4 Minimum outside contact to CCD implant	3
19.5 Minimum select overlap of electrode (or poly)	2
19.6 Minimum poly/electrode overlap within channel active	2

Appendix B

Input Deck for SILVACO Device Simulation

```
##### IV curve extraction #####

##### gate voltage = 5.0 #####
go atlas
MESH INFILE=light.str
comm Electrodes: #1=cathode #2=gate #3=anode

# set material models
material taun0=1e-6 taup0=1e-6 material=silicon
models BIP SURFMOB CCSMOB FERMI
impact selb

contact name=gate n.Poly
output jx.h jy.h jx.e jy.e flowlines
log outf=iv1.log master

# get initial solution
solve init
method newton trap
solve vstep=0.1 vfinal=1.0 name=gate
solve vstep=0.5 vfinal=5.0 name=gate

# Bias the drain solve vanode=0.1 vstep=0.1 vfinal=1 name=anode
solve vstep=0.2 vfinal=3 name=anode
##

go atlas

.begin
Vdc 5 0 300
I 0 4 71
Lanode 4 3 20e-9
dload 4 5 diode

RG 1 2 10

vg 2 0 15 pulse 15 0 0.0 0.05u 0.05u 20u 40us

aigt 3=anode 1=gate 0=cathode infile=on1.str width=1.36e6

.model diode D
.options m2ln relpot print rv=1e-6 loadsolutions
.load infile=on1.str
.nodeset v(5)=300 v(4)=1.4 v(3)=1.4 v(1)=15 v(2)=15

.log outfile=300V_71A_s
.tran 1ns 40us
#.save outfile=pdsave master=pd
.end
```

```
Models device=aigt BIP CCSMOB SURFMOB FERMI PRINT
contact device=aigt name=gate n.poly
material device=aigt material=silicon taun0=1e-6 taup0=1e-6
impact device=aigt selb
method cx.tol=1e-3 px.tol=1e-3 climit=1e7 dvmax=1e6
output jx.cond jy.cond flow jx.e jx.h jy.e jy.h
```

```
quit
```

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Wei Dong was born in 1970 in Beijing, China. She received a B.S. degree in Electronics Engineering from Fudan University, Shanghai, China, in 1992. She received a M.S. degree in Electronics Engineering from Fudan University, Shanghai, China, in 1995. After studying for two years at Virginia Polytechnic Institute and State University, Blacksburg, Virginia, she received a M.S. degree in Electrical Engineering in 1997. During the period of M.S. study at Virginia Polytechnic Institute and State University, she was a Graduate Research Assistant.