

High Density Cell Design For Ultra Low On-Resistance

Fully Characterized Avalanche Voltage and Current

Advanced Trench Process Technology

Improved Shoot-Through FOM

SO-8 Package Design

GENERAL DESCRIPTION

The CMT4953G provide the designer with the best combination of fast switching , ruggedized device design , low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial-industrial mount applications and suited for low voltage applications such as DC/DC converters.

APPLICATIONS

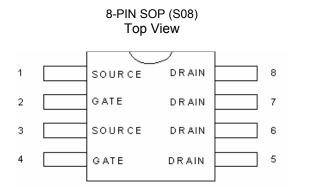
- Power Management in Notebook
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- ♦ LCD Display inverter

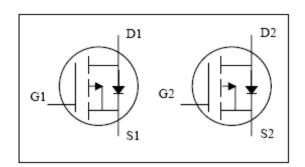
PIN CONFIGURATION

SYMBOL

FEATURES

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P-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT4953G	SOP-8

*Note: G : Suffix for Pb Free Product



ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain- Source Voltage		V _{DS}	-30	V
Gate- Source Voltage		V _{GS}	±20	V
Continuous Drain Current ¹	T _A =25℃	Ι _D	-4.5	А
Pulsed Drain Current ²			-23	A
Total Power Dissipation ¹	T _A =25℃	PD	2	W
Operating Junction Temperature Range			-55 to150	°C
Storage Temperature Range		T _{STG}	-55 to 150	°C
Linear Derating Factor			0.02	°C /W
Thermal Resistance Junction-ambient ¹ (Max)		Rthj-amb	62.5	°C/W



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_{\rm J}$ = 25 $^\circ\!{\rm C}$. (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
D		V _{GS} =-10V, I _D =-4.6A	-	-	55	m Ω
R _{DS(ON)}	Static Drain-Source On-Resistancem ²	V _{GS} =-4.5V, I _D =-3.6A	-	-	90	mΩ
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{D}=-250$ uA	-1	-	-2.5	V
9fs	Forward Transconductance ²	V _{DS} =-5V, I _D =-4.6A	-	5	-	S
I _{DSS}	Drain-Source Leakage Current (Tj=25 C)	V _{DS} =-24V, V _{GS} =0V	-	-	-1	uA
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V	-	-	±100	nA
Qg	Total Gate Charge ²	I _D =-4.6A	-	11.7	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-15V	-	2.1	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-10V	-	2.9	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-15V	-	9	-	ns
t _r	Rise Time	I _D =-1A	-	10	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω,V _{GS} =-10V	-	37	-	ns
t _f	Fall Time	R _D =15 Ω	-	23	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	582	-	pF
C _{oss}	Output Capacitance	V _{DS} =-15V	-	125	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	86	-	pF

Source-Drain Diode

	Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
V	SD	Forward On Voltage ²	I _S =-1.7A, V _{GS} =0V	-	-0.84	-1.2	V

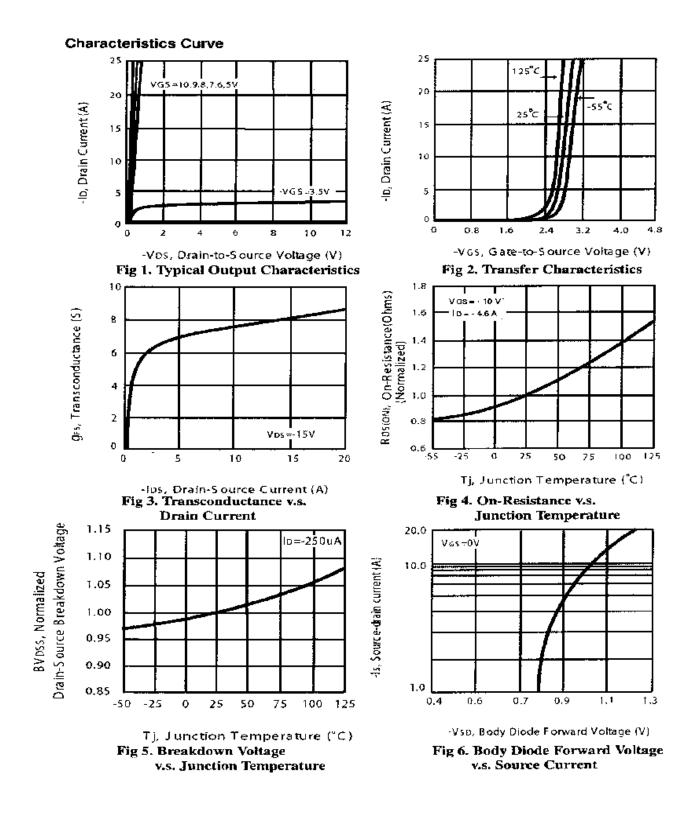
Notes:

1.Surface mounted on FR4 Board , $t{\leq}2\%$

2.Pulse width $\ \leq 300 \text{us}$, duty cycle $\ \leq 2\%.$



TYPICAL CHARACTERISTICS





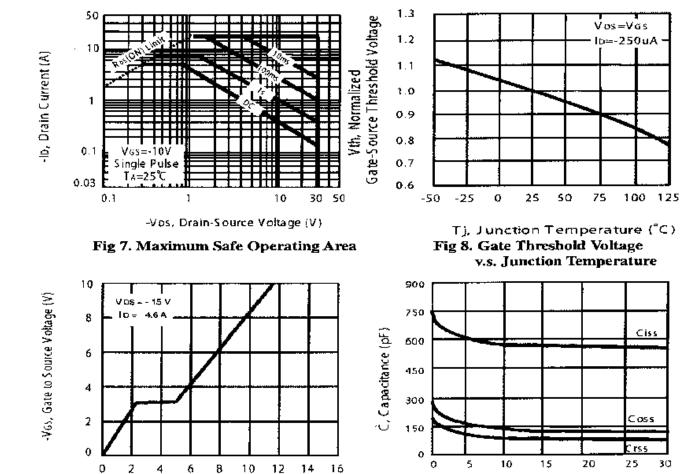


Fig 9. Gate Charge Characteristics

Qg, Total Gate Charge (nC)

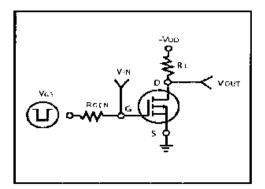


Fig 11. Switching Time Circuit

Fig 10. Typical Capacitance Characteristics

-Vos, Drain-to Source Voltage (V)

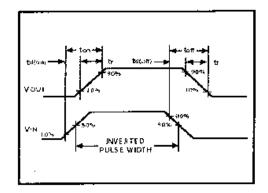


Fig 12. Switching Time Waveform

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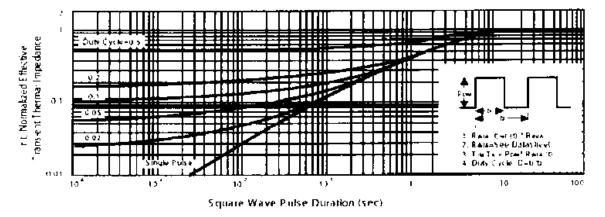
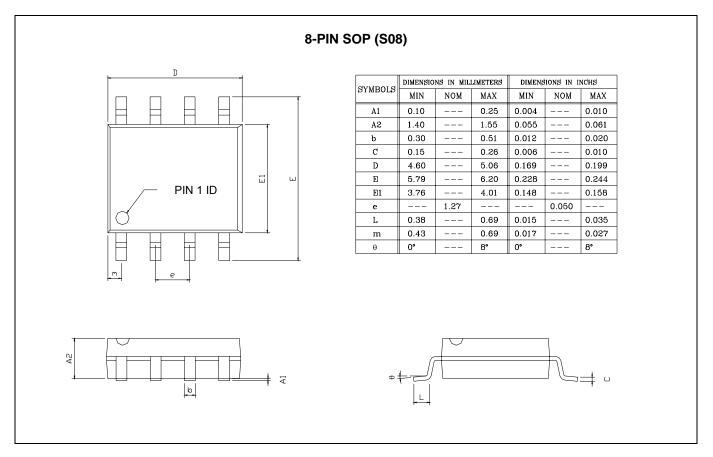


Fig 13. Normalized Thermal Transient Impedance Curve

PACKAGE DIMENSION





IMPORTANT NOTICE

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