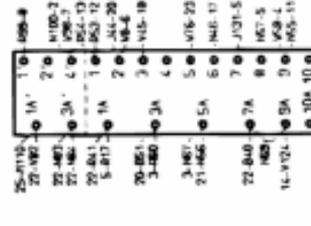
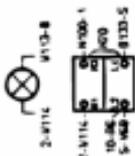


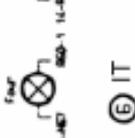
① COM



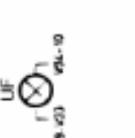
② INT + VPRF



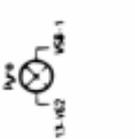
③ VO



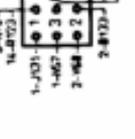
④ VO



⑤ PR



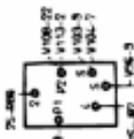
⑥ IT



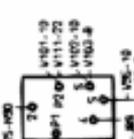
⑦ REG F AVD



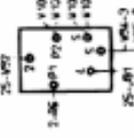
⑧ REG F ARD



⑨ REG F ARG



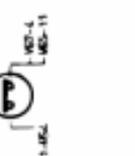
⑩ REG F AVG



⑪ THCU



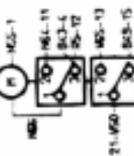
⑫ 1 60° TG



⑬ STH



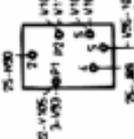
⑭ VERR



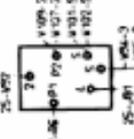
⑮ REG F AVD



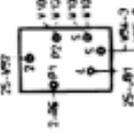
⑯ REG F ARD



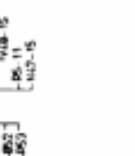
⑰ REG F ARG



⑱ REG F AVG



⑳ THCU



㉑ 1 60° TG



㉒ STH



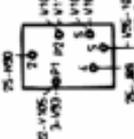
㉓ VERR



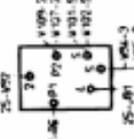
㉔ REG F AVD



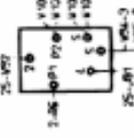
㉕ REG F ARD



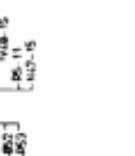
㉖ REG F ARG



㉗ REG F AVG



㉘ THCU



㉙ 1 60° TG



㉚ STH



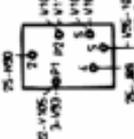
㉛ VERR



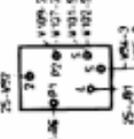
㉜ REG F AVD



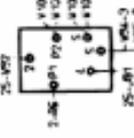
㉝ REG F ARD



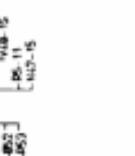
㉞ REG F ARG



㉟ REG F AVG



㊱ THCU



㊲ 1 60° TG



㊳ STH



㊴ VERR



㊵ REG F AVD

