FAIRCHILD SEMICONDUCTOR®

April 2012

FSB117H / FSB127H / FSB147H
mWSaver™ Fairchild Power Switch (FPS™)

Features

mWSaver™ Technology

- Achieve Low No-Load Power Consumption Less than 40mW at 230V_{AC} (EMI Filter Loss Included)
- Meets 2013 ErP Standby Power Regulation (Less than 0.5W Consumption with 0.25W Load) for ATX Power and LCD TV Power
- Eliminate X-Cap Discharge Resistor Loss with Ax-CAP™ Technology
- Linearly Decreased Switching Frequency at Light-Load Condition and Advanced Burst Mode Operation at No-Load Condition
- 700V High-Voltage JFET Startup Circuit to Eliminate the Startup Resistor Loss

Highly Integrated with Rich Features

- Internal Avalanche-Rugged 700V SenseFET
- Built-in 5ms Soft-Start
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Proprietary Asynchronous Jitter to Reduce EMI

Advanced Protection

- Internal Overload / Open-Loop Protection (OLP)
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Constant Power Limit (Full AC Input Range)
- Internal Auto Restart Circuit (OLP, V_{DD} OVP, OTP)
- Internal OTP Sensor with Hysteresis
- Adjustable Peak Current Limit

Related Resources

- *Evaluation Board: FEBFSB127H_T001*
- *Fairchild Power Supply WebDesigner — Flyback Design & Simulation - In Minutes at No Expense*

Description

The FSB-series is a next-generation, green-mode Fairchild Power Switch (FPS™) incorporating Fairchild's innovative mWSaver™ technology, which dramatically reduces standby and no-load power consumption, enabling conformance to all worldwide Standby Mode efficiency guidelines. It integrates an advanced current-mode pulse width modulator (PWM) and an avalanche-rugged 700V SenseFET in a single package, allowing auxiliary power designs with higher standby energy efficiency, reduced size, improved reliability, and lower system cost than previous solutions.

Fairchild Semiconductor's mWSaver™ technology offers best-in-class minimum no-load and light-load power consumption. An innovative Ax-CAP™ method, one of the five proprietary mWSaver™ technologies, minimizes losses in the EMI filter stage by eliminating the X-cap discharge resistors while still meeting IEC61010-1 safety requirement. mWSaver™ Green Mode gradually decreases switching frequency as load decreases to minimize switching losses.

A new proprietary asynchronous jitter decreases EMI emission and built-in synchronized slope compensation allows stable peak-current-mode control over a wide range of input voltage. The proprietary internal line compensation ensures constant output power limit over entire universal line voltage range.

Requiring a minimum number of external components, the FSB-series provides a basic platform that is well suited for the cost-effective flyback converter design with low standby power consumption.

Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Auxiliary Power Supply for PC, Server, LCD TV, and Game Console
- SMPS for VCR, SVR, STB, DVD, and DVCD Player, Printer, Facsimile, and Scanner
- General Adapter
- LCD Monitor Power / Open-Frame SMPS

Ordering Information

Part Number	SenseFET	Operating Temperature Range	Package Packing	Method
FSB117HNY	1A 700V	-40°C to +105°C	8-pin, Dual In-Line Package (DIP)	Tube
FSB127HNY	2A 700V			
FSB147HNY	4A 700V			

Application Diagram

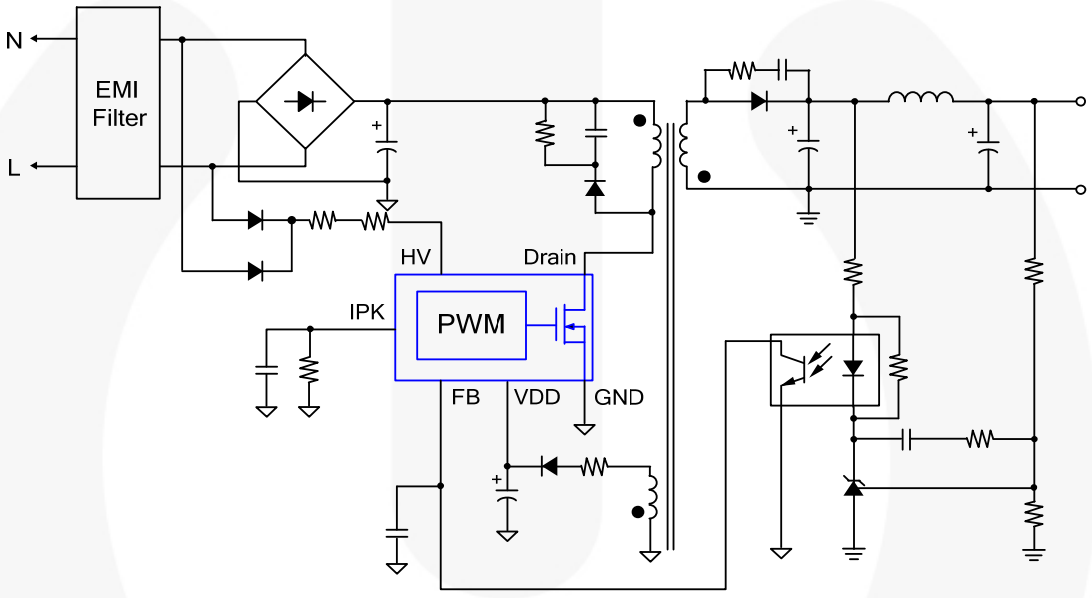


Figure 1. Typical Flyback Application

Table 1. Output Power Table[1]

Product	230V_{AC} ±15%[2] 85-2		65V_{AC}	
	Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]
FSB117H	10W	15W	9W	13W
FSB127H	14W	20W	11W	16W
FSB147H	23W	35W	17W	26W

Notes:

1. The maximum output power can be limited by junction temperature.
2. 230 V_{AC} or 100/115 V_{AC} with voltage doubler.
3. Typical co ntinuous p ower in a non-v entilated enc losed a dapter with su fficient drai n p attern of print ed circu it board (PCB) as a heat sink, at 50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern of printed circuit board (PCB) as a heat sink, at 50°C ambient.

Internal Block Diagram

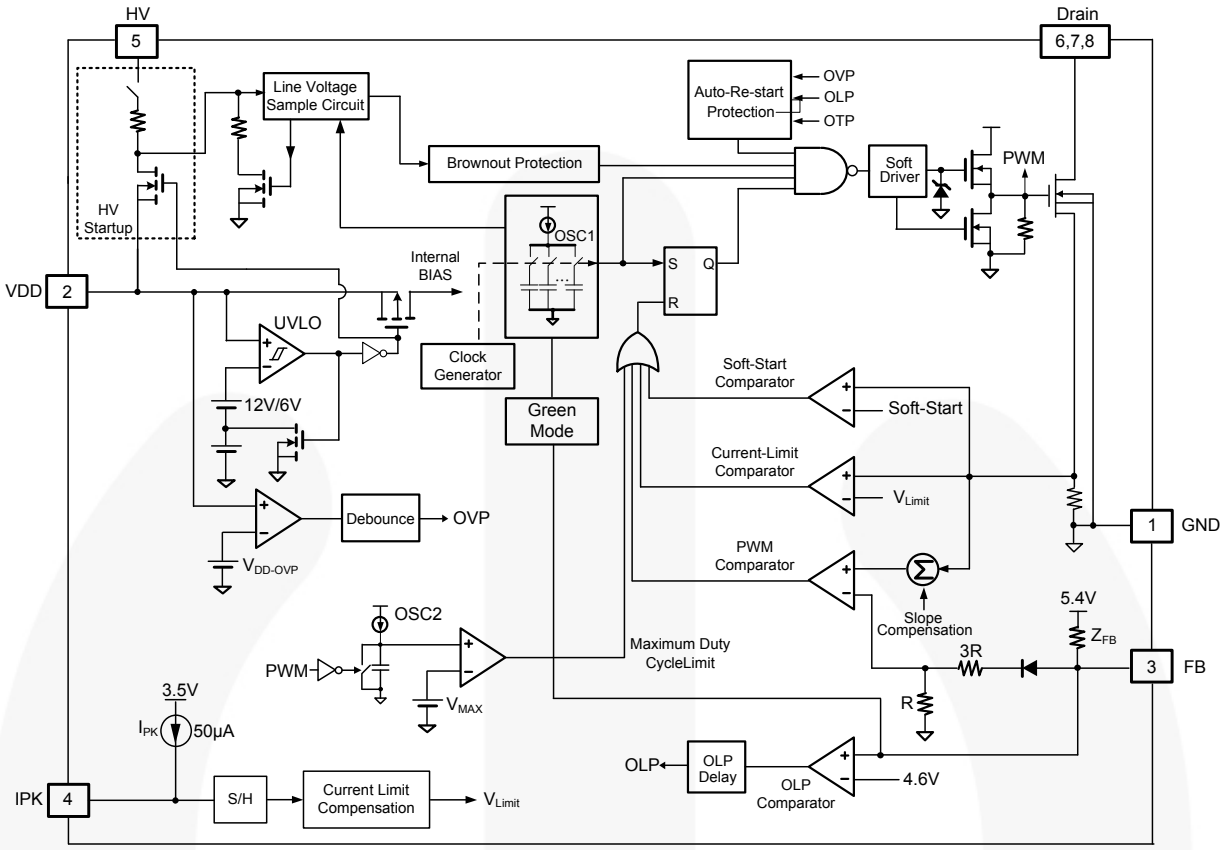
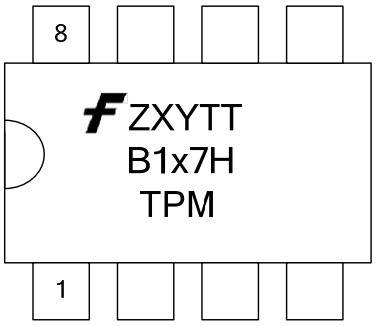


Figure 2. Block Diagram

Pin Configuration



F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2-Digit Die Run Code
T – Package Type (N: DIP)
P – Y: Green Package
M – Manufacture Flow Code

Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	Ground. This pin internally connects to the SenseFET source and signal ground of the PWM controller.
2	VDD	Supply voltage of the IC. Typically the holdup capacitor connects from this pin to ground. Rectifier diode in series with the transformer auxiliary winding connects to this pin to supply bias during normal operation.
3	FB	Feedback. The signal from the external compensation circuit connects to this pin. The PWM duty cycle is determined by comparing the signal on this pin and the internal current-sense signal.
4	IPK	Adjust peak current. Typically a resistor connects from this pin to the GND pin to program the current-limit level. The internal current source (50μA) introduces voltage drop across the resistor, which determines the current limit level of pulse-by-pulse current limit.
5	HV	Startup. Typically, resistors in series with diodes from the AC line connect to this pin to supply internal bias and to charge the external capacitor connected between the VDD pin and the GND pin during startup. This pin is also used to sense the line voltage for brownout protection and AC line disconnection detection.
6	Drain	SenseFET drain. This pin is designed to directly drive the transformer.
7		
8		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DRAIN}	Drain Pin Voltage[5,6]			700	V
I_{DM}	Drain Current Pulsed[7]	FSB117H		4.0	A
		FSB127H		8.0	
		FSB147H[9]		9.6	
E_{AS}	Single Pulsed Avalanche Energy[8]	FSB117H		50	mJ
		FSB127H		140	
		FSB147H		120	
V_{DD}	DC Supply Voltage			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{IPK}	IPK Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			700	V
P_D	Power Dissipation (T_A < 50°C)		1.5		W
T_J	Operating Junction Temperature		-40	Internally Limited[10]	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Soldering Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin	Human Body Model: JESD22-A114	5.50		kV
		Charged Device Model: JESD22-C101	2.00		
	Electrostatic Discharge Capability, All Pins Including HV Pin	Human Body Model: JESD22-A114	3.00		
		Charged Device Model: JESD22-C101	1.25		

Notes:
5. All voltage values, except differential voltages, are given with respect to the network ground terminal.
6. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
7. Non-repetitive rating: pulse width is limited by maximum junction temperature.
8. L=51mH, starting T_J=25°C.
9. L=14mH, starting T_J=25°C.
10. Internally limited by Over-Temperature Protection (OTP). Refer to T_{OTP}.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
R_{HV}	Resistor Connect to HV Pin for Full Range Input Detection	150	250	kΩ

Thermal Resistance Table

Symbol	Parameter	Typ.	Unit
θ_{JA}	Junction-to-Air Thermal Resistance	86	°C/W
ψ_{JT}	Junction-to-Package Thermal Resistance[11]	20	°C/W

Note:
11. Measured on the package top surface.

Electrical Characteristics

V_{DD}=15V, T_A=25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SenseFET Section[12]							
BV_{DSS}	Drain-Source Breakdown Voltage		V_{DS}=700V, V_{GS}=0V	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS}=700V, V_{GS}=0V			50	μA
			V_{DS}=560V, V_{GS}=0V, T_C=125°C			200	
$R_{DS(ON)}$	Drain-Source On-State Resistance[13]	FSB117H	V_{GS}=10V, I_D=0.5A	8.8		11.0	Ω
		FSB127H			6.0	7.2	
		FSB147H V	$_{GS}$=10V, I_D=2.5A		2.3	2.7	
C_{ISS}	Input Capacitance	FSB117H	V_{GS}=0V, V_{DS}=25V, f=1MHz	250		325	pF
		FSB127H			550	715	
		FSB147H			450	500	
C_{OSS}	Output Capacitance	FSB117H	V_{GS}=0V, V_{DS}=25V, f=1MHz	25		33	pF
		FSB127H			38	50	
		FSB147H			60	72	
C_{RSS}	Reverse Transfer Capacitance	FSB117H	V_{GS}=0V, V_{DS}=25V, f=1MHz	10		15	pF
		FSB127H			17	26	
		FSB147H			7	21	
$t_{d(on)}$	Turn-On Delay	FSB117H	V_{DS}=350V, I_D=1.0A	12		34	ns
		FSB127H			20	50	
		FSB147H			12	35	
t_r	Rise Time	FSB117H	V_{DS}=350V, I_D=1.0A	4		18	ns
		FSB127H			15	40	
		FSB147H			20	50	
$t_{d(off)}$	Turn-Off Delay	FSB117H	V_{DS}=350V, I_D=1.0A	30		70	ns
		FSB127H			55	120	
		FSB147H			30	70	
t_f	Fall Time	FSB117H	V_{DS}=350V, I_D=1.0A	10		30	ns
		FSB127H			25	60	
		FSB147H			16	42	

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Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Control Section						
VDD Section						
V_{DD-ON}	UVLO Start Threshold Voltage		11	12	13	V
$V_{DD-OFF1}$	UVLO Stop Threshold Voltage		5	6	7	V
$V_{DD-OFF2}$	I_{DD-OLP} Enable Threshold Voltage		8	9	10	V
V_{DD-OLP}	V_{DD} Voltage Threshold for HV Startup Turn-On at Protection Mode	5		6	7	V
I_{DD-ST}	Startup Supply Current	V_{DD-ON} – 0.16V			30	µA
I_{DD-OP1}	Operating Supply Current with Normal Switching Operation	V_{DD}=15V, V_{FB}=3V			3.8	mA
I_{DD-OP2}	Operating Supply Current without Switching Operation	V_{DD}=15V, V_{FB}=1V			1.8	mA
I_{DD-OLP}	Internal Sinking Current	V_{DD-OLP} + 0.1V	30	60	90	µA
V_{DD-OVP}	V_{DD} Over-Voltage Protection		27	28	29	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time	70		140	210	µs
HV Section						
I_{HV}	Supply Current Drawn from HV Pin	HV=120V_{DC}, V_{DD}=0V with 10µF	1.5		5.0	mA
I_{HV-LC}	Leakage Current after Startup	HV=700V, V_{DD}=$V_{DD-OFF1}$+1V			10	µA
V_{AC-ON}	Brown-in Threshold Level (V_{DC})	DC Voltage Applied to HV Pin Through 200kΩ Resistor	105	110	115	V
V_{AC-OFF}	Brownout Threshold Level (V_{DC})			V_{AC-ON}-10		V
t_{UVP}	Brownout Protection Time		0.8	1.2	1.6	s
Oscillator Section						
f_{OSC}	Frequency in Nominal Mode	Center Frequency	94	100	106	kHz
		Hopping Range	±4.0	±6.0	±8.0	
t_{HOP}	Hopping Period[12]			20		ms
f_{OSC-G}	Green-Mode Frequency		20	23	26	kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation[12]	T_A=-40 to 105°C			5	%

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Feedback Input Section							
A_V	Internal Voltage Dividing Factor of FB Pin(12)			1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Pull-Up Impedance of FB Pin			15	21	27	kΩ
$V_{FB-OPEN}$	FB Pin Pull-Up Voltage		FB Pin Open	5.2	5.4	5.6	V
V_{FB-OLP}	FB Voltage Threshold to Trigger Open-Loop Protection		4.3		4.6	4.9	V
t_{D-OLP}	Delay of FB Pin Open-Loop Protection			46	56	66	ms
V_{FB-N}	FB Voltage Threshold to Exit Green Mode		V_{FB} is Rising	2.4	2.6	2.8	V
V_{FB-G}	FB Voltage Threshold to enter Green Mode		V_{FB} is Falling		V_{FB-N}-0.2		V
V_{FB-ZDC}	FB Voltage Threshold to Enter Zero-Duty State		V_{FB} is Falling	1.95	2.05	2.15	V
$V_{FB-ZDCR}$	FB Voltage Threshold to Exit Zero-Duty State		V_{FB} is Rising		V_{FB-ZDC} +0.1		V
IPK Pin Section							
$V_{IPK-OPEN}$	IPK Pin Open Voltage			3.0	3.5	4.0	V
V_{IPK-H}	Internal Upper Clamping Voltage of IPK Pin					3(12)	V
V_{IPK-L}	Internal Lower Clamping Voltage of IPK Pin			1.5(12)			V
I_{PK}	Internal Current Source of IPK Pin		T_A=-40 to 105°C, V_{IPK}=2.25V	45	50	55	µA
$I_{LMT-FL-H}$	Current Limit Plateau when I_{PK} Pin Voltage is Internally Clamped to Upper Limit	FSB117H	V_{IPK}=3V, Duty>40%	0.72	0.80	0.88	A
		FSB127H		0.90	1.00	1.10	
		FSB147H		1.35	1.50	1.65	
$I_{LMT-VA-H}$	Initial Current Limit when I_{PK} Pin Voltage is Internally Clamped to Upper Limit	FSB117H	V_{IPK}=3V, Duty=0%		$I_{LMT-FL-H}$ -0.20		A
		FSB127H			$I_{LMT-FL-H}$ -0.25		
		FSB147H			$I_{LMT-FL-H}$ - 0.37		
$I_{LMT-FL-L}$	Current Limit Plateau when I_{PK} Pin Voltage is Internally Clamped to Lower Limit	FSB117H	V_{IPK}=1.5V, Duty>40%	0.36	0.40	0.44	A
		FSB127H		0.45	0.50	0.55	
		FSB147H		0.67	0.75	0.83	
$I_{LMT-VA-L}$	Initial Current Limit when I_{PK} Pin Voltage is Internally Clamped to Lower Limit	FSB117H	V_{IPK}=1.5V, Duty=0%		$I_{LMT-FL-L}$ -0.10		A
		FSB127H			$I_{LMT-FL-L}$ -0.12		
		FSB147H			$I_{LMT-FL-L}$ - 0.18		

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Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Current-Sense Section(14)						
t_{PD}	Current Limit Turn-Off Delay			100	200	ns
t_{LEB}	Leading-Edge Blanking Time		230	280	330	ns
t_{SS}	Soft-Start Time(12)			5		ms
GATE Section(14)						
DCY_{MAX}	Maximum Duty Cycle		70			%
Over-Temperature Protection Section (OTP)						
T_{OTP}	Junction Temperature to trigger OTP(12)		135	142	150	°C
ΔT_{OTP}	Hysteresis of OTP(12)			25		°C

Notes:

12. Guaranteed by design; not 100% tested in production.
13. Pulse test: pulse width ≤ 300μs, duty ≤ 2%.
14. These parameters, although guaranteed, are tested in wafer-sort process.

Typical Characteristics

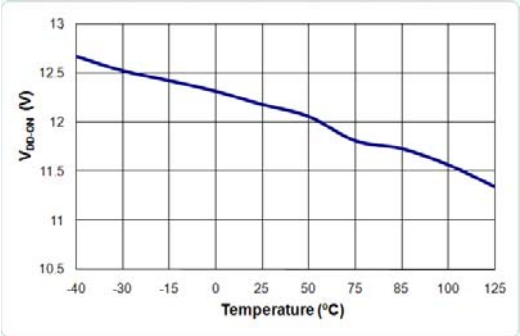

Figure 4. V_{DD-ON} vs. Temperature

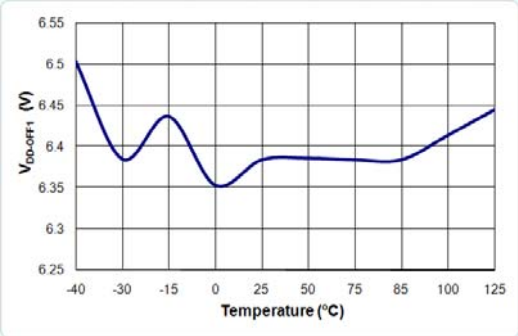

Figure 5. $V_{DD-OFF1}$ vs. Temperature

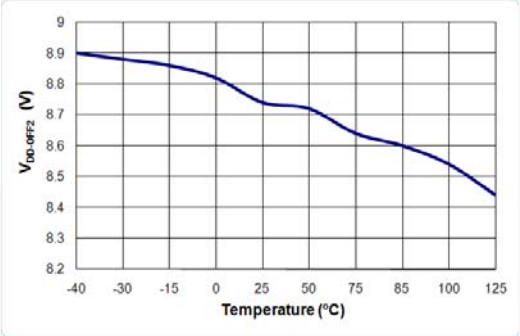

Figure 6. $V_{DD-OFF2}$ vs. Temperature

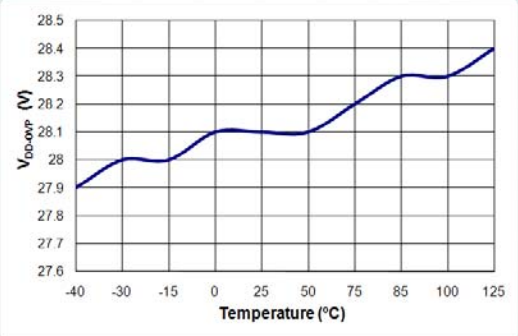

Figure 7. V_{DD-OVP} vs. Temperature

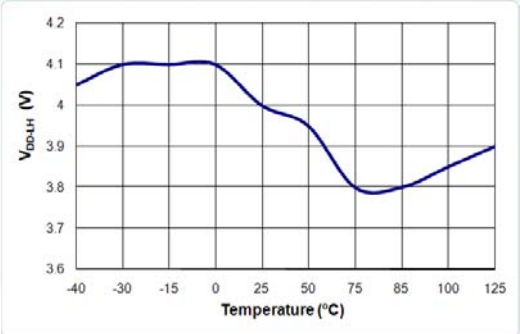

Figure 8. V_{DD-LH} vs. Temperature

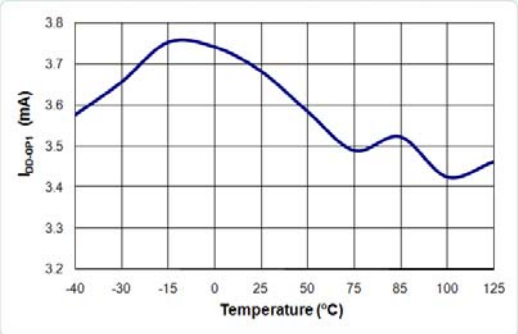

Figure 9. I_{DD-OP1} vs. Temperature

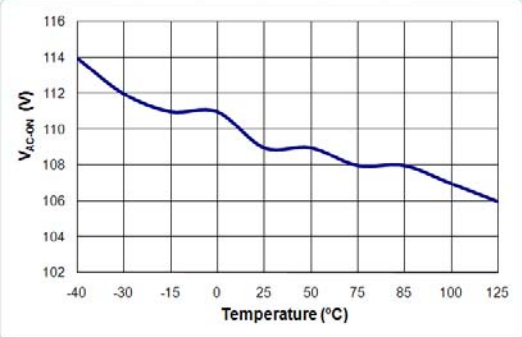

Figure 10. V_{AC-ON} vs. Temperature

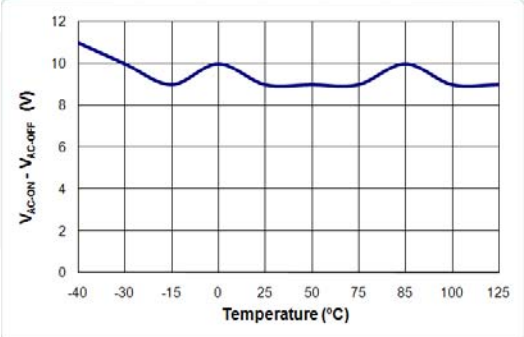

Figure 11. V_{AC-ON} – V_{AC-OFF} vs. Temperature

Typical Characteristics

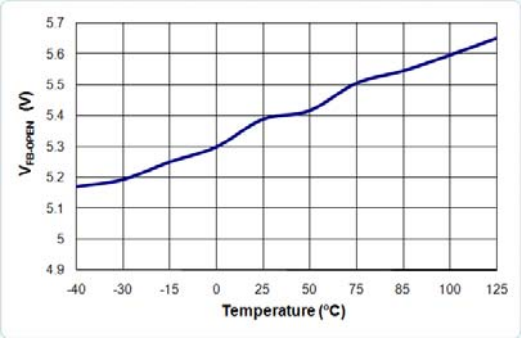

Figure 12. $V_{FB-OPEN}$ vs. Temperature

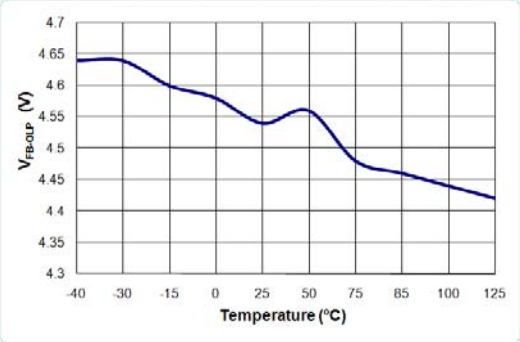

Figure 13. V_{FB-OLP} vs. Temperature

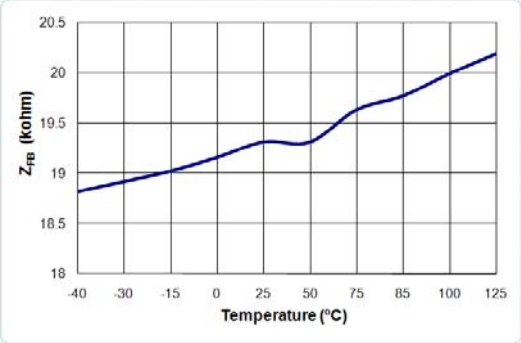

Figure 14. Z_{FB} vs. Temperature

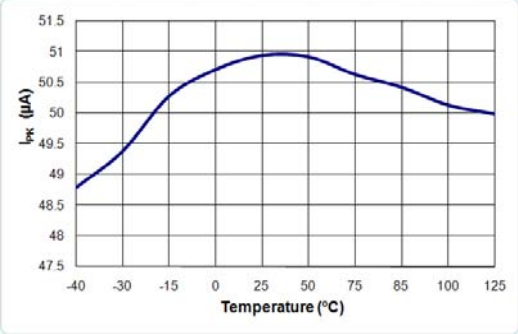

Figure 15. I_{PK} vs. Temperature

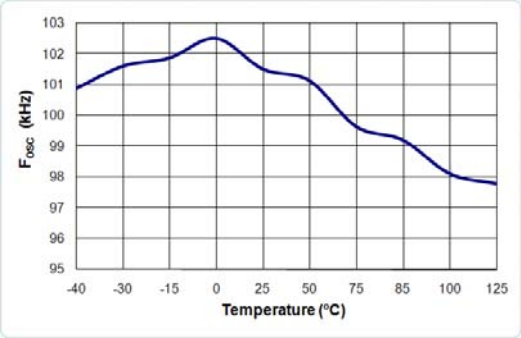

Figure 16. f_{OSC} vs. Temperature

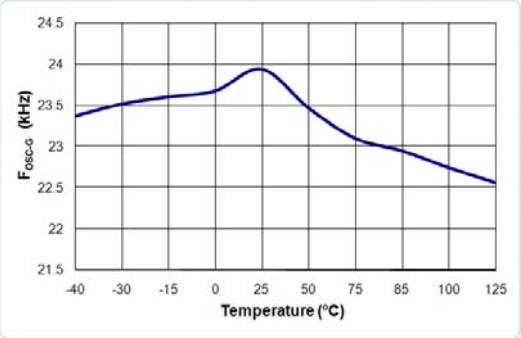

Figure 17. f_{OSC-G} vs. Temperature

Functional Description

Startup Operation

The HV pin is typically connected to the AC line input through two external diodes and one resistor (R_{HV}), as shown in Figure 18. When the AC line voltage is applied, the V_{DD} hold-up capacitor is charged by the line voltage through the diodes and resistor. After V_{DD} voltage reaches the turn-on threshold voltage (V_{DD-ON}), the startup circuit charging V_{DD} capacitor is switched off and V_{DD} is supplied by the auxiliary winding of the transformer. Once the FSB-series starts, it continues operation until V_{DD} drops below 6V ($V_{DD-OFF1}$). The IC startup time with a given AC line input voltage is:

$$t_{STARTUP} = \frac{R_{HV} \cdot C_{DD} \cdot \ln\left(\frac{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi} - V_{DD\_ON}}\right)}{} \quad (1)$$

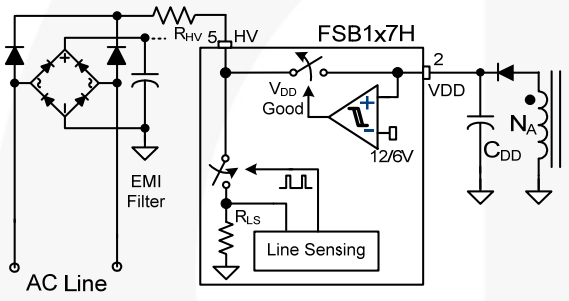

Figure 18. Startup Circuit

Brown-in/out Function

The HV pin can detect the AC line voltage using a switched voltage divider that consists of external resistor (R_{HV}) and internal resistor (R_{LS}), as shown in Figure 18. The internal line sensing circuit detects the real RMS value of the line voltage using sampling circuit and peak detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize the power consumption in light-load condition.

Based on the detected line voltage, brown-in and brownout thresholds are determined. Since the internal resistor (R_{LS}) of the voltage divider is much smaller than R_{HV}, the thresholds are given as:

$$V_{BROWN-IN}(RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-ON}}{\sqrt{2}} \quad (2)$$

$$V_{BROWN-OUT}(RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-OFF}}{\sqrt{2}} \quad (3)$$

PWM Control

The FSB-series employs current-mode control, as shown in Figure 19. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. A synchronized positive slope is added to the SenseFET current information to guarantee stable current-mode control over a wide range of input voltage. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

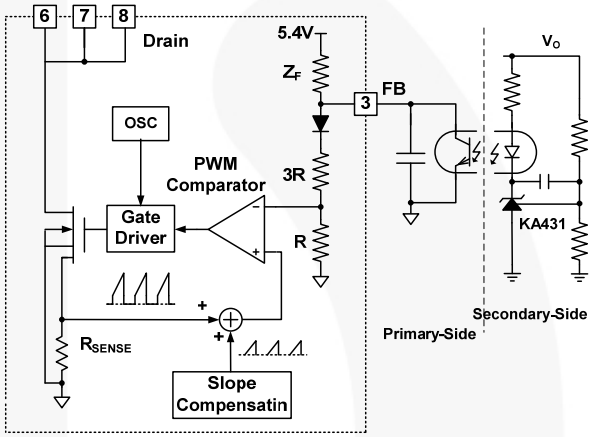

Figure 19. Current Mode Control

Soft-Start

The FSB-series has an internal soft-start circuit that progressively increases the pulse-by-pulse current limit level of MOSFET during start up to establish the correct working conditions for transformers and capacitors, as shown in Figure 20. The current limit levels have nine steps, as shown in Figure 21. This prevents transformer saturation and reduces stress on the secondary diode during startup.

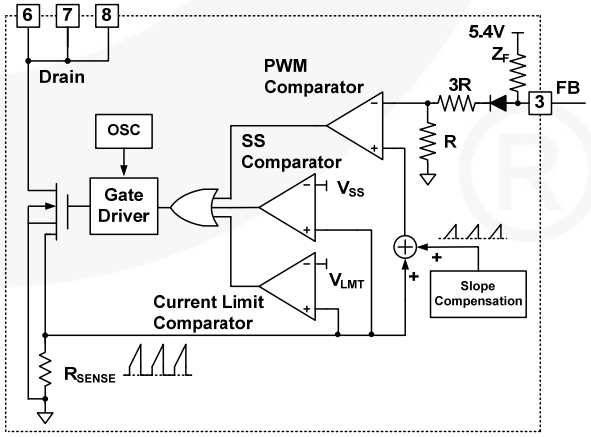

Figure 20. Soft-Start and Current-Limit Circuit

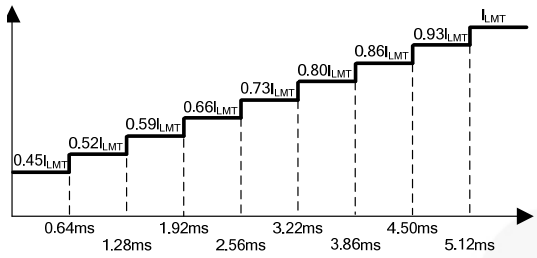

Figure 21. Current Limit Variation During Soft-Start

Adjustable Peak Current Limit & H/L Line Compensation for Constant Power Limit

To make the limited output power constant regardless of the line voltage condition, a special current-limit profile with sample and hold is used (as shown in Figure 22). The current-limit level is sampled and held at the falling edge of gate drive signal as shown in Figure 23. Then, the sampled current limit level is used for the next switching cycle. The sample-and-hold function prevents sub-harmonic oscillation in current-mode control.

The current-limit level increases as the duty cycle increases, which reduces the current limit as duty cycle decreases. This allows lower current-limit level for high-line voltage condition where the duty cycle is smaller than that of low line. Therefore, the limited maximum output power can remain constant even for a wide input voltage range.

The peak current limit is programmable using a resistor on the IPK pin. The internal current 50μA source for the IPK pin generates voltage drop across the resistor. The voltage of the IPK pin determines the current-limit level. Since the upper and lower clamping voltage of the IPK pin are 3V and 1.5V, respectively, the suggested resistor value is from 30kΩ to 60kΩ.

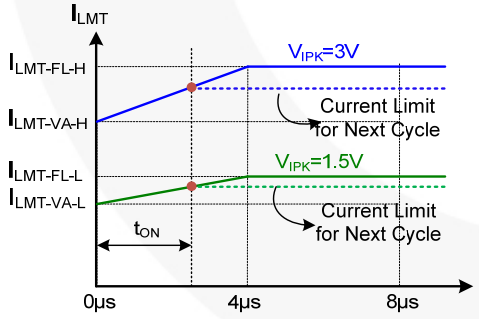

Figure 22. I_{LMT} vs. PWM Turn-On Time

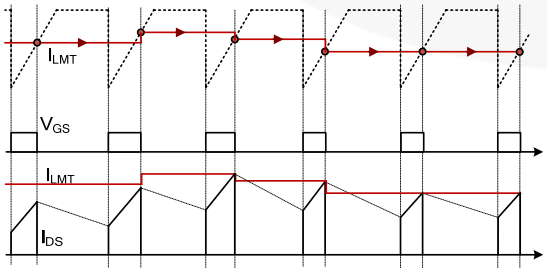

Figure 23. Current Limit Variation with Duty Cycle

mWSaver™ Technology

Ax-CAP™ to Remove X-Cap Discharge Resistor

The EMI filter in the front end of the switched mode power supply typically includes a capacitor across the AC line connector, as shown in Figure 24. Most of the safety regulations, such as UL 1950 and IEC61010-1, require the capacitor be discharged to a safe level within a given time after unplugged from the power outlet. Typically a discharge resistor across the capacitor is used to ensure the capacitor is discharged naturally, which however introduces power loss of the power supply. As power level increases, the EMI filter capacitor tends to increase, requiring a smaller discharge resistor to maintain same discharge time. This typically results in more power dissipation in high-power applications. The innovative Ax-CAP™ technology intelligently discharges the filter capacitor only when the power supply is unplugged from the power outlet. Since the Ax-CAP™ discharge circuit is disabled in normal operation, the power loss in the EMI filter size can be virtually removed.

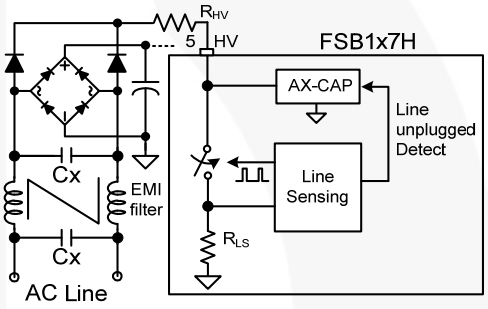

Figure 24. AX-Cap™ Circuit

Green Mode

The FSB-series modulates the PWM frequency as a function of FB voltage, as shown in Figure 25. Since the output power is proportional to the FB voltage in current-mode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 100kHz. Once V_{FB} decreases below V_{FB-N} (2.6V), the PWM frequency linearly decreases from 100kHz to 23kHz to reduce switching losses at light-load condition. As V_{FB} decreases to V_{FB-G} (2.4V), the switching frequency is fixed at 23kHz.

As V_{FB} falls below V_{FB-ZDC} (2.1V), the FSB-series enters Burst Mode operation, where PWM switching is disabled. Then, the output voltage starts to drop, causing the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$, switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss to reduce power consumption, as shown in Figure 26.

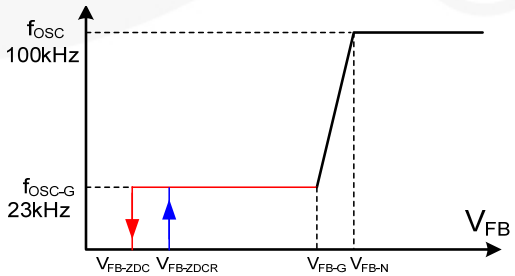

Figure 25. PWM Frequency

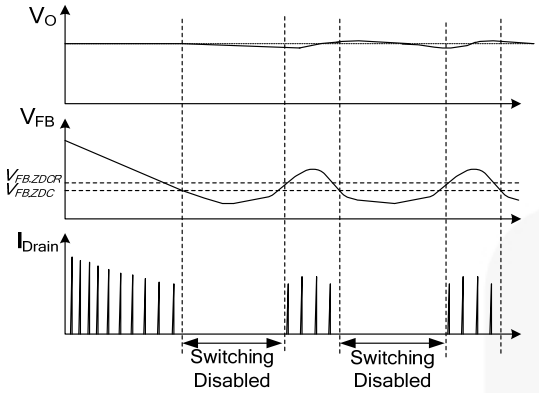

Figure 26. Burst-Mode Operation

Protections

The FSB-series provides protection function, that include Overload / Open-Loop Protection (OLP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP). All the protections are implemented as Auto-Restart Mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{DD} to fall. When V_{DD} falls to 6V, the protection is reset and HV startup circuit charges V_{DD} up to 12V voltage, allowing re-startup.

Open-Loop / Overload Protection (OLP)

Because of the pulse-by-pulse current-limit capability, the maximum peak current through the SenseFET is limited and maximum input power is limited. If the output consumes more than the limited maximum power, the output voltage (V_O) drops below the set voltage. Then the current through the opto-coupler LED and the transistor become virtually zero and FB voltage is pulled HIGH as shown in Figure 27. If feedback voltage is above 4.6V for longer than 56ms, OLP is triggered. This protection is also triggered when the feedback loop is open due to a soldering defect.

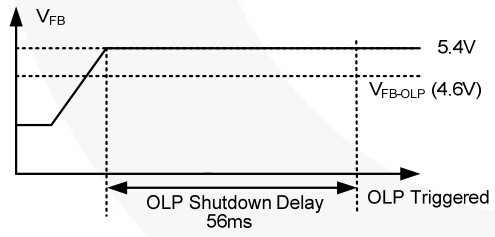

Figure 27. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes virtually zero. Then feedback voltage climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. Since V_{DD} voltage is proportional to the output voltage by the transformer coupling, the overvoltage of output is indirectly detected using V_{DD} voltage. The OVP is triggered when V_{DD} voltage reaches 28V. Debounce time (typically 150μs) is applied to prevent false triggering by switching noise.

Over-Temperature Protection (OTP)

The SenseFET and the control IC are integrated in one package. This makes it easy for the control IC to detect the abnormal overtemperature of the SenseFET. If the temperature exceeds approximately 140°C, the OTP is triggered and the MOSFET remains off. When the junction temperature drops by 25°C from OTP temperature, the FSB-series resumes normal operation.

Two-Level UVLO

Since all the protections of the FSB-series are auto-restart, the power supply repeats shutdown and re-startup until the fault condition is removed. FSB-series has two-level UVLO, which is enabled when protection is triggered, to delay the re-startup by slowing down the discharge of V_{DD}. This effectively reduces the input power of the power supply during the fault condition, minimizing the voltage/current stress of the switching devices. Figure 28 shows the normal UVLO operation and two-step UVLO operation. When V_{DD} drops to 6V without triggering the protection, PWM stops switching and V_{DD} is charged up by the HV startup circuit. Meanwhile, when the protection is triggered, FSB-series has a different V_{DD} discharge profile. Once the protection is triggered, the IC stops switching and V_{DD} drops. When V_{DD} drops to 9V, the operating current becomes very small and V_{DD} is slowly discharged. When V_{DD} is naturally discharged down to 6V, the protection is reset and V_{DD} is charged up by the HV startup circuit. Once V_{DD} reaches 12V, the IC resumes switching operation.

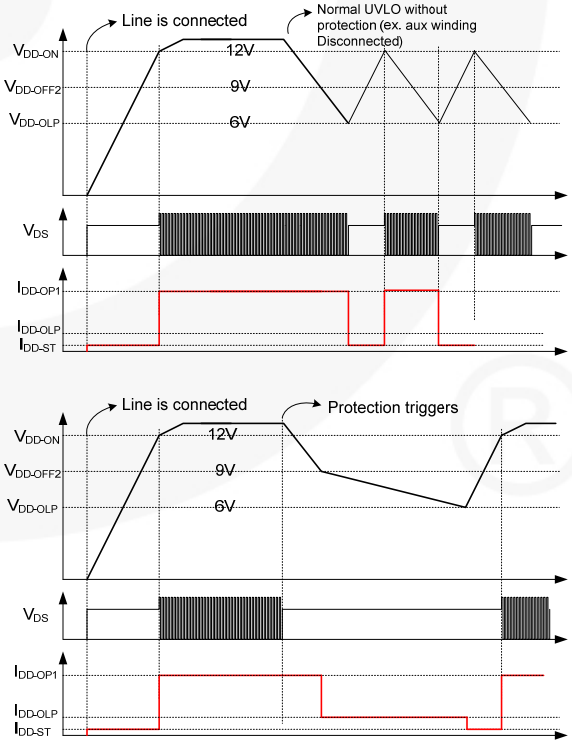

Figure 28. Two-Level UVLO

Typical Application Circuit

Application	Fairchild Devices	Input Voltage Range	Output
Standby Auxiliary Power	FSB127H	$85V_{AC}$ ~ $265V_{AC}$	5V/3.2A

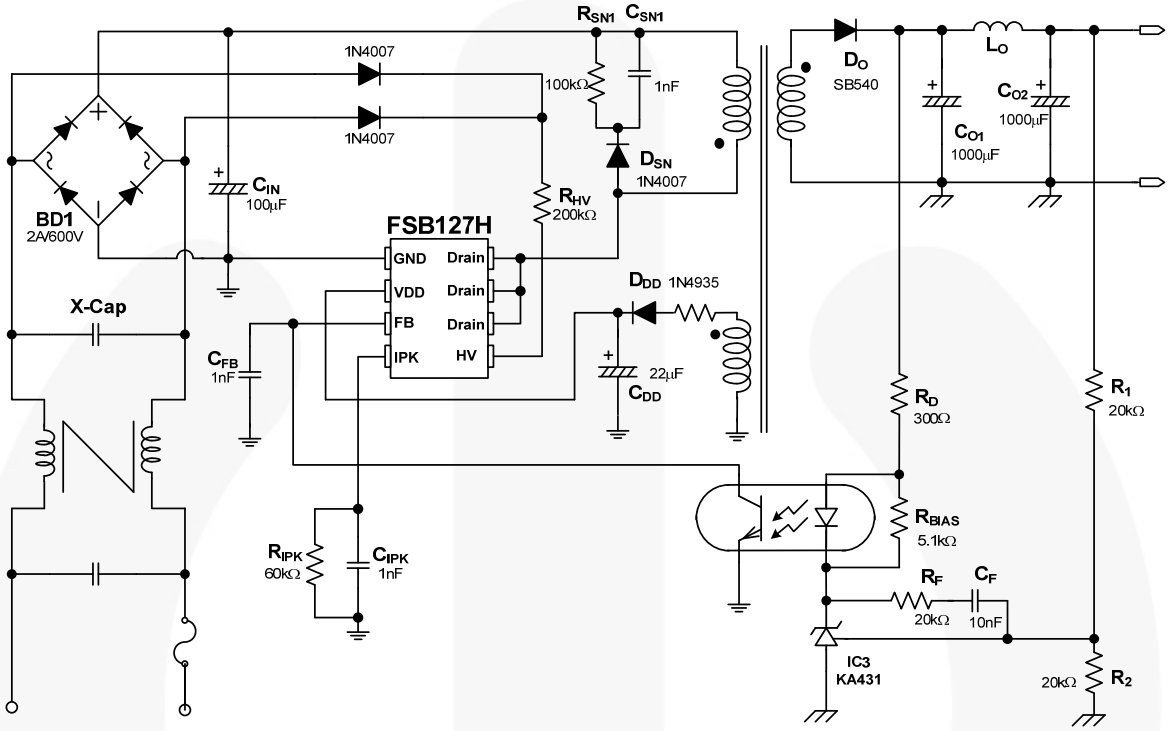

Figure 29. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: EI 22
- Bobbin: EI 22

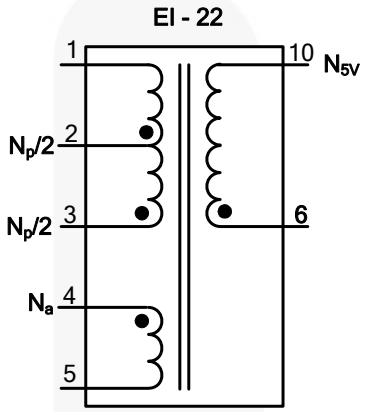

Figure 30. Transformer Specification

Pin	(S → F)	Wire	Turns	Winding Method
N_a	4 → 5	0.15φ×1	12	Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 1-Layer				
$N_p/2$	3 → 2	0.27φ×1	31	Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 2-Layer				
N_{5V}	6 → 10	0.55φ×2	5	Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 2-Layer				
$N_p/2$	2 → 1	0.27φ×1	31	Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 2-Layer				

Pin		Specification	Remark
Primary-Side Inductance	1 – 3	900μH ±10%	100kHz, 1V
Primary-Side Effective Leakage	1 – 3	< 30μH Maximum	Short All Other Pins

Physical Dimensions

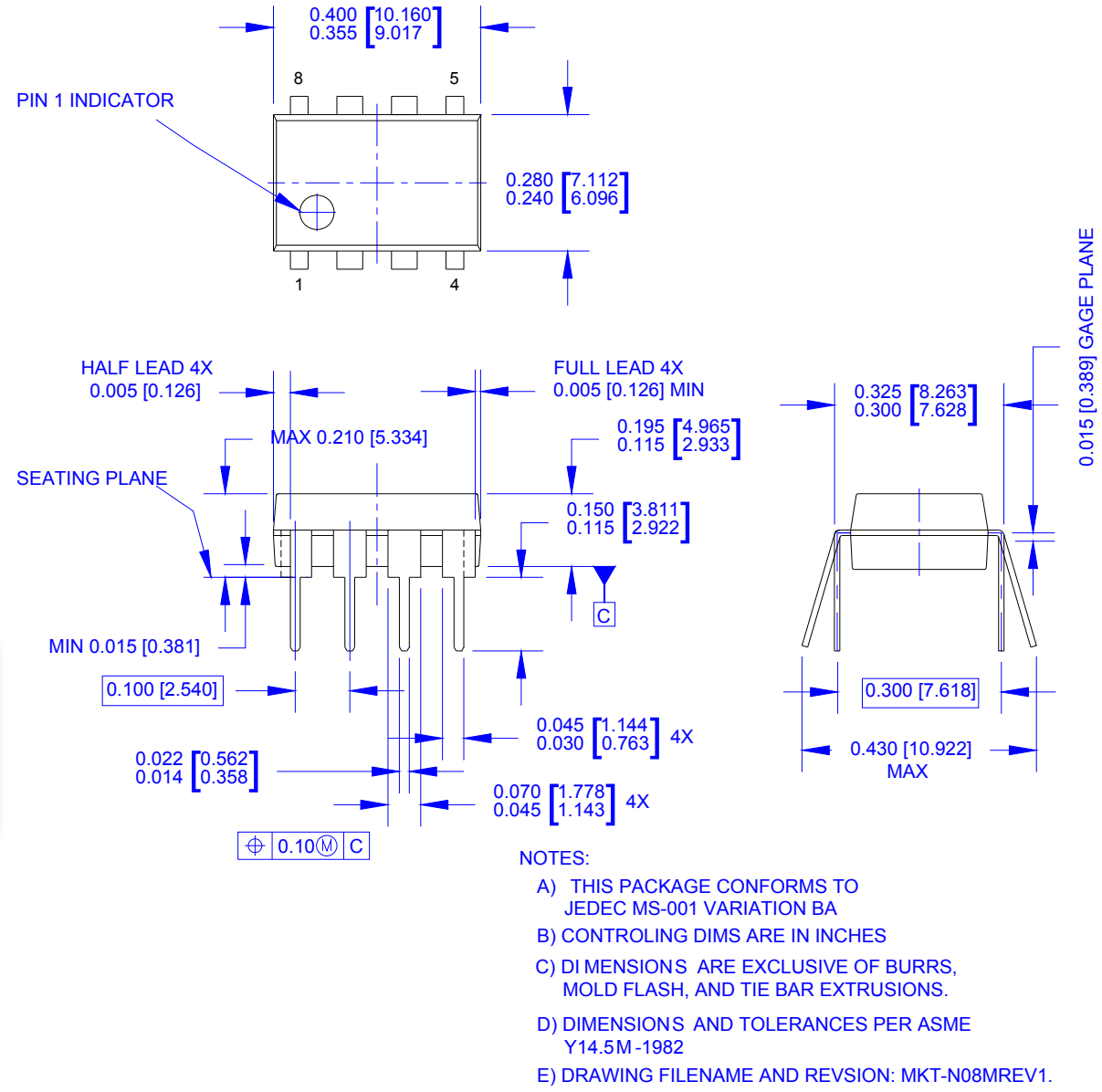

Figure 31. 8-Pin, Dual In-Line Package (DIP)

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Rev. I61