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# AVR097: Migration between ATmega128 and ATmega1281/ATmega2561

## Features

- General Porting Considerations
- Memory
- Clock sources
- Interrupts
- Power Management
- BOD
- WDT
- Timers/Counters
- USART & SPI
- ADC
- Analog Comparator
- ATmega103 Compatibility
- Operational Range

## 1 Introduction

This application note summarizes the differences between ATmega128 and ATmega1281/2561. For detailed information on the devices, refer to the datasheets.

ATmega128 and ATmega1281/2561 are designed to be a pin and functionality compatible sub family. This application note points out the differences to be aware of when porting code between the devices.



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Application Note

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## 2 General Porting Considerations

Between the devices described in this application note, some register bits are in different locations within a register. In addition some registers have changed names, and some bits are located in different registers as shown in Table 1 and Table 2.

**Table 1.** Changes to register names

Register Name in ATmega128	Register name in ATmega1281/2561
MCUCSR	MCUSR
SFIOR	-
-	TWIAMR <sup>(1)</sup>

Note: 1. The TWI Address Mask Register. This is a new feature in the Atmega1281/2561

**Table 2.** Changes to bit locations

Bit Name	ATmega128 Register	ATmega1281/2561 Register
SRE SRW10	MCUCR	XMCRA
JTD	MCUCSR	MCUCR
PUD	SFIOR	MCUCR
TSM PSR321 <sup>(1)</sup>	SFIOR	GTCCR
ACME	SFIOR	ADCSRB
SM2, SM1 SM0, SE	MCUCR	SMCR

Note: 1. Bit name is PSRSYNC in Atmega1281/2561

To make the porting process as easy as possible, always refer to registers and bit positions using their defined names. Avoid using absolute addresses and values. In most cases, the register and bit names are unchanged from device to device. When you are porting a design, it is more convenient to include the correct definition file for the new device, rather than manually changing all your addresses and bit values. It is also considered good programming practice to use named references instead of absolute values. An example is shown below.

```
PORTE |= (1<<PORTE5);           // Set pin 5 on port E high
DDR   &= ~(1<<PORTE5);         // Set pin 5 on port E as input

// Configure USI
USICR = (1<<USISIE)|(0<<USIOIE)|(1<<USIWM1)|(0<<USIWM0)|
        (1<<USICS1)|(0<<USICS0)|(0<<USICLK)|(0<<USITC);
```

To avoid conflicts with added features and register functionality, never access registers that are marked as reserved. Reserved bits should always be written to zero if accessed. This ensures forward compatibility, and added features will stay in their default states when unused.

## 3 Memory

The sizes of the memories are the main difference between the ATmega128, ATmega1281, and ATmega2561. They are all summarized in Table 3.

**Table 3.** Memory sizes

	FLASH [bytes]	SRAM [bytes]	EEPROM [bytes]
ATmega128	128k	4k	4k
ATmega1281	128k	8k	4k
ATmega2561	256k	8k	4k

### 3.1 EEPROM

The time to wait for a programming of an EEPROM page is different on ATmega128 compared to ATmega1281/2561. Typical programming times are listed in Table 4. Note that ATmega1281/2561 has an additional option for splitting the EEPROM write into a separate erase and write operation. For more details on this feature refer to the datasheet or the application note: "AVR@103: Using the EEPROM Programming Modes".

**Table 4.** Wait times when programming EEPROM

	Typical programming time
ATmega128	8.5 ms
Atmega1281/2561	3.3 ms

### 3.2 XRAM

The register bits SRE (External SRAM/XMEM Enable) and SRW10 (Wait-state Select Bit) are located in MCUCR in ATmega128 and in XMCRA in ATmega1281/2561.

## 4 Clock sources

ATmega128 has nearly all the same clock options, settings and timing as the ATmega1281/2561. An exception is that ATmega1281/2561 has an additional internal 128kHz RC Oscillator. All start-up delays on ATmega1281/2561 have a constant of 14 clock cycles added to the standard value compared to ATmega128. The functionality of the Clock Select bits (CKSEL3..0, SUT1,0, CKOPT) themselves are not equal between the devices. Refer to the datasheet to find new matching settings for the clock select configuration.

The ATmega1281/2561 has a system clock prescaler that can/has to be altered runtime from the application code to achieve the desired system clock frequency.

The system clock prescaler is implemented differently in the ATmega128 and in the ATmega1281/2561. The prescaler in ATmega1281/2561 (CLKPR) can only divide the clock by powers of two. The XDIV prescaler in ATmega128 can be set up to divide by all values from 1 to 129.

## 5 Interrupts

ATmega1281/2561 has 57 interrupts. ATmega128 has 35 interrupts. The additional interrupts in ATmega1281/2561 reflects the additional features in the device.





ATmega1281/2561 can trigger on 24-pin change events with three different interrupt vectors. ATmega128 does not have this feature.

## 6 Power Management

ATmega1281/2561 has a Power Reduction Register (PRR) that provides a method to stop the clock to individual peripherals. ATmega128 does not have this feature.

## 7 BOD

The Brown Out Detection (BOD) options are similar between the devices, except for that ATmega1281/2561 has an additional level to support the extended operation range. The bit setting to select the BOD configuration varies; Table 5 and

Table 6 show the settings for the two devices. Note that the voltage BOD levels are slightly higher on ATmega1281/2561 then on ATmega128.

**Table 5.** BOD fuse configuration on ATmega128

BODEN	BODLEVEL	Typical $V_{BOT}$ [V]
0	1	2.7
0	0	4.0
1	1	BOD disabled
1	0	BOD disabled

**Table 6.** BOD fuse configuration on ATmega1281/2561

BODLEVEL 2..0	Typical $V_{BOT}$ [V]
111	BOD disabled
110	1.8
101	2.7
100	4.3

## 8 WDT

The ATmega1281/2561 has the Enhanced Watchdog Timer (WDT), which is improved compared to the one in ATmega128. If the WDT is not used, it is still recommended to disable it initially in the application code to clear unintentional WDT enabled events.

If the operation voltage is 5V and the WDTON fuse is left unprogrammed, the WDT will behave similar on both devices. The frequency of the Watchdog Oscillator in ATmega1281/2561 is approximately 128 kHz for all supply voltages. The typical frequency of the Watchdog Oscillator in ATmega128 is close to 1.0 MHz at 5V, but the time-out period increases with decreasing VCC. This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design. In ATmega128, the Watchdog Timer is either enabled or disabled, while ATmega1281/2561 supports two safety levels selected by the WDTON Fuse. The ATmega1281/2561 has a watchdog interrupt mode that is not supported in ATmega128. Refer to the ATmega1281/2561 datasheet or the Application note "AVR132 - Enhanced Watchdog Timer" for more information.

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## 9 Timers/Counters

Timer/counter 1 and 3 are equal between the devices, except for the TIMSK registers. Here the register names and bits are differently organized. Refer to the datasheets to find the new configuration settings.

Essentially the timers/counters 0 and 2 are only swapped between the devices. I.e. the features of timer 0 in ATmega128 can be found in timer 2 in ATmega1281/2561, and vice versa. The pin mappings for these timers are also swapped. I.e. after porting the code to the other timer the pin features are still associated with the same pin as the other device. The control registers are differently organized between the devices. Please check the naming and positioning of all registers associated with timer/counter 0 and 2 when porting code, and find the new settings according to the datasheets.

When operating the timer/counter2 from an external 32.768 kHz watch crystal or an external clock source, external capacitors must be connected to the TOSC1/2 pins when using ATmega1281/2561, as opposed to ATmega128 where the crystal is connected directly between the pins. Refer to the ATmega1281/2561 datasheet for details on crystal connections.

ATmega1281/2561 has two Output Compare units on both timer/counter 0 and 2, while ATmega128 has one on each.

## 10 USART & SPI

The USART's are equal between the devices, except for that the ATmega1281/2561 has an additional SPI master mode within the USART that is not available in ATmega128. For additional SPI interface support one can use a software implementation as described in "AVR320: Software SPI Master".

## 11 ADC

Both devices have an option to use an internal 2.56V voltage reference. In addition the ATmega1281/2561 also has an option for 1.1V internal voltage reference.

Both devices have an option to run the ADC in a "Free Running Mode". But due to that ATmega1281/2561 also has an option to use many other auto trigger sources; the name of the feature enable bit in the control register is different. On ATmega128 it is ADFR (ADC Free Running Select), and on ATmega1281/2561 it is ADATE (ADC Auto Trigger Enable). The default setting of the ADATE is "Free Running Mode".

The internal bandgap reference used in ATmega128 is typical 1.23V, and in ATmega1281/2561 it is 1.1V.

## 12 Analog Comparator

The ACME (Analog Comparator Multiplexer Enable) bit is located in different register bytes in the two devices. In ATmega128 it is located in SFIOR, and in ATmega1281/2561 it is located in ADCSRB.

The internal bandgap reference used in ATmega128 is typical 1.23V, and in ATmega1281/2561 it is 1.1V.





## 13 ATmega103 Compatibility

ATmega128 has a special option for compatibility to ATmega103. ATmega1281/2561 does not have this option.

## 14 Operational Range

**Table 7.** Operating voltage and Speed grades.

	<b>Operating Voltage</b>	<b>Speed Grade</b>
ATmega128	4.5 - 5.5V	0 - 16 MHz
ATmega128L	2.7 - 5.5V	0 - 8 MHz
ATmega1281	2.7 - 5.5V	0 - 8 MHz @ 2.7 - 5.5V 0 - 16MHz @ 4.5 - 5.5V
ATmega2561	4.5 - 5.5V	0 - 16MHz
ATmega1281V/2561V	1.8 - 5.5V	0 - 4 MHz @ 1.8 - 5.5V 0 - 8 MHz @ 2.7 - 5.5V

## 15 ATmega1281 and ATmega2561 packages

Note that the ground paddle size of the ATmega128 and ATmega1281/2561 are different for the MLF packaging type.



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