PIC18F14K22

Oscillator Selection bits:

FOSC = LP	LP oscillator
FOSC = XT	XT oscillator
FOSC = HS	HS oscillator
FOSC = ERCCLKOUT	External RC oscillator, CLKOUT function on OSC2
FOSC = ECCLKOUTH	EC, CLKOUT function on OSC2 (high)
FOSC = ECH	EC (high)
FOSC = ERC	External RC oscillator
FOSC = IRC	Internal RC oscillator
FOSC = IRCCLKOUT	Internal RC oscillator, CLKOUT function on OSC2
FOSC = ECCLKOUTM	EC, CLKOUT function on OSC2 (medium)
FOSC = ECM	EC (medium)
FOSC = ECCLKOUTL	EC, CLKOUT function on OSC2 (low)
FOSC = ECL	EC (low)

4 X PLL Enable bit:

PLLEN = OFF	PLL is under software control
PLLEN = ON	Oscillator multiplied by 4

Primary Clock Enable Bit:

PCLKEN = OFF	Primary clock is under software control
PCLKEN = ON	Primary clock enabled

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRTEN = ON	PWRT enabled
PWRTEN = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)

BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown Out Voltage:

BORV = 30	VBOR set to 3.0 V nominal
BORV = 27	VBOR set to 2.7 V nominal
BORV = 22	VBOR set to 2.2 V nominal
BORV = 19	VBOR set to 1.9 V nominal

Watchdog Timer Enable bit:

WDTEN = OFF	WDT is controlled by SWDTEN bit of the WDTCON register
WDTEN = ON	WDT is always enabled. SWDTEN bit has no effect.

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RA3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled, RA3 input pin disabled

HFINTOSC Fast Start-up bit:

HFOFST = OFF	The system clock is held off until the HFINTOSC is stable.
HFOFST = ON	HFINTOSC starts clocking the CPU without waiting for the oscillator to stablize.

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select Bit:

BBSIZ = OFF	1kW boot block size
BBSIZ = ON	2kW boot block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Code Protection bit:

CP0 = ON	Block 0 code-protected
CP0 = OFF	Block 0 not code-protected

Code Protection bit:

CP1 = ON	Block 1 code-protected
CP1 = OFF	Block 1 not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block code-protected
CPB = OFF	Boot block not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit:

WRT0 = ON	Block 0 write-protected
WRT0 = OFF	Block 0 not write-protected

Write Protection bit:

WRT1 = ON	Block 1 write-protected
WRT1 = OFF	Block 1 not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block write-protected
WRTB = OFF	Boot block not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers write-protected
WRTC = OFF	Configuration registers not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit:

EBTR0 = ON	Block 0 protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 not protected from table reads executed in other blocks

Table Read Protection bit:

EBTR1 = ON	Block 1 protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block protected from table reads executed in other blocks
EBTRB = OFF	Boot block not protected from table reads executed in other blocks

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Help Updated: 08/07/09
13:46:00