

A 500 μ W 5Mbps ULP Super-regenerative RF Front-End

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Abstract—This paper presents an ultra low power super-regenerative RF front-end for wireless body area network (WBAN) applications. The RF front-end operates in the 2.36-2.4 GHz medical BAN and 2.4-2.485 GHz ISM bands, and consumes 500 μ W. It supports OOK modulation at high data rates ranging from 1-5 Mbps. It achieves a sensitivity of -67 dBm at a BER of 10^{-3} . The combination of digital and analog quench generation and RF front-end optimization provides ultra-low power consumption at high data rates. The RF front end is implemented in a 90 nm CMOS technology and is packaged in a QFN56 package.

I. INTRODUCTION

The wireless body area network (WBAN) is a wireless network used for communication among sensor nodes operating on, in or around the human body in order to monitor vital body parameters and movements [1]. Its application to medical scenarios, where various signals are recorded, such as electroencephalography (EEG) or electrocardiography (ECG), highlight the benefits from technological advances. These sensor nodes should sense the signal from the body, perform processing of the sensor signal, and transmit it to a local processing unit. One of the key characteristics of BAN sensors is their autonomous operation. For true energy autonomy, the total energy consumption of a sensor should be minimized. Analysis of the sensor power budget shows that the transceiver is the most power hungry block. A potential candidate to achieve ultra low power wireless communication in BAN is the super-regenerative receiver [2]. Due to its simplicity of design and low power expenditure, it is a commonly employed architecture in sensor networks [3-5]. Nevertheless, these transceivers operate mostly at lower data rates, whereas lifestyle, fitness or entertainment type of applications require the use of high data rates. Recognizing the great market potential and rapid technological developments in this area, a new IEEE 802.15.6 standard is developed which is optimized for low power BAN devices supporting a data rate ranging from 10 kbps up to 10 Mbps.

This work focuses on the implementation of an ultra low power (ULP) super-regenerative RF front-end

operating in the 2.36-2.4 GHz medical BAN [6] and 2.4-2.485 GHz ISM bands. It supports data rates from 1 MHz up to 5 MHz and accommodates the OOK modulation scheme. The receiver is implemented in 90nm CMOS technology and draws 416 μ A at 5 Mbps from a 1.2V supply.

II. SUPER-REGENERATIVE RECEIVER ARCHITECTURE

The super-regenerative principle is based on the variation in start-up time of an oscillator. The oscillator is biased with a time varying quench current [2]. In the presence of an input signal oscillations build up faster. Signal detection is based on the difference in the start-up time which depends on the strength of the input signal. The performance of the super-regenerative receiver in terms of sensitivity and selectivity is determined by the waveform of the quench current. This behavior is analyzed under a sinusoidal, square, triangular and saw-tooth quench wave in [3]. The conclusion is that a saw-tooth waveform provides better selectivity. Following this analysis, the authors in [4] present a quench waveform that further improves the selectivity. In [4] the selectivity is improved by maintaining the oscillator first in the Q-enhancement mode, and after that in the super-regenerative mode. In order to achieve high data rate with low power consumption, some additional improvements are required. In the implemented super-regenerative receivers in [4-5] the data rate is equal to the quench rate. However, the DAC based quench generation requires a high system clock, which is 10 times higher than the quench rate. This constrains the achievable data rate and increases the power consumption.

In this paper, we present a further improvement in case of high data rates. By generating the quench waveform in a combined analog and digital fashion, the proposed ULP receiver achieves both low power consumption and high data rates. The block diagram of the proposed ULP super regenerative receiver RF front-end is shown in Fig. 1. The RF front-end consists of a low-noise amplifier (LNA), an oscillator, a differential to single-ended convertor (DSC), an envelope detector (ED) and the quench waveform generator (QWG). The LNA provides input matching for the antenna, amplification of the RF signal, and it improves

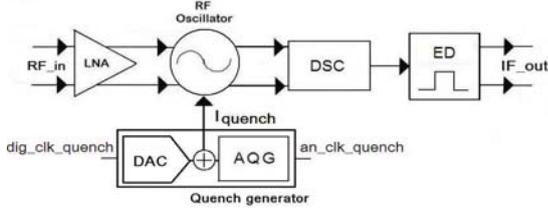


Figure 1. Super-regenerative receiver RF front end architecture

the isolation between the antenna and the oscillator. The oscillator is the main part of the receiver, and operates in the Q-enhancement mode and the super-regenerative mode [4]. The DSC provides the differential to single-ended conversion and the common-mode level suppression of the oscillator. The ED performs the down-conversion of the wanted signal to DC. The QWG provides the time variant quench current for the oscillator. The QWG consists of a DAC and an analog quench generator (AQG). Fig. 2 presents the timing diagram of the quench wave generation. The quench rate is equal to the data rate. The two quench clocks determine the duty-cycle of the current in the digital and analog part of the QWG. By changing the duty cycle of the AQG clock, the oscillator on-time can be controlled. The last plot in Fig. 2 shows the generated quench current. The DAC sets the current one LSB below the critical current. The critical current is the current at which the oscillator will start oscillating. The AQG generates a saw-tooth similar shape.

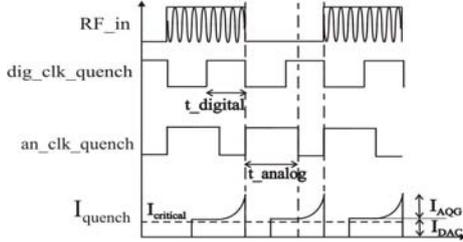


Figure 2. Timing diagram of RF front end

III. CIRCUIT IMPLEMENTATION

In this section, the building blocks composing the ULP radio are discussed.

A. Low-Noise Amplifier and Voltage-Controlled Oscillator

The schematic of the integrated low-noise amplifier (LNA) and the voltage-controlled oscillator (VCO) is shown in Fig. 3. A common source LNA with a capacitive-transformer matching network and a complementary cross-coupled LC oscillator are adopted for the final implementation. The LNA provides the input matching. Also, it improves isolation for the VCO, so that the 50ohm antenna impedance would not load the resonant tank of the VCO and lower the quality factor of the tank. The capacitive-transformer matching network consists of the inductor L_g , and the capacitors C_1 and C_2 [6]. This matching network improves the voltage gain of the LNA. In order to increase the voltage gain of the matching

network, a SMD L_g with high Q is used. The drawback of this type of matching network is the degradation of the noise figure by 3dB compared to methods like inductive degeneration. The transistors $M_{n1} - M_{n4}$ form a standard cascode transconductor. The transistors are biased in moderate inversion in order to minimize the power consumption. The output current of the LNA is directly injected in the LC tank of the VCO, and the LC tank forms the load of the LNA. In order to reduce the power consumption of the oscillator a bondwire inductance is used in the LC tank. The tank capacitance consists of switched MIM capacitors in parallel with a pair of varactors controlled by an analog tuning voltage. To obtain the center frequency, the capacitance will be tuned in the PLL. The complementary cross-coupled pair provides twice the negative conductance compared to a single PMOS or NMOS cross-coupled pair. This reduces the current consumption by half for a given LC tank. The transistor size in the VCO is limited by noise. Actually, the super-regenerative VCO acts as an amplifier. Therefore, the phase noise of the VCO is not critical, but the amplitude noise during the start-up period can affect the start-up of the oscillations. In order to prevent the noise of the VCO from dominating the start-up time of the receiver, g_m provided by $M_{n5} - M_{p8}$ in the VCO must be smaller than g_m provided by $M_{n1} - M_{n2}$ in the LNA.

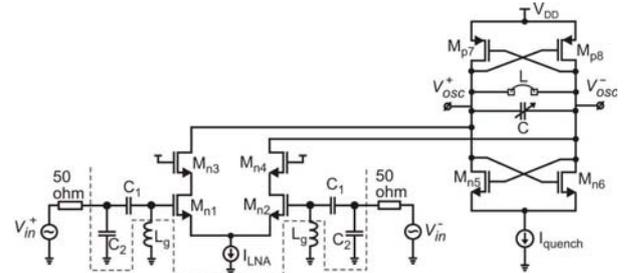


Figure 3. Schematic of the LNA and super-regenerative VCO

B. Differential to single-ended convertor (DSC)

The simplified schematic of the integrated DSC is shown in Fig. 4(a). The DSC is AC coupled to the VCO via the capacitors C_d . It is used as a buffer between the VCO and the ED to suppress the common-mode level of the oscillator that appears due to the time varying quench signal. Since the super-regenerative gain of the VCO is high enough, an additional voltage gain of the DSC is not necessary. Therefore, the bias current, the size of the input NMOS transistors $M_{n1} - M_{n2}$ and the size of the load PMOS transistors $M_{p3} - M_{p4}$ in the DSC are chosen in such way that the voltage gain of the DSC is equal to 1 for a minimal bias current.

C. Envelope detector (ED)

The simplified schematic of the integrated ED is presented in Fig. 4(b). This topology basically is a bandwidth limited source follower [7]. The input transistor M_{n1} in the ED is biased in the weak inversion, and the drain current is an exponential function of the gate-source voltage. The second order component of the drain current generates the wanted baseband DC voltage at the output of

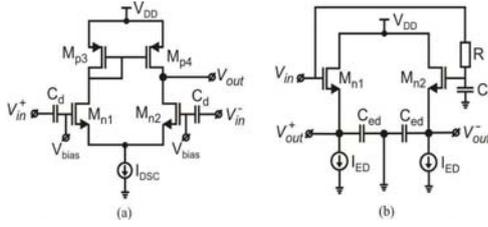


Figure 4. Simplified schematic of: (a) DSC and (b) ED

the ED. The capacitor C_{ED} sets the bandwidth of the ED together with the output impedance of the ED, which is inversely proportional to the transconductance of M_{n1} . The bandwidth of the ED must be high enough to avoid filtering of the detected baseband signal with a given baseband data rate. Since, the super-regenerative RF front-end has been designed to support maximum 5 Mbps data rate, the ED bandwidth has to be 5 MHz. The transistor M_{n2} is an identical device as a part of the replica path. The replica circuit is used to generate a pseudo-differential signal envelope. In the replica path, the RC filter suppresses the high frequency input signal, while the DC level is matched with the DC level at the source of M_{n1} .

D. Quench Wave Generator (QWG)

The QWG consists of the DAC and the analog quench generator (AQG). The schematic of these individual blocks is shown in Fig. 5. Due to the direct connection of the QWG to the oscillator which limits the voltage headroom, the 5-bit DAC employs a simple binary current-mode topology. The DAC provides a current range from $0\mu A$ to $320\mu A$ with a minimum current step size of $10\mu A$. The analog part of the QWG is designed such that a slow rising waveform is produced. Based on a given clock, the voltage over the capacitor grows linearly in time and is shorted to ground at the clock's falling edge, generating a saw tooth voltage waveform. Further control is achieved by the external DC bias current used to charge the capacitor. The waveform is passed to a transconductance stage which performs the current transformation and the exponential waveform generation. The peak amplitude of the current waveform is also made flexible and can be increased in steps of $40\mu A$ by switching on or off individual transistors in the transconductance stage. The peak amplitude ranges from $100\mu A$ - $400\mu A$. Both digital and analog blocks are controlled by an external clock. The quench waveform is generated by superimposing the analog waveform on top of the DAC current.

IV. MEASUREMENT RESULTS

The ULP RF front-end is fabricated in a 90nm CMOS technology with RF/mixed-signal option. The chip micrograph is shown in Fig. 6. The chip occupies 0.8 mm by 1.7 mm including pad-ring and is bonded inside a QFN56 air-cavity package for testing. The packaged chip is placed on a custom designed FR4 PCB board.

Sensitivity and selectivity measurements are carried out. The RF front-end is excited by an OOK modulated signal

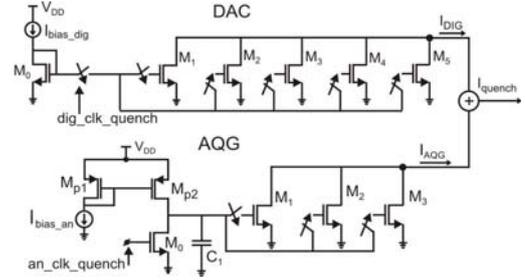


Figure 5. QWG block: DAC and AQG

with the data rate equal to the quench rate. The output transient signal is observed at the ED. In order to evaluate the performance of the receiver, the signal from the oscilloscope is read out by a vector signal analyzer (VSA) program. Fig. 7 shows the transient signal at the output of the envelope detector captured by the VSA program. The input power level is -55 dBm for 3 Mbps and the output voltage level is 21 mV.

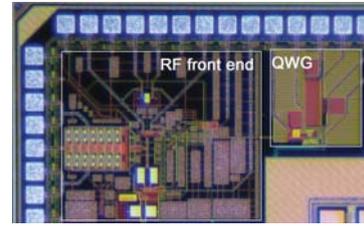


Figure 6. Chip micrograph of the Receiver Front-end

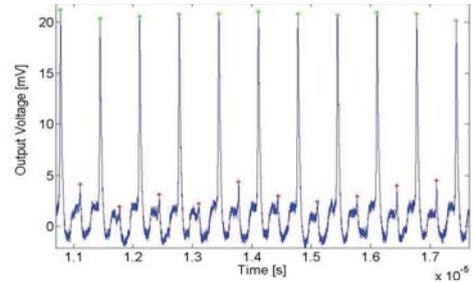


Figure 7. Transient signal at output of ED

For sensitivity measurements, the number of ones and zeros is counted within the 2ms recording time of the VSA program. Afterwards, the probability density functions for zeros and ones are plotted from which the SNR and the bit error rate (BER) are calculated. Fig. 8 shows the resulting receiver sensitivity where the BER is plotted as a function of the input power level for 1,3,5 Mbps data rate. The BER results for the various data/quench rates are quite similar. In the measurement, the quench shape is constant for all three data rates, i.e. the duty cycle of the analog and digital quench clocks is the same. Therefore, the noise level in the oscillator is constant since the oscillator current is the same at the different quench rates. Further, the bandwidth of the ED is not changed, therefore the SNR of signal remains constant. The overall RF front-end performance is achieved at a DC power consumption of $310\mu A$ for 1 MHz, $356\mu A$ for 3 MHz, and $412\mu A$ for 5 MHz. At higher data rate, the current is higher due to the shorter "off" period of the

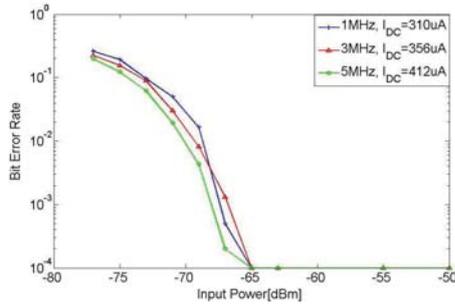


Figure 8. BER versus of input power for various data/quench rates

quench current. For a BER of 10^{-3} , the achieved sensitivity is -67 dBm. The system level measurements incorporating this front-end are presented in [8]. By using oversampling, a sensitivity of -72 dBm is achieved at 1 Mbps with 3 MHz quench rate.

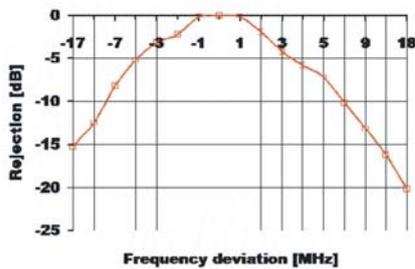


Figure 9. Signal rejection at 2.4 GHz central frequency

Fig. 9 shows the signal rejection measurement of the RF front end. The oscillator is not quenched and is biased with a constant current which is one LSB below the critical current. In this case, the RF front-end works in the Q-enhancement mode. The RF front-end is excited by a single test tone. The frequency is swept around the operating frequency. The output level of the oscillator is measured on the spectrum analyzer. In practice, the signal rejection differs due to the time variance of the quench current. The rejection -10 dB at 11 MHz and can be improved by decreasing the current step-size of the DAC in the QWG.

Fig. 10 shows the selectivity measurement of the RF front end. The BER is calculated by observing the transient signal at the ED output, while the carrier frequency is swept around the operating frequency of the RF front-end. As the carrier frequency is shifted from the operating frequency, the BER will deteriorate. The selectivity result is similar for the different data/quench rates. The bandwidth around the central frequency for which the BER is less than 10^{-3} is 11 MHz.

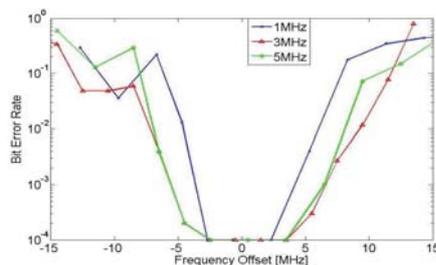


Figure 10. Front-end selectivity

As shown in Table I, this implementation achieves state of the art performance in terms of low sensitivity for high data rate. It has to be noted that the power consumption of the receivers in [3-5] includes the analog and digital base-band. However, this work shows only the RF front-end. Since the RF front-end is the most power hungry block in the receiver, it can be assumed the analog and digital base band will not dramatically increase the power consumption.

TABLE I COMPARISON WITH STATE OF THE ART ULP RECEIVERS

Ref	Technology	Freq. (GHz)	Selectivity	Sensitivity (dBm)	Data rate (Mbps)	Power (mW)
This work	CMOS 90	2.4	10MHz @-10dB	-67	5	0.5@ 1.2 V (RF front end)
[3]	CMOS 0.35	1	150kHz @-5dB	-107.5	0.1	1.2@ 1.5V (RF front-end+ analog BB)
[4]	CMOS 0.13	2.4	900kHz @-3dB	-60	1	2.8@ 1.2V (total receiver)
[5]	CMOS 0.13	5	10MHz @-30dB	-60	1.2	6.6@ 1.2V (total receiver)

V. CONCLUSIONS

An ultra low power super-regenerative RF front-end is presented in this paper. The proposed RF front-end integrates the analog and digital quench generation on chip. Along with RF front-end optimization, low power consumption and high data rate are achieved. It supports OOK modulation at high data rates ranging from 1-5 Mbps. The RF front-end consumes 500 μ W and achieves a sensitivity of -67 dBm at 5 Mbps.

ACKNOWLEDGMENT

The authors acknowledge the discussions held with other group members such as Cui Zhou, Li Huang, Xiaoyan Wang, and Kathleen Philips.

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