Journal of the Korean Physical Society, Vol. 49, No. 2, August 2006, pp. 642∼645

Some Physical Properties of a Surrounding-Gate MOSFET with Undoped Body

Guang-Xi Hu* and Ting-Ao Tang

State Key Laboratory of ASIC & System, Fudan University, Shanghai 200433, P.R. China and School of Microelectronics, Fudan University, Shanghai 200433, P.R. China

(Received 15 February 2006)

A kind of Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) with a surrounding gate is presented. Some physical properties of the MOSFET are obtained by solving Poisson's equation analytically. We propose a new criteria for the threshold voltage, and the threshold voltage is obtained in due course. The threshold voltage of a surrounding-gate nMOSFET is influenced by the thickness of the oxide and the radius of the cylinder. It's also influenced by the work function difference between the gate electrode and intrinsic silicon. A MOSFET with a thinner oxide or a smaller radius will have a higher threshold voltage. We can obtain a desirable threshold voltage by choosing the right material for the gate and the right size for the MOSFET.

PACS numbers: 85.30.-p, 02.60.Cb
Keywords: MOSFETs, Semiconductor devices, Transistors

I. INTRODUCTION

According to Moore's law [1], the number of transistors on a single silicon chip will increase continually, and the transistor scale will decrease as indicated in the International Roadmap for Semiconductors (ITRS-2000) [2]. In the year 2000, Je *et al.* fabricated a quantum wire transistor with a width of only 65 nm [3]. As the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is continuing to scale down, gate oxide tunneling is becoming an important factor, and a double-gate MOSFET has been proposed and studied to reduce this effect [4–6]. The evenly doped surrounding-gate (SG) MOSFET has been proposed and some of its physical properties have been obtained [7–10]. The undoped or lightly doped SG MOSFET has also been proposed and studied to some extent, and some physical properties, such as the current through the device and the I-V characteristics, have been obtained [11–13].

To understand the undoped SG MOSFET better, we study some physical properties of the MOSFET, and those properties can be of great help in the Ultra Large Scale Integrated-circuit (ULSI) design. The surface potential, the sheet density of mobile charge, and the threshold voltage of the MOSFET are obtained by solving Poisson's equation analytically in cylindrical coordinates. The source (drain) can either be on the top or the bottom of the cylinder.

The shape of the MOSFET is cylindrical. The band diagrams of an nMOSFET with a cylindrical shape are shown in Fig. 1. The thickness of the oxide is t_{ox}, and the radius of the cylinder is a. The material for the gate can either be metal or heavily doped polysilicon. Fig. 1 (c) shows a sketch of the cylindrical coordinates.

For an undoped or lightly doped body, the Poisson's equation in cylindrical coordinates is

$$\frac{d^2\psi}{d\rho^2} + \frac{1}{\rho}\frac{d\psi}{d\rho} + \frac{d^2\psi}{dz^2} + \frac{1}{\rho^2}\frac{d^2\psi}{d\varphi^2} = \frac{qn_i}{\varepsilon_{si}} e^{q\psi/kT}, \qquad (1)$$

where q is the electronic charge, k is Boltzmann's constant, T is the temperature, n_i is the intrinsic carrier

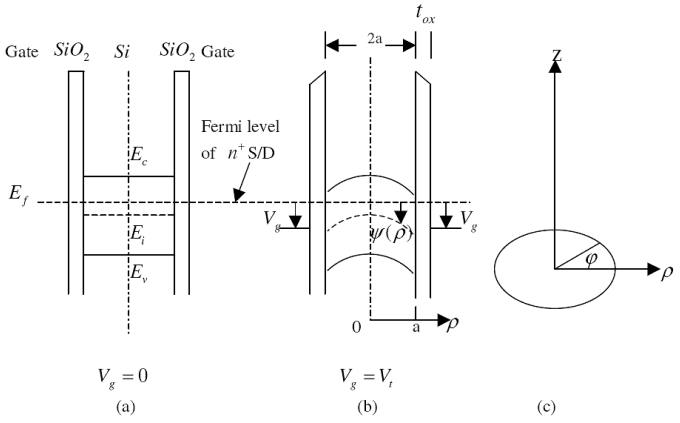

Fig. 1. (a) Schematic band diagram of a surrounding-gate nMOSFET at zero gate voltage. (b) Schematic band diagram of a surrounding-gate nMOSFET near the threshold voltage. (c) Sketch of cylindrical coordinates.

*E-mail: gxhu@fudan.edu.cn

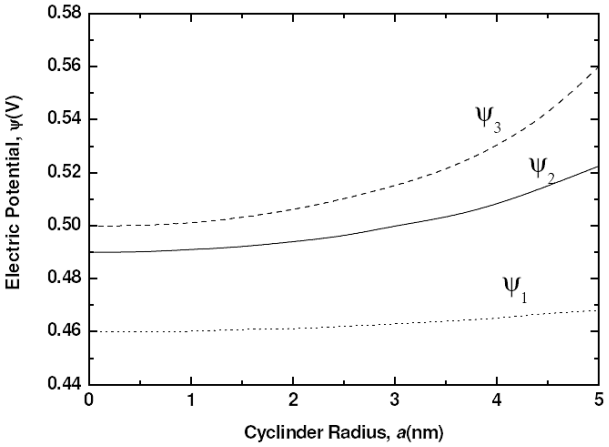

Fig. 2. Potential ψ as a function of position in the silicon body. The corresponding gate voltages $(V_g - \phi_{ms})$ are 0.558 V for ψ_1, 0.632 V for ψ_2, and 0.835 V for ψ_3.

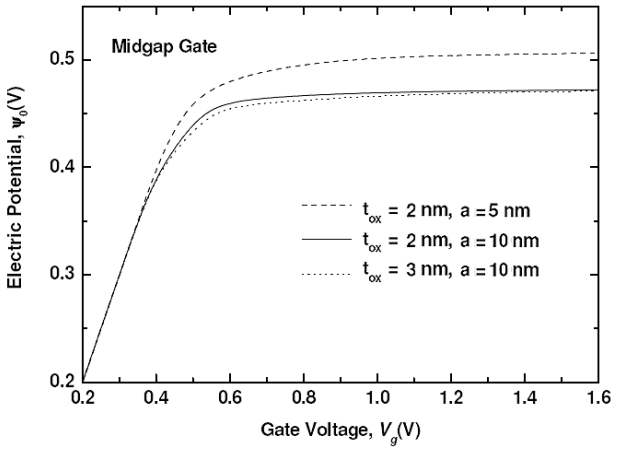

Fig. 3. Electric potential at $\rho = 0$ (ψ_0) for different nMOSFETs. The dashed line is for $t_{ox} = 2$ nm and $a = 5$ nm. The solid line is for $t_{ox} = 2$ nm and $a = 10$ nm. The dotted line is for $t_{ox} = 3$ nm and $a = 10$ nm. $\phi_{ms} = 0$ is assumed.

density, and ε_{si} is the permittivity of silicon. For simplicity, we assume that the height of the cylinder is much larger than the radius and that ψ is independent of z. With consideration of the symmetry of φ, Eq. (1) is simplified as

$$\frac{d^2\psi}{d\rho^2} + \frac{1}{\rho}\frac{d\psi}{d\rho} = \frac{qn_i}{\varepsilon_{si}} e^{q\psi/kT}. \tag{2}$$

The boundary conditions are as follows

$$\left.\frac{d\psi}{d\rho}\right|_{\rho=0} = 0, \tag{3}$$

$$\varepsilon_{si}\left.\frac{d\psi}{d\rho}\right|_{\rho=a} = c_{ox}\left(V_g - \phi_{ms} - \psi_s\right). \tag{4}$$

We have assumed that for an nMOSFET with $q\psi/kT \gg 1$, the hole density can be neglected.

$$c_{ox} = \frac{\varepsilon_{ox}}{a\ln\left(1 + t_{ox}/a\right)}$$

is the capacitance of the oxide.

The analytical solution to Eq. (2) is [12–14]

$$\psi = \psi_0 - \frac{2kT}{q}\ln\left(B\rho^2 + 1\right), \tag{5}$$

where B is given by [12]

$$B = -\frac{q^2 n_i}{8kT\varepsilon_{si}}\exp\left(\frac{q\psi_0}{kT}\right), \tag{6}$$

and ψ_0 is the potential at the origin of the cylinder. The potential at the surface ψ_s will be obtained as follow

$$\begin{aligned}\psi_s = \psi\Big|_{\rho=a} &= \psi_0 - \frac{2kT}{q}\ln\left(Ba^2 + 1\right) \\ &= \psi_0 - \frac{2kT}{q}\ln\left[1 - \frac{a^2q^2n_i}{8kT\varepsilon_{si}}\exp\left(\frac{q\psi_0}{kT}\right)\right]\end{aligned} \tag{7}$$

As we know from the above equation,

$$1 - \frac{a^2q^2n_i}{8kT\varepsilon_{si}}\exp\left(\frac{q\psi_0}{kT}\right) > 0$$

and

$$\psi_0 < \frac{kT}{q}\ln\frac{8kT\varepsilon_{si}}{a^2q^2n_i}. \tag{8}$$

From Eqs. (4) and (5), we have

$$\begin{aligned}&c_{ox}\left(V_g - \phi_{ms} - \psi_s\right) \\ &\quad = \frac{2kT\varepsilon_{si}}{qa}\left[\sqrt{1 + \frac{a^2q^2n_i}{2kT\varepsilon_{si}}\exp\left(\frac{q\psi_s}{kT}\right)} - 1\right].\end{aligned} \tag{9}$$

II. PHYSICAL PROPERTIES OF A SURROUNDING-GATE MOSFET

With Eqs. (5), (7), and (9), one can easily do the numerical calculations. In Fig. 2, we show the potential ψ versus position ρ. The parameters are $t_{ox} = 2$ nm, and $a = 5$ nm. ψ_1, ψ_2, and ψ_3 correspond to $V_{g1} - \phi_{ms} = 0.558$ V, $V_{g2} - \phi_{ms} = 0.632$ V, and $V_{g3} - \phi_{ms} = 0.835$ V, respectively. ϕ_{ms} is the work function difference between the gate electrode and intrinsic silicon. $\phi_{ms} = 0$ for a midgap work function gate, $-E_g/2q$ for n^+ poly, and $E_g/2q$ for p^+ poly. ψ_1 shows the property that below the threshold voltage (about 0.55 V), the potential ψ is almost the same as ψ_0 and changes little with the position ρ.

Fig. 3 shows the potential ψ_0 versus gate voltage V_g, where $\phi_{ms} = 0$ is assumed. From the figure, we can see that when the gate voltage is below the threshold voltage, the potential ψ_0 changes almost linearly with the gate voltage. When the gate voltage is above the threshold

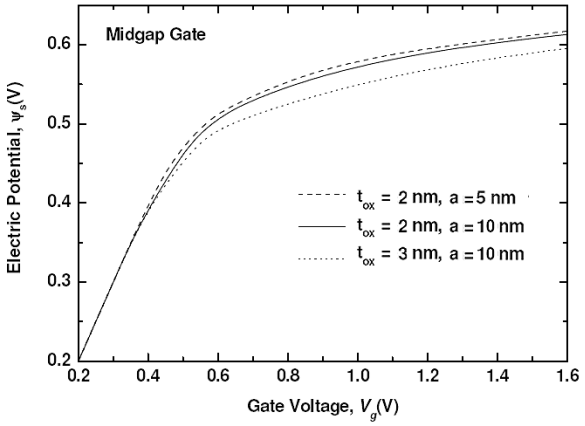

Fig. 4. Electric potential at $\rho = a$ (ψ_s) for different nMOSFETs. The dashed line is for $t_{ox} = 2$ nm and $a = 5$ nm. The solid line is for $t_{ox} = 2$ nm and $a = 10$ nm. The dotted line is for $t_{ox} = 3$ nm and $a = 10$ nm. $\phi_{ms} = 0$ is assumed.

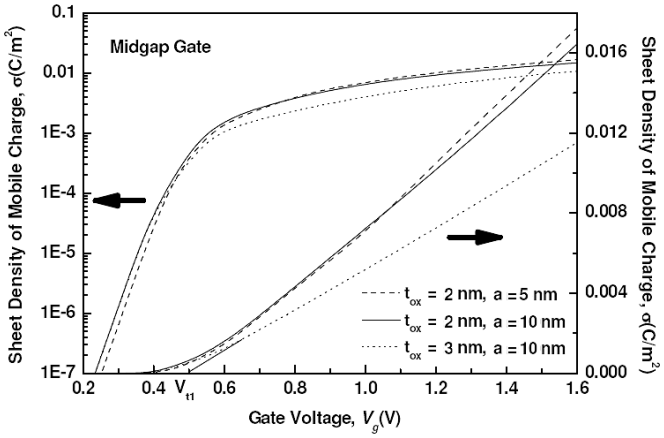

Fig. 5. Sheet density of mobile charge, $\sigma = \varepsilon_{si}\,(d\psi/d\rho)_{\rho=a}$, of surround-gate nMOSFETs on both logarithmic and linear scales versus gate voltage. $\phi_{ms} = 0$ is assumed. The threshold voltages are obtained by extrapolating the linear parts of the curves. V_{t_1} corresponds to $t_{ox} = 3$ nm and $a = 10$ nm.

voltage, ψ_0 changes little with gate voltage and seems to be pinned at an upper bound $\psi_{0\,\max}$. Actually, from Eq. (8), we have

$$\psi_{0\,\max} = \frac{kT}{q} \ln \frac{8kT\varepsilon_{si}}{a^2 q^2 n_i}. \tag{10}$$

In a symmetric double-gate case [4], ψ_0 is pinned to an upper bound of $(kT/q)\ln\left(2\pi^2\varepsilon_{si}kT/q^2 n_i W^2\right)$, where W is the distance between the two gates.

Fig. 4 shows the surface potential ψ_s versus gate voltage. With Eq. (9), one obtains the numerical results. ψ_s seems to be more sensitive to the thickness of the oxide than to the radius of the cylinder. ψ_s will have a larger value for a thinner oxide.

Fig. 5 shows the sheet density of mobile charge, σ, versus gate voltage V_g. From electrodynamics, we know that

$$\sigma = \varepsilon_{si} \left.\frac{d\psi}{d\rho}\right|_{\rho=a} = \frac{2kT\varepsilon_{si}}{qa}\left[\sqrt{1 + \frac{a^2 q^2 n_i}{2kT\varepsilon_{si}} \exp\left(\frac{q\psi_s}{kT}\right)} - 1\right]. \tag{11}$$

When the gate voltage is smaller than the threshold voltage (about 0.55 V), the total inversion charge density increases exponentially with V_g (see the left curves in Fig. 5). The rate of increase is about 12.5 decade/V. When the gate voltage is larger than the threshold voltage, σ increases with V_g linearly (see the right curves in Fig. 5).

III. THRESHOLD VOLTAGE

Since the silicon body is undoped or lightly doped, we define the threshold voltage as the voltage at which the extrapolated intercept of the linear portion of the $\sigma(V_g)$ curve meets the V_g-axis. This definition is consistent with traditional definitions. Generally speaking, the threshold voltage V_g is determined by plotting I_{ds} (electric current from the source to the drain) versus V_g at low drain voltages. The extrapolated intercept of the linear portion of the $I_{ds}(V_g)$ curve with the V_g-axis will give the value of V_t [15]. The current from the source to the drain I_{ds} is almost proportional to the sheet density of the mobile charge σ, which will establish the validity of the threshold voltage definition given in this paper. By this definition, when the gate voltage is above the threshold voltage, the current from the source to the drain will increase linearly with gate voltage, too.

With the above definition, we obtain from Fig. 5 that V_{t_1} is about 0.50 V for a MOSFET with $t_{ox} = 3$ nm and $a = 10$ nm, V_{t_2} is about 0.54 V for a MOSFET with $t_{ox} = 2$ nm and $a = 10$ nm, and V_{t_3} is about 0.58 V for a MOSFET with $t_{ox} = 2$ nm and $a = 5$ nm. $\phi_{ms} = 0$ is assumed. V_{t_2} and V_{t_3} are not shown in the figure. Taking ϕ_{ms} into account will shift the threshold voltage upwards ϕ_{ms} ($\phi_{ms} > 0$) or downwards $|\phi_{ms}|$ ($\phi_{ms} < 0$).

IV. DISCUSSION AND CONCLUDING REMARKS

So far, we have obtained some interesting results for a surrounding-gate nMOSFET based on analytical solutions.

i) The threshold voltage of a surrounding-gate nMOSFET is influenced by the thickness of the oxide and the radius of the cylinder. A MOSFET with a thinner oxide or a smaller radius will have a higher threshold voltage. We can obtain a desired

threshold voltage by choosing the right material for the gate.

ii) The potential at the origin of the cylinder, ψ_0, is more sensitive to the radius a than to the thickness of the oxide t_{ox} while the potential at the surface of the silicon, ψ_s, is more sensitive to the thickness of the oxide t_{ox} than to the radius a.

iii) One important physical effect not studied in the paper is the inversion layer quantum effect, which will shift the peak electron concentration away from the oxide interface toward the center of the silicon body. For a double-gate MOSFET, the effect won't influence the results too much [4]. Future research should be done on the quantum effect in a surrounding-gate MOSFET.

ACKNOWLEDGMENTS

Helpful discussions with Profs. M. F. Li and L. K. Wang are acknowledged.

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