Possibility of Transport Through a Single Acceptor in a Gate-All-Around Silicon Nanowire PMOSFET

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***Abstract*—Temperature-dependent electrical transport measurements of cylindrical shaped gate-all-around silicon nanowire p-channel MOSFET were performed. At 4.2 K, they show current oscillations, which can be analyzed by single hole tunneling originated from nanowire quantum dots. In addition to this single hole tunneling, one device exhibited strong current peaks, surviving even at room temperature. The separations between these current peaks corresponded to the energy of 25 and 26 meV. These values were consistent with the sum of the bound-state energy spacing and the charging energy of a single boron atom. The radius calculated from the obtained single-atom charging energy was also comparable to the light-hole Bohr radius.**

***Index Terms*—Gate-all-around (GAA), silicon nanowire FET (SNWFET), single-acceptor atom, temperature dependence.**

I. Introduction

RAPID scaling of MOSFETs has led us into a regime where counting individual dopants (donors and acceptors) [1]–[3] as well as individual oxide charges [4] is important in determining the threshold voltage of each device. The threshold voltage is not the quantity determined from the average doping density any more, and there is an appreciable device-to-device fluctuation due to irregular distribution of individual dopants. As the device size becomes even smaller, we encounter a device whose characteristic is determined completely by the existence of a single impurity in the channel. Recently, various transport studies regarding such single-dopant effects have been reported [5]–[8]. In the case of nanowire devices, a single impurity in the channel will also strongly affect the characteristics of the whole device because the impurity, no matter where it exists in the length direction, can easily influence the entire current flow.

Gate-all-around (GAA) silicon nanowire FET (SNWFET) is considered as an ideal candidate among the devices with 3-D electric field control [9]. Previously, we reported the characteristics of twin SNWFETs fabricated by using full CMOS processes [10]. Low-temperature (T) characterization of these devices exhibited interesting single-electron tunneling [11] and shell filling behaviors [12]. However, so far, the effect of single dopant on these GAA structure has rarely been reported. In this paper, we report the evidence of single-impurity dominant transport in a GAA SNW PMOS (p-channel MOS) FET fabricated by similar CMOS processes. We performed systematic T-dependence studies of the transport characteristics, and we observed anomalous current peaks from one of the devices. We analyzed these peaks in terms of the evidence of transport through single-acceptor states.

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II. Device Fabrications

Fig. 1 shows the detailed fabrication procedures of our GAA SNW PMOSFETs [10]. The description of the processes is also summarized in the figure. A cylindrical SNW with the radius (r) of 5 nm and the length (L) of 60 nm is bridging the source and the drain contacts, and it is fully surrounded by a 3.5-nm SiO_2 and a TiN gate. The H_2 trimming after the etching of the sacrificial SiGe layer results in circular cross sections with smooth surface [10]. The penetration of the implanted dopants during the postimplantation heat treatments creates p regions on both ends of the SNW. The discrete dopants that can become the source of the single-dopant transport are the residual boron atoms diffused further into the middle of the channel from this p region [see Fig. 1(e)]. Our nanowire is only unintentionally doped during the epitaxy, and the average concentration of the impurities introduced during epitaxy is expected to be much smaller than the concentration of the outdiffused dopants. Therefore, the chance for the impurities originated from the epitaxial growth to participate in the transport can be negligible.

III. Results and Discussions

Fig. 2(a) and (b) shows a typical room temperature T, drain current–gate voltage (I_{DS}–V_{GS}, in log scale) and drain

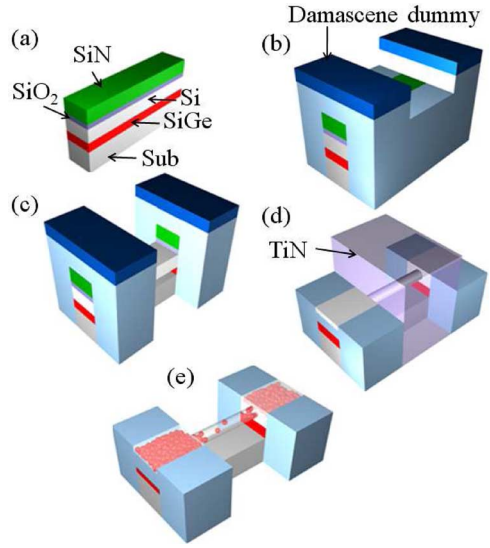

Fig. 1. Fabrication procedures of our GAA SNW PMOSFET. (a) Epitaxial growth of sacrificial SiGe and active silicon layer, SiN hard mask deposition and trimming, etching for shallow trench isolation. (b) Trench oxide fill, Damascene dummy deposition, and Damascene process for SiN hard mask opening. (c) Field oxide recess and removal of SiGe layer. (d) H_2 annealing for trimming of SNW, gate oxidation, TiN gate filling, blocking layer formation, and ion implantation. (e) Schematic dopant distribution in the SNW.

current–drain voltage (I_{DS}–V_{DS}, in linear scale) characteristic, respectively, measured from one of the SNW PMOSFETs. The drain-induced barrier lowering, subthreshold swing, and ON–OFF current ratio from these characteristics are 27.3 mV/V, 73 mV/decade, and more than 10^4, respectively. As shown in Fig. 2(b), there are no kinks in the saturation region, which indicates that the channel of the nanowire is fully depleted [13].

We obtained the low-T characteristics of several SNW PMOSFETs fabricated in the same batch. At low T, we usually observe regular current oscillations, which are originated from single hole tunneling of the quantum dot defined by the gate-bias-induced band bending of the p source/lightly doped nanowire/p drain [12], [14], [15] [also see the band diagram of Fig. 5(b)]. Fig. 3(a) shows the I_{DS}–V_{GS} measured from one device (device A) at $T = 4.2$ K. This device exhibits unexpected behaviors. Near the turn-ON region of the device ($-0.8 < V_{GS} < -0.5$ V), it exhibits strong current peaks whose shapes are almost triangular. Their shape is different from other regular Coulomb oscillation peaks in the region $V_{GS} < -0.8$ V. The shapes of the first and the second peak (denoted by I1 and J1) are almost independent of the value of V_{DS}. Fig. 3(b) shows the T-dependence of these anomalous current peaks at low V_{DS} (-500 μV). The current peaks are merged into a single large peak at $T = 50$ K, and it persists even at room T. The circled regions at $T = 80$, 110, and 280 K show the slopes that are different from those of other T's. They could be originated from oxide charge instabilities. However, they do not affect the peak structures that are the main focus of this paper.

Fig. 4(a) shows the 4.2 K contour plots of dI_{DS}/dV_{DS} in the V_{DS}–V_{GS} planes measured from device A with anomalous peaks. Fig. 4(b) shows the 4.2 K contour plots of dI_{DS}/dV_{DS}

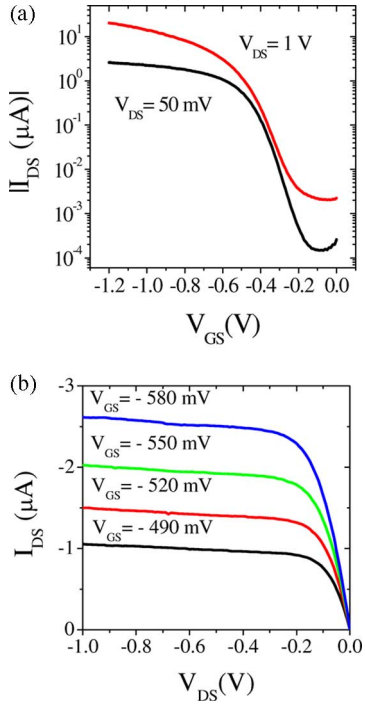

Fig. 2. (a) I_{DS}–V_{GS} (log scale) and (b) I_{DS}–V_{DS} (linear scale) characteristics of a typical SNW PMOSFET measured at room temperature. They show clear PMOS behavior with reasonable subthreshold swing and ON–OFF ratio.

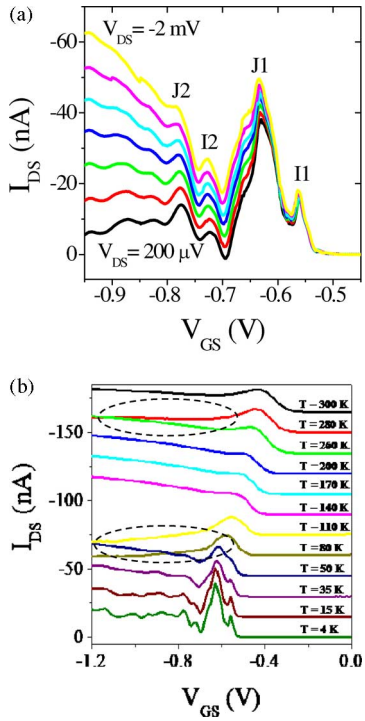

Fig. 3. (a) I_{DS}–V_{GS} at various V_{DS} values measured from one of our SNW PMOSFETs (device A). Data were taken at $T = 4.2$ K. Four anomalous peaks are observed (denoted as I1, I2, J1, and J2). (b) I_{DS}–V_{GS} measured from the same device at several different Ts. $V_{DS} = 500$ μV. The current peak structure survives even at $T = 300$ K.

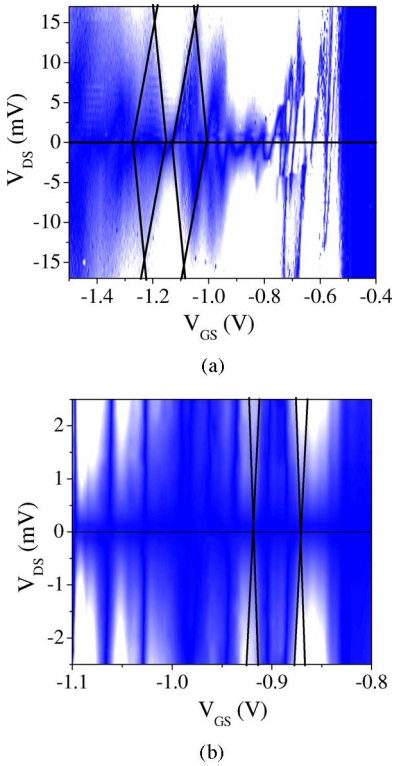

Fig. 4. V_{GS}–V_{DS} contour plots of dI_{DS}/dV_{DS} measured at 4.2 K. (a) Device A. (b) Device B. The solid lines denote the single hole tunneling Coulomb diamond from which the capacitance values are extracted.

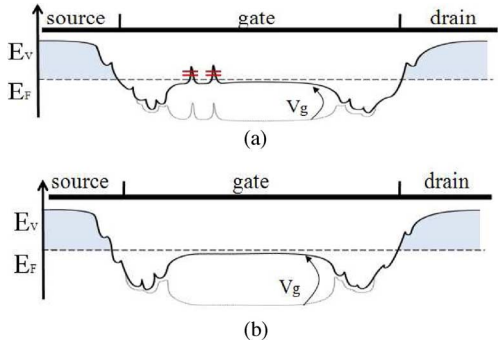

Fig. 5. Schematic band diagram (valence band edges). (a) Device A. (b) Device B. Single hole tunneling occurs through the bound states of the individual boron atoms (denoted by red bars), resulting in anomalous current peaks.

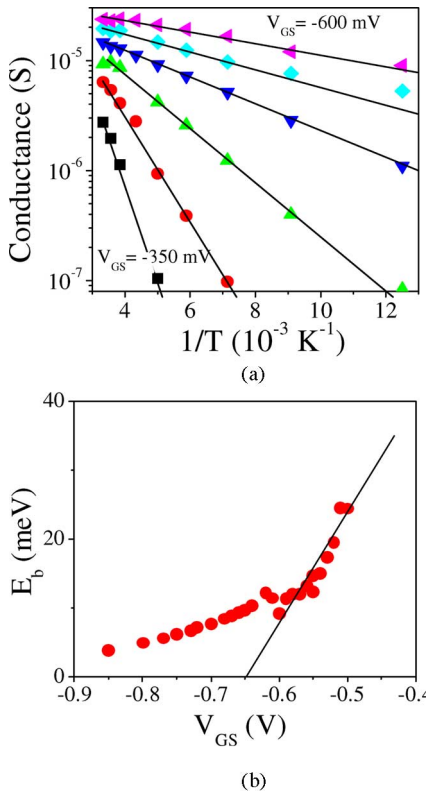

Fig. 6. (a) Activation plots of the conductance at various V_{GS} values. (b) Activation energy E_b versus V_{GS}. The extrapolation gives the threshold voltage of -0.65 V. It suggests that the tunneling through the bound states occurs right after turn-ON.

in the V_{DS}–V_{GS} planes measured from a normal device (device B). Device B of Fig. 4(b) shows clear Coulomb diamonds that are symmetric against the V_{DS} axis, and it also shows almost periodic oscillations in V_{GS}. However, the diamonds of device A of Fig. 4(a) are strongly asymmetric and the period of the oscillations is irregular, especially in the range $-0.8\ \text{V} < V_{GS} < -0.6\ \text{V}$.

We interpret the strong asymmetric peak of device A as the evidence of transport through single-acceptor impurities in the channel. Assuming the diffusion of semi-infinite solid and using the doping concentration in the center of the nanowire ($L/2$), the average number of impurities (N) in the nanowire channel is estimated by the following formula:

$$N = \pi r^2 (L - 30\ \text{nm}) C_s \left[1 - \text{erf}\left(\frac{L}{4\sqrt{Dt}}\right)\right]$$

where C_s, D, and t are the doping concentration of the implanted source/drain region, diffusion constant, and total time of diffusion, respectively. Here, we use the penetration depth (the length of the p region in the SNW) of 15 nm [12]. The total heat budget after boron ion implantation of the source and the drain region is 800 °C for $t = 10$ min. It is difficult to exactly know the value of C_s, and we assume the worst case of 10^{19} cm^{-3}. With the D value of $\sim 10^{-15}$ cm^2/s (at 800 °C), $N \approx 0.25$. The estimated number of diffused dopants in the channel is consistent with the fact that the anomalous peaks occur only in one device. We analyze the data in the same line as [5]. Fig. 5 shows schematic band diagrams (valence band edges) of devices A and B. Both band diagrams show nanowire quantum dot with two tunnel barriers, which are formed from the gate-induced band bending of the lightly doped nanowire and the heavily doped source/drain junctions. The band diagram of device A shows two discrete impurities. The ground and the excited states of each impurity are denoted as thick lines. The four peaks denoted as I1, I2, J1, and J2 in Fig. 3(a) are tunneling through these bound states of two discrete impurities in the channel. Fig. 6(a) shows the activation plot of the low V_{DS} conductance obtained from the T-dependence in the range $-350\ \text{mV} < V_{GS} < -600\ \text{mV}$. Fig. 6(b) plots the obtained activation energy E_b as a function of V_{GS}. The extrapolation gives the threshold voltage of

-0.65 V. All the peaks in Fig. 3(a) are near this threshold voltage. The current peak near the threshold voltage occurs only when the Fermi level (E_F) of the source region is aligned with the bound states of the single acceptor. The discrete acceptors probably exist near the source barrier so that the tunneling into the acceptor can result in large current peaks.

The coupling capacitances were obtained from the analysis of the Coulomb diamonds in Fig. 4 (in the entire range of V_{GS} for device B and $V_{GS} < -0.8$ V for device A). The slopes used for the estimation of the capacitances are drawn in the figure. Device A had the gate capacitance $C_G = 1.24$ aF, the source capacitance $C_S = 0.65$ aF, and the drain capacitance $C_D = 6.39$ aF, and $\alpha = 0.15$. Device B had $C_G = 1.95$ aF, $C_S = 0.63$ aF, and $C_D = 8.7$ aF, and $\alpha = 0.17$. The parameters of one device are in agreement with those of another device within 20%, suggesting that the observed single hole tunneling was originated from the same quantum dots defined by the source and drain doping [12].

Using these parameters, the gate conversion factor $\alpha = qC_G/(C_G + C_S + C_D) \approx 0.17$ (eV/V) can be obtained where q is the hole charge. This α value is also consistent with $dE_b/dV_{GS} \approx 0.16$ eV/V obtained from the solid line of Fig. 6(b). The separation between the peak positions, I1 and I2 (J1 and J2) in V_{GS}, is then converted to 25.4 meV (26.4 meV). The typical energy spacing between the bound states of boron is approximately 5 meV [14]. The Coulomb charging energy of the single acceptor is the observed energy spacing minus this bound-state energy spacing of 5 meV (resulting in 20 meV). The amount of 20 meV corresponds to the spherical dot with the radius of 3 nm if we assume the capacitance of a sphere ($4\pi\varepsilon r$, where ε is the dielectric constant of silicon and r is the radius of the dot). The obtained radius is in agreement with the Bohr radius of a light hole [$(\varepsilon\hbar^2)/(m^*q^2) = 3.9$ nm] whose effective mass m^* is 0.16 times the free electron mass.

IV. Conclusion

We performed temperature-dependent transport measurements of cylindrical-shaped GAA SNW PMOSFETs. Single hole tunneling behaviors were observed at 4.2 K, and one of the devices exhibited anomalously strong current peaks, which survived even at room temperature. The separation between two peaks with identical shapes corresponded to the energy of 25–26 meV. This value was consistent with the sum of the bound-state energy spacing of boron atom and the single-hole charging energy of a dot with 3 nm radius. This radius is also comparable to the Bohr radius of a single-acceptor atom when the light hole effective mass is used.

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