

SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

SDLS004

D2633, JANUARY 1981 — REVISED MARCH 1988

- Parallel Register Inputs ('LS592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('LS593)
- Counter has Direct Overriding Load and Clear
- Accurate Counter Frequency: DC to 20 MHz

description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. A low-going \overline{RCO} pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to CCK of the following stage.

The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs. The tables below show the operation of the enable (CCKEN, \overline{CCKEN}) inputs. A register clock enable (RCKEN) is also provided.

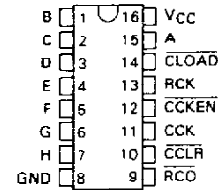
OUTPUT ENABLE CONTROL ('593 ONLY)

G	\overline{G}	A/Q _A thru H/Q _H
L	L	input mode
L	H	input mode
H	L	output mode
H	H	input mode

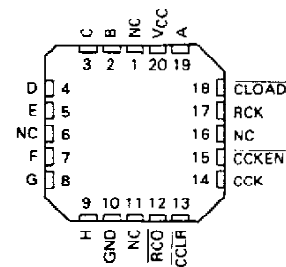
COUNTER CLOCK ENABLE CONTROL

CCKEN	\overline{CCKEN}	EFFECT ON CCK
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

SN54LS592 . . . J OR W PACKAGE SN74LS592 . . . N PACKAGE (TOP VIEW)

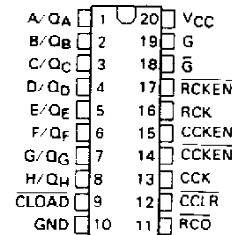


SN54LS592 . . . FK PACKAGE (TOP VIEW)

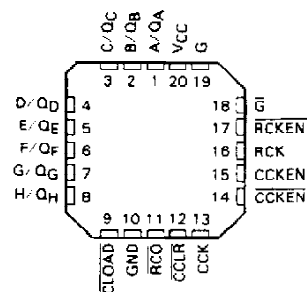


NC — No internal connection

SN54LS593 . . . J OR W PACKAGE SN74LS593 . . . DW OR N PACKAGE (TOP VIEW)



SN54LS593 . . . FK PACKAGE (TOP VIEW)



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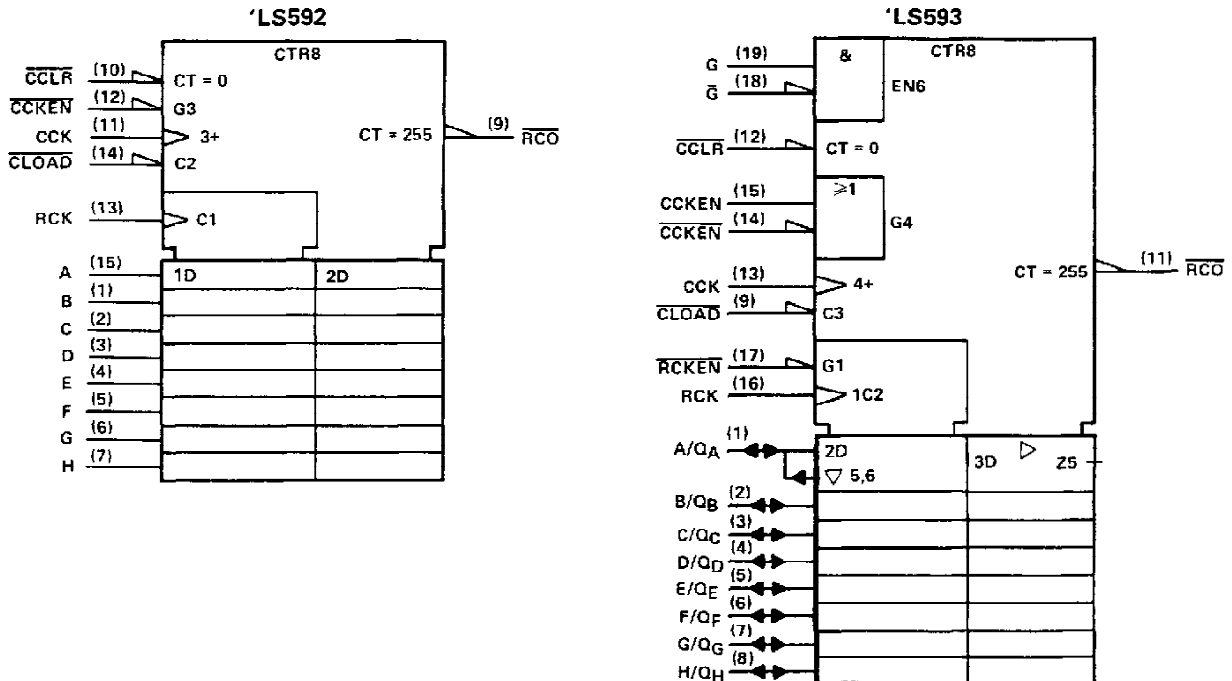
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schematics of inputs and outputs



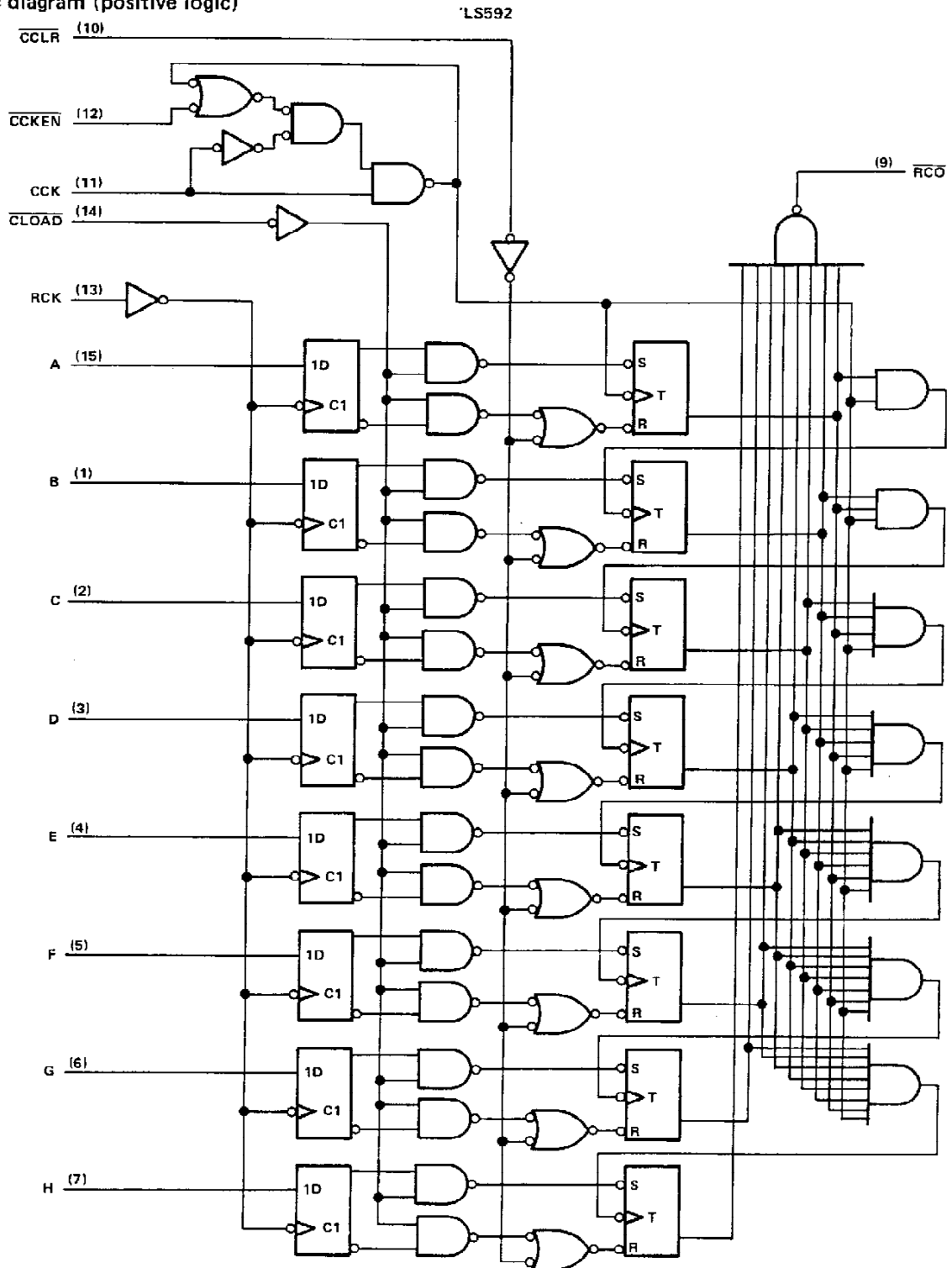
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

SN54LS592, SN74LS592 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)

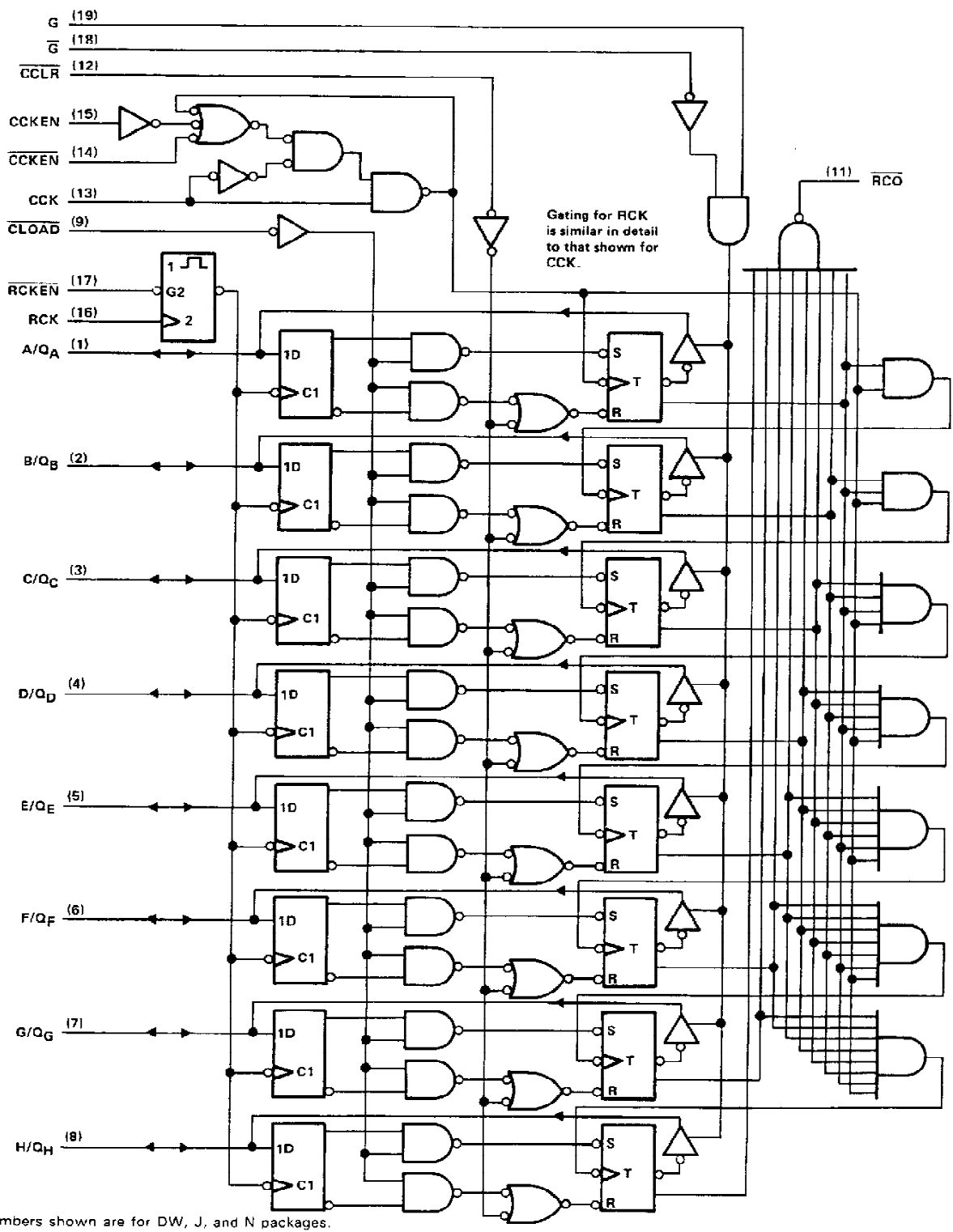


Pin numbers shown are for J, N, and W packages.

SN54LS593, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)

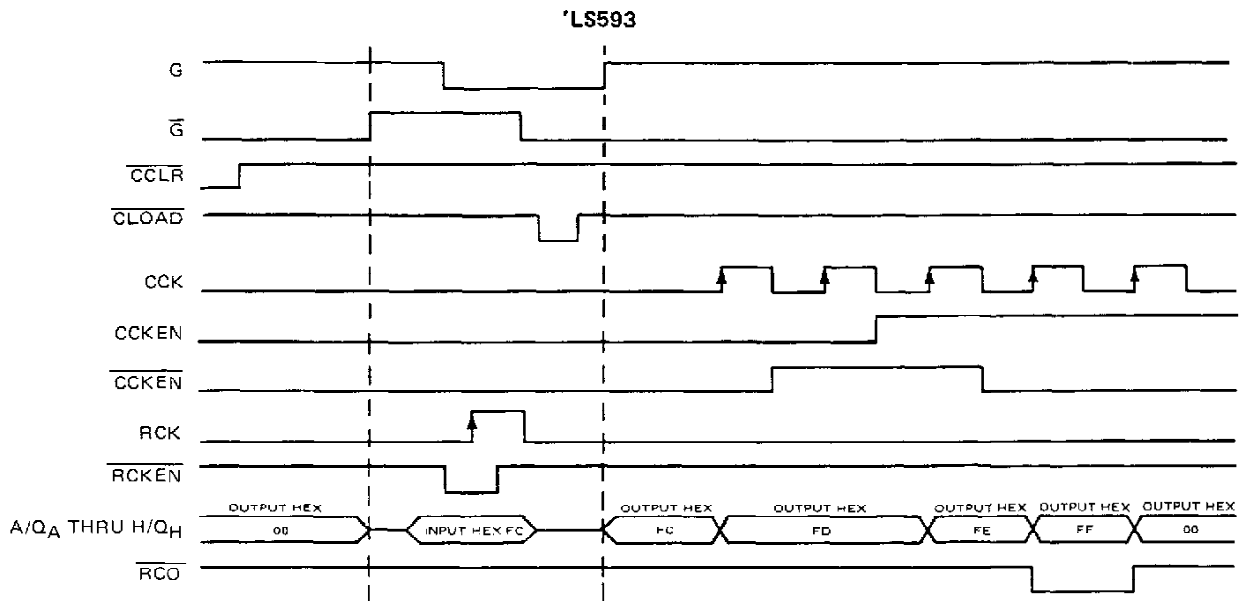
'LS593



Pin numbers shown are for DW, J, and N packages.

**SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS**

typical operating sequences



SN54LS592, SN54LS593, SN74LS592, SN74LS593

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593	-55°C to 125°C
SN74LS592, SN74LS593	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current	\overline{RCK}		-1	\overline{RCK}		-1	mA
		Q 'LS593 only		-1	Q 'LS593 only		-2.6	
I_{OL}	Low-level output current	\overline{RCK}		8	\overline{RCK}		16	mA
		Q 'LS593 only		12	Q 'LS593 only		24	
f_{CCK}	Counter clock frequency	0		20	0		20	MHz
$t_w(\overline{CCK})$	Duration of counter clock pulse	25			25			ns
$t_w(\overline{CCLR})$	Duration of counter clear pulse	20			20			ns
$t_w(\overline{RCK})$	Duration of register clock pulse	20			20			ns
$t_w(\overline{CLOAD})$	Duration of counter load pulse	40			40			ns
t_{su}	Register enable setup time	\overline{RCKEN} low to $\overline{RCK} \uparrow$, 'LS593		20	\overline{RCKEN} low to $\overline{RCK} \uparrow$, 'LS593		20	ns
t_{su}	Counter enable setup time before $\overline{CCK} \uparrow$	\overline{CCKEN} low, 'LS592		30	\overline{CCKEN} low, 'LS592		30	ns
		\overline{CCKEN} low or \overline{CCKEN} high, 'LS593		30	\overline{CCKEN} low or \overline{CCKEN} high, 'LS593		30	
		\overline{CCLR} inactive before $\overline{CCK} \uparrow$		20	\overline{CCLR} inactive before $\overline{CCK} \uparrow$		20	
t_{su}	Setup time	\overline{CLOAD} inactive before $\overline{CCK} \uparrow$		20	\overline{CLOAD} inactive before $\overline{CCK} \uparrow$		20	ns
		$\overline{RCK} \uparrow$ before $\overline{CLOAD} \uparrow$ (see Note 2)		30	$\overline{RCK} \uparrow$ before $\overline{CLOAD} \uparrow$ (see Note 2)		30	
		Data A thru H before $\overline{RCK} \uparrow$		20	Data A thru H before $\overline{RCK} \uparrow$		20	
		Data A thru H after $\overline{RCK} \uparrow$		0	Data A thru H after $\overline{RCK} \uparrow$		0	
t_h	Hold time	Data A thru H after $\overline{RCK} \uparrow$		0	Data A thru H after $\overline{RCK} \uparrow$		0	ns
		All others		0	All others		0	
T_A	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: This time insures the data saved by $\overline{RCK} \uparrow$ will also be loaded into the counter.



SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT				
		MIN	TYP‡	MAX	MIN		TYP‡	MAX		
V_{IK}	$V_{CC} = \text{MIN.}, I_I = -18 \text{ mA}$			-1.5		-1.5	V			
V_{OH}	'LS593 Q	$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V.}$ $V_{IL} = \text{MAX.}$	$I_{OH} = -1 \text{ mA}$	2.4	3.2		V			
	$\overline{\text{RCO}}$		$I_{OH} = -2.6 \text{ mA}$			2.4		3.1		
V_{OL}	'LS593 Q	$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V.}$ $V_{IL} = \text{MAX.}$	$I_{OL} = -1 \text{ mA}$	2.4	3.2	2.4	3.2	V		
			$I_{OL} = 12 \text{ mA}$			0.25	0.4			
			$I_{OL} = 24 \text{ mA}$						0.35	0.5
			$I_{OL} = 8 \text{ mA}$			0.25	0.4		0.25	0.4
			$I_{OL} = 16 \text{ mA}$				0.35	0.5		
I_{OZH}	'LS593 Q	$V_{CC} = \text{MAX.}, V_{IH} = 2 \text{ V.}$ $V_O = 2.7 \text{ V}$				20	20	μA		
I_{OZL}	'LS593 Q	$V_{CC} = \text{MAX.}, V_{IH} = 2 \text{ V.}$ $V_O = 0.4 \text{ V}$				-0.4	-0.4	mA		
I_I	'LS593 Q	$V_{CC} = \text{MAX.}$	$V_I = 5.5 \text{ V}$			0.1	0.1	mA		
	Others		$V_I = 7 \text{ V}$			0.1	0.1			
I_{IH}		$V_{CC} = \text{MAX.}, V_I = 2.7 \text{ V}$				20	20	μA		
I_{IL}	CCK	$V_{CC} = \text{MAX.}, V_I = 0.4 \text{ V}$				-0.8	-0.8	mA		
	RCK		'LS592				-0.2		-0.2	
			'LS593				-0.8		-0.8	
	A thru H						-0.4		-0.4	
	Others						-0.2		-0.2	
I_{OS}^{\S}	'LS593 Q	$V_{CC} = \text{MAX.}, V_O = 0 \text{ V}$		-30	-130	-30	-130	mA		
	$\overline{\text{RCO}}$			-20	-100	-20	-100			
I_{CC}	'LS592	$V_{CC} = \text{MAX.}$ All possible inputs grounded, All outputs open	I_{CCH}	40	60	40	60	mA		
			I_{CCL}	40	60	40	60			
	'LS593		I_{CCH}	47	70	47	70			
			I_{CCL}	53	80	53	80			
	I_{CCZ}		57	85	57	85				

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V.}, T_A = 25^\circ\text{C.}$

§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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8-BIT BINARY COUNTERS WITH INPUT REGISTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS592			'LS593			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CCK ↑	\overline{RCO}	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	20	35		20	35		MHz
t_{PLH}	CCK ↑	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$				14	21		ns
t_{PHL}	CCK ↑	Q					26	39		ns
t_{PLH}	\overline{CLOAD} ↓	Q					34	51		ns
t_{PHL}	\overline{CLOAD} ↓	Q					28	42		ns
t_{PHL}	\overline{CCLR} ↓	Q					25	38		ns
t_{PZH}	G ↑	Q					31	47		ns
t_{PZL}	G ↑	Q					27	40		ns
t_{PZH}	\overline{G} ↓	Q					29	45		ns
t_{PZL}	\overline{G} ↓	Q					31	47		ns
t_{PHZ}	G ↓	Q					33	50		ns
t_{PLZ}	G ↓	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$				35	52		ns
t_{PHZ}	\overline{G} ↑	Q					26	39		ns
t_{PLZ}	\overline{G} ↑	Q					28	42		ns
t_{PLH}	CCK ↑	\overline{RCO}								
t_{PHL}	CCK ↑	\overline{RCO}	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	15	23		14	21		ns
t_{PLH}	\overline{CLOAD} ↓	\overline{RCO}		20	30		20	30		ns
t_{PHL}	\overline{CLOAD} ↓	\overline{RCO}		31	47		31	47		ns
t_{PLH}	\overline{CCLR} ↓	\overline{RCO}		27	41		27	41		ns
t_{PHL}	\overline{CCLR} ↓	\overline{RCO}		30	45		30	45		ns
t_{PLH}	RCK ↑	\overline{RCO}	$R_L = 1\text{ k}\Omega$; $C_L = 30\text{ pF}$ $\overline{CLOAD} = L$	35	53		42	63		ns
t_{PHL}	RCK ↑	\overline{RCO}		30	45		33	50		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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