POWER designer

Expert tips, tricks, and techniques for powerful designs

No. 108

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Operation and Benefits of Active-Clamp Forward Power Converters

— Bob Bell, Power Applications Engineer

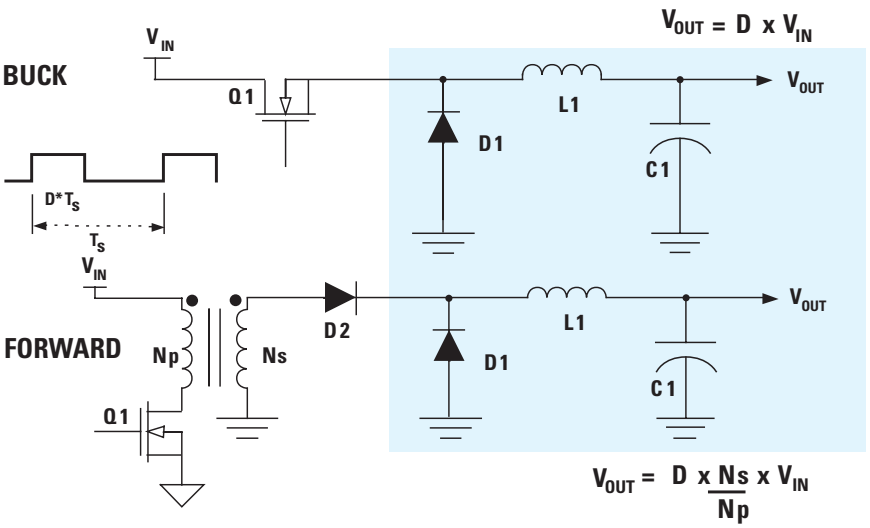


Figure 1. Buck and Forward Topologies

Forward converters with active-clamp reset offer multiple benefits to designers and are presently finding wide use. Power converters based on the forward topology are an excellent choice for applications where high efficiency and good power handling capability is required in the 50 to 500W power range. While the popularity of forward topology is based upon many factors, designers have been primarily drawn to it's simplicity, performance, and efficiency.

The forward converter is derived from the buck topology. The main difference between the two topologies is that the transformer employed in the forward topology provides input-output ground isolation as well as a step-down or step-up function. The transformer in a forward topology does not inherently reset each switching cycle as do symmetrical topologies (push-pull, half-bridge, and full-bridge). A number of different reset mechanisms have been employed in forward power converters, each method has its own benefits and challenges. Forward converters with active-clamp reset offer multiple benefits to designers and are presently finding wide use.

NEXT ISSUE:

Low-Power FPGA Designs

National Semiconductor

The Sight & Sound of Information

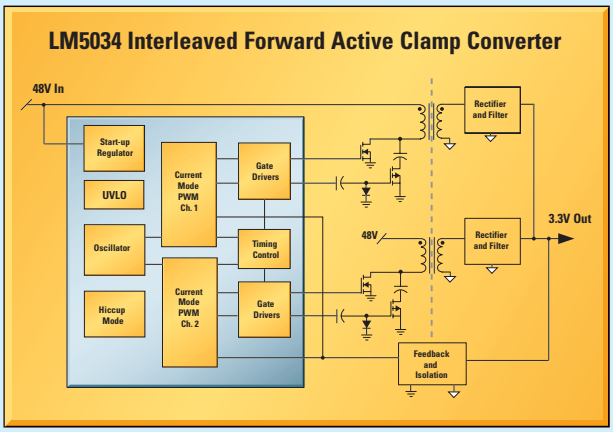
100V Dual Interleaved Active-Clamp Current-Mode Controller

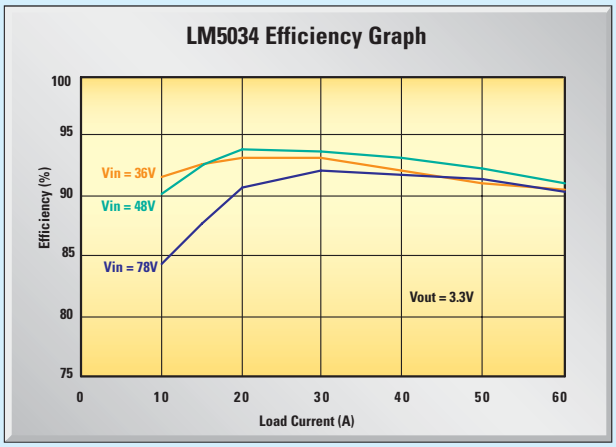
Highly Integrated LM5034 Maximizes Efficiency and Power Density of DC-DC Converters

Features

- Independent current-mode controllers
- Interleaved single or dual output operation
- Compound 2.5A main FET gate drivers
- Active clamp FET gate drivers
- Integrated 100V start-up regulator
- Up to 1 MHz switching frequency programmed by a single resistor
- Programmable maximum duty cycle
- Adjustable soft-start and input under-voltage sensing
- Adjustable deadtime between main and active clamp gate drivers
- Available in TSSOP-20 packaging

Ideal for telecom infrastructure, networking, industrial, and automotive power supplies





Product Highlight:

LM5034 enables high efficiency in 200W to 500W DC-DC converters while reducing input ripple

Operation and Benefits of Active-Clamp Forward Power Converters

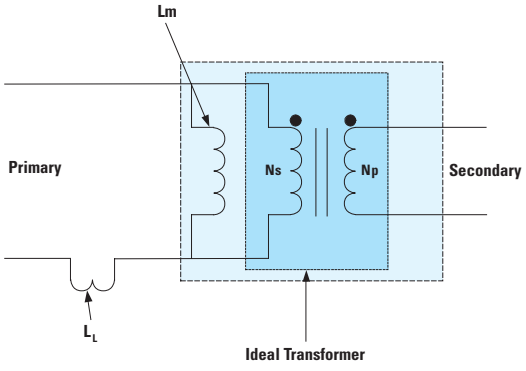


Figure 2. Transformer Model

Figure 1 shows the similarities between a buck and forward converter. Note the only difference between the transfer functions is the inclusion of the turns ratio term (Ns/Np) in the forward transfer function. Ns and Np are the number of secondary and primary turns, wound on the transformer core. *Figure 2* presents a transformer model, including the "Magnetizing Inductance" (Lm) shown in parallel with the primary winding. This magnetizing inductance can be measured at the primary terminals with the secondary winding(s) open circuit. The current in the magnetizing inductance is proportional to the flux density within the core. A given size core can only support a certain flux density before saturation of the core occurs. When the core saturates, there is a rapid reduction in inductance. Another element of the transformer model is the "Leakage Inductance" (L_L) in series with the primary winding. This leakage inductance can be measured at the primary terminals with the secondary winding(s) shorted. This term represents the stray primary inductance, which is not coupled to the secondary.

Active-Clamp Circuit Operation

Figures 3a through *3c* illustrate the main operational steps of an active clamp forward power converter. At time t0, the main power switch (Q1) is on, applying V_{IN} across the transformer primary. The transformer secondary winding voltage is V_{IN} x Ns/Np. The primary current is comprised of two components at this time; the reflected current from the output inductor (I_L x Ns/Np) and the current ramping up in the magnetizing inductance (Lm). The reset switch Q2 is open and the clamp capacitor (Cc) has been previously charged to a voltage of V_{IN}/(1-D), which will be explained later. This interval is the power phase, energy is transferred from the primary to the secondary during this period. The approximate duration of the power phase is Ts x V_{OUT} / V_{IN}, where Ts is the switching period.

At time t1, the main power switch (Q1) is turned off and the reset switch (Q2) is turned on. The magnetizing current flows through the clamp capacitor and Q2 instead of through Q1. Since the clamp capacitor voltage is greater than V_{IN}, the voltage across the transformer primary is now reversed, compared to the power phase t0. Because the potential across the magnetizing inductance has been reversed, the magnitude of the magnetizing current will decrease as the energy stored in the

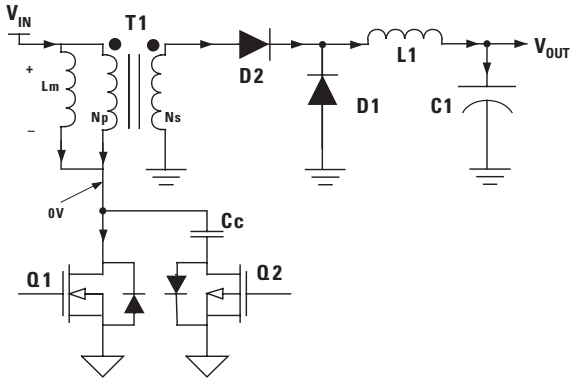


Figure 3a. Operation at Step t0

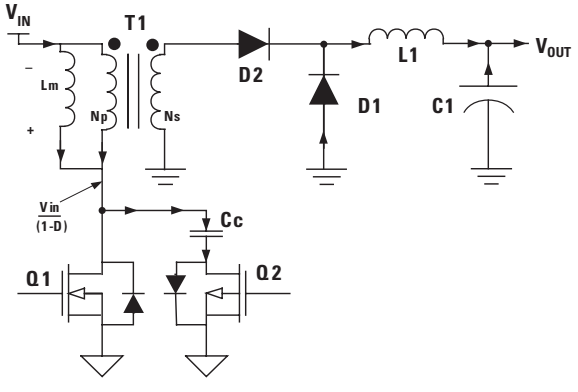


Figure 3b. Operation at Step t1

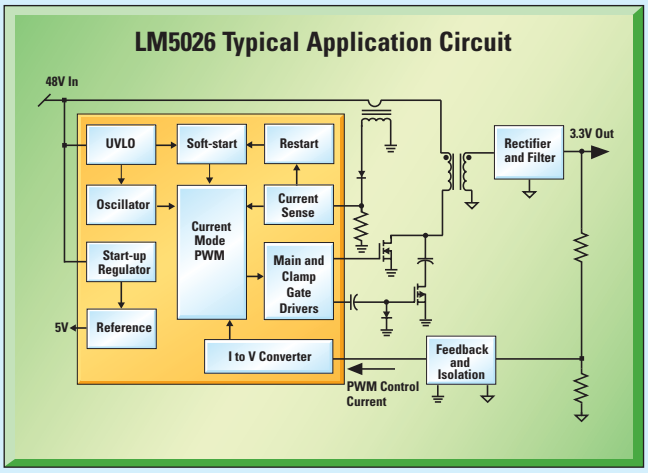
Current-Mode Controller for Forward Converters with Active-Clamp Reset

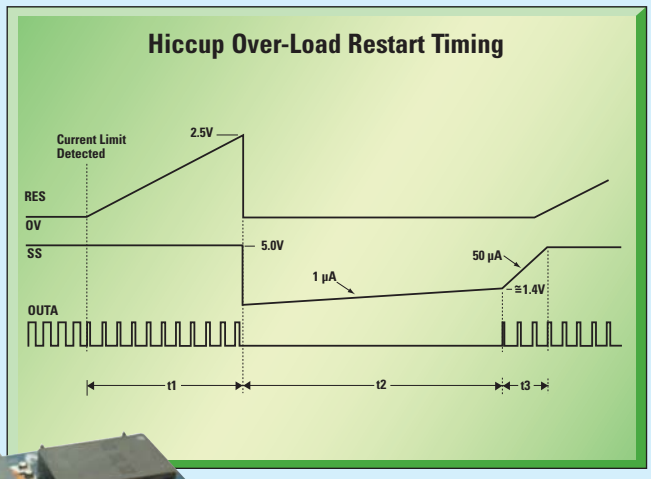
LM5026 Offers Versatile Dual-Mode Over-Current Protection with Hiccup Delay Timer

Features

- Wide range (8V to 100V) start-up bias regulator
- Two high-speed power MOSFET drivers: 3A main output driver and 1A clamp driver
- User-programmable maximum duty-cycle and UVLO hysteresis thresholds
- User-programmable gate driver overlap and dead-time
- Versatile dual-mode over-current protection with hiccup mode delay timer
- TSSOP-16 or thermally enhanced LLP-16 packaging

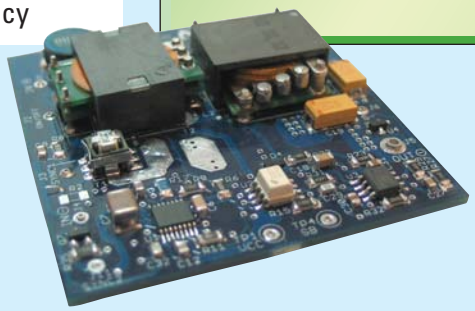
Ideal for use in telecommunications power systems, +42V automotive power systems, -48V distributed power systems, industrial power supplies, and multi-output power supplies





Product Highlight:

Robust and flexible forward active-clamp controller offers highest efficiency



Operation and Benefits of Active-Clamp Forward Power Converters

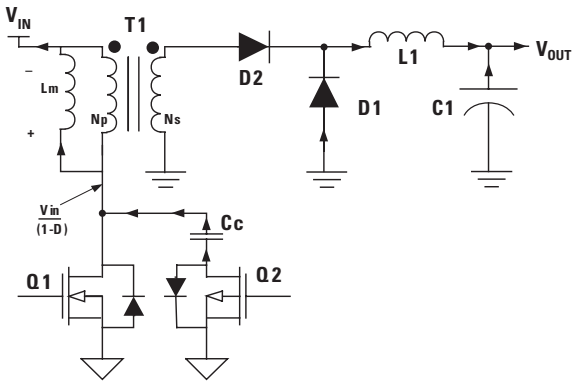


Figure 3c. Operation at Step t2

magnetizing inductance is transferred into the clamp capacitor. The voltage across the clamp capacitor increases slightly during this period and peaks when the magnetizing current reaches zero.

At t2, the current in the magnetizing inductance reaches zero and starts to build in the opposite direction, sourced from the clamp capacitor through the reset switch (Q2) and the magnetizing inductance (Lm) then back to the source (V_{IN}). The current will continue to build in the opposite direction as the clamp capacitor returns the energy that it had previously captured from the magnetizing inductance. Steady state conditions require the clamp capacitor voltage to return to the starting potential and the magnetizing current at the conclusion of the reset time to reach the same magnitude (opposite polarity) as the current at the beginning of this reset time. At the conclusion of t2, the switching period is over, as defined by the controller oscillator period. The reset switch is turned off, stopping the flow of current from the clamp capacitor.

Figure 4 shows several of the key circuit waveforms. The uppermost waveforms are the modulator ramp and error signals which determine the main switch on-time. The center waveform is the main switch drain voltage, which is low when the switch is on and rises to the clamp capacitor potential when the

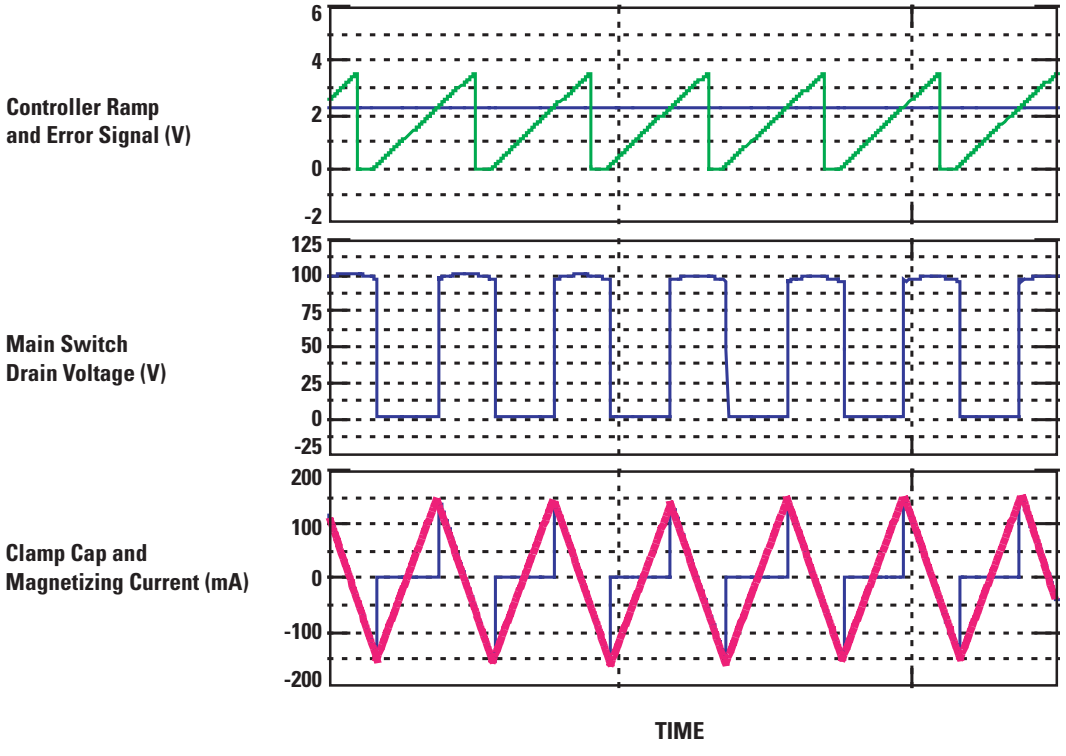
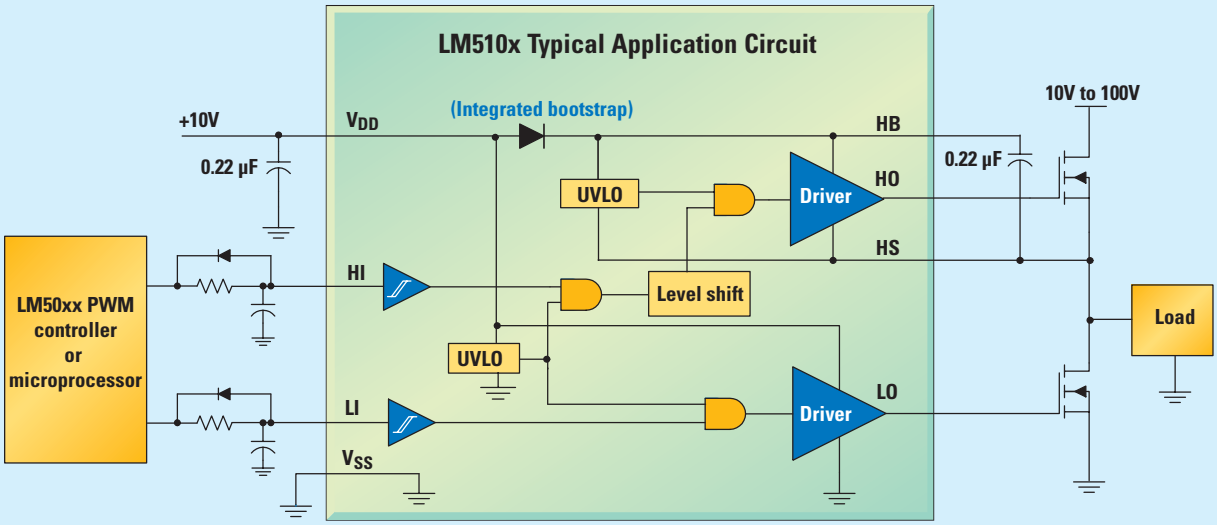


Figure 4. Key Active-Clamp Waveforms

100V Half-Bridge Power MOSFET Drivers

LM510x Family Offers the Industry's Highest Peak Gate Drive Current



Features

- Flexible configurations: interleaved forward, cascaded push-pull, half-bridge or full-bridge
- User-programmable turn-on edge delay feature (LM5105)
- New high-voltage bootstrap diode
- Best-in-class speed and efficiency in high-frequency switching regulator applications
- Negative load voltage transient capability down to –5V (LM5105/07)
- Available in SOIC and tiny, thermally enhanced LLP® packaging

Ideal for half-bridge and full-bridge power DC-DC converters, cascading current-fed or voltage-fed DC-DC converters, high-voltage buck DC-DC converters, and solid-state motor and solenoid drivers

Family Highlight:

Synchronous gate drivers optimized for every topology and high efficiency

Peak Gate Current	Product ID	Input Threshold	Packaging	Comments
NEW! 3.0A	**LM5100A/01A**	CMOS / TTL	LLP-10, SOIC-8	Upgrade on HIP2100/01
NEW! 1.8A	**LM5105**	TTL	LLP-10	Programmable dead-time, negative V_{LOAD}
NEW! 1.4A	**LM5107**	TTL	LLP-8, SOIC-8	Upgrade of ISL6700, negative V_{LOAD}

Operation and Benefits of Active-Clamp Forward Power Converters

switch is off. The red line in the lower waveform represents the magnetizing inductance current, which flows through the clamp capacitor (blue line waveform) during the reset time. As expected, both currents are balanced around the zero.

Benefits of Active-Clamp Reset

Several switching loss benefits can be realized with active-clamp reset. With sufficiently fast gate drive, the turn off of Q1 can be virtually lossless. To accomplish this, the gate of Q1 must be turned off (and the flow of current stopped) before the drain voltage has a chance to rise. The rise of the drain voltage is delayed due to the drain-source capacitance; a robust gate driver can turn off Q1 before the drain voltage increases significantly. The use of a compound gate driver made up of MOS and Bipolar devices provides a high peak gate discharge current to ensure a fast turn off and reduced switching losses. Turn-on losses can be reduced with proper selection of the switch delays, allowing time for the drain voltage reduction prior to the initiation of the main switch.

For steady state operation, the net Voltage x Time product applied to the magnetizing inductance over a complete cycle must equal zero. When the main switch is on, the Volt x Time product is V_{IN} x D x Ts, where D is the on-time duty cycle and Ts is the switching period. The off period is defined as (1-D) x Ts. The voltage across the primary when the main switch is off is $V_C - V_{IN}$, where V_C is the clamp capacitor voltage. In steady state operation, the Volt x Time products must be equal:

$$V_{IN} \times D \times Ts = (V_C - V_{IN}) \times (1-D) \times Ts$$

Solving for clamp capacitor voltage yields:

$$V_C = V_{IN} / (1-D)$$

Remember that the duty cycle (D) decreases as V_{IN} increases. The clamp capacitor voltage will adapt to changing line (V_{IN}) conditions to maintain this equality. This important feature minimizes the voltage stress across the main switch for all operating conditions, thus allowing use of lower $V_{(BR)DSS}$ rated devices. A lower MOSFET $V_{(BR)DSS}$ rating leads to lower on resistance and lower gate charge, which translates into higher conversion efficiency.

The energy stored in the leakage inductance is re-circulated rather than dissipated and the possibility of duty cycles over 50% leads to lower voltage stress on the rectifiers, further reducing losses.

Evaluation Boards

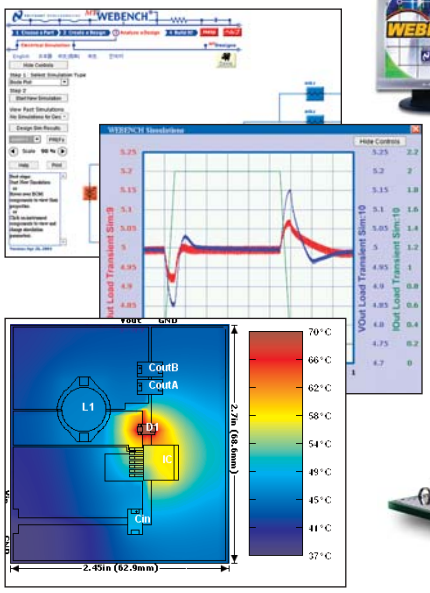
Several DC-DC converter demonstration boards employing active clamp reset are available, implemented with either voltage-mode or current-mode control. The input voltage range is 36V to 75V, with the output rated for 100W at 3.3V. The peak efficiency of 93% was measured at 15A load. The power transformer has a 6-to-1 turns ratio. The primary winding is made of 12 turns and the secondary winding is made of 2 turns. A planar construction technique is employed and the primary is fabricated with a multi-layer PC board. The high-current secondary is fabricated with insulated copper stampings.

The LM5025, LM5026, and LM5034 controllers directly drive the N-Channel power switch and a P-Channel reset switch. The internal gate drivers are sized differently for each switch. The reset switch only carries the magnetizing current allowing smaller gate drive. The main switch requires a robust gate drive in order to achieve the reduction in switching losses. The necessary timing delay between each of the gate driver outputs is programmable within the controller. The output rectifiers are implemented with synchronous MOSFETs. The active reset scheme eases the implementation of synchronous rectifiers as they can be self-driven.

Conclusion

In summary, the active-clamp technique allows the use of lower voltage rated MOSFETs and eases the use of self-driven synchronous rectifiers. The magnetizing and leakage energies are recycled and returned to the source. These benefits allow power converter designers to extend the power conversion efficiency. ■

Power Design Tools



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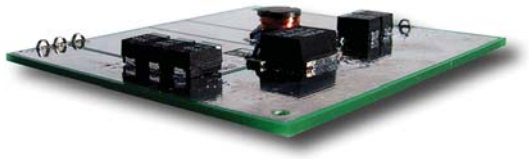

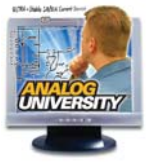

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