MODIFIED COMPACT MODEL OF MOSFET WORKING UNDER ESD STRESS

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A modified compact model to simulate the high current characteristics of a MOSFET working under ESD stress is developed. The model realized with current source is used to demonstrate the better accuracy of simulated I-V characteristics for the snapback region. The variation of the simulated output I-V characteristics from gate voltage values is presented graphically.

Keywords: ESD, MOSFET model, Spice simulation

1. INTRODUCTION

The high current and voltage levels at the ICs under ESD stress is the one of major problems for failures in the semiconductor industry. Now days with tendency of IC's sizes diminishing and result of ESD occurring the device work in different mode, named snapback. Therefore, the simulation and test of the ESD protection circuits is important and necessary. Developing of compact model includes uses of CAD simulation tools, sufficient computing power and special protection device and the process of work requires correction of all level of simulation.

In this paper is presented a modified compact MOSFET model working under ESD stress which is developed with Spice. The compact model is realized with current source and allows receiving a precision result of simulated I-V characteristics at all gate voltage values. The circuit parameters are extracted from experimental data using a systematic methodology, presented in paper [1]. Analytical equations about avalanche multiplication factor M are developed and the results are presented graphical for different values of gate voltage.

2. PROBLEM STATEMENT

2.1 Problems in snapback mode for MOS transistors

In result of ESD stress the current flows into the substrate region and the device works in a mode different from the normal gate-controlled mode. The device moves into a regime where the

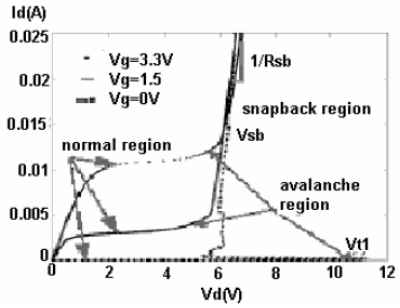

Fig. 1 Experimental I-V characteristics for MOSFET

source/drain junction and substrate current are controlled by distributed bulk voltage drops and complex breakdown mechanism. The measured I-V curves [1] in Fig.1 present three regions of operation: normal, avalanche breakdown and snapback. The normal mode includes the linear region and the saturation region, defined by standard MOS equations and modeled in SPICE. When the voltage drops under lateral bipolar transistor is large enough to turn it on the device enters in the avalanche region. As a result the drain current Id rapidly increases exponentially (in Fig.1) due to channel carrier multiplication. As long as standard MOS equations are not longer valid in the avalanche breakdown region and the snapback region, it is necessary to develop the analytical models for description of ESD region to formulate the analytical avalanche breakdown expressions.

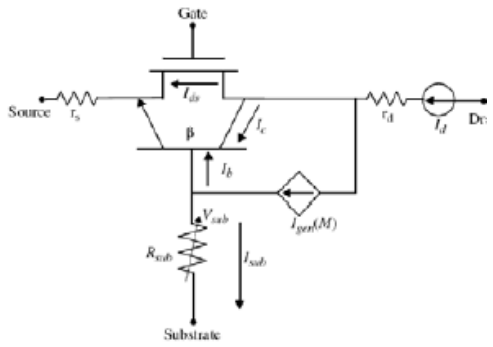

Fig. 2 Compact model of MOSFET transistor

2.2 Parameter extraction depending on gate voltage values V(G)

In [1] was presented circuit model including voltage source but in this case it was impossible to simulate I-V curve at Vg=0. Therefore it is necessary to optimize the model by replacing the voltage source with current source to improve the accuracy of simulated results. The modified compact model is presented in fig.3.

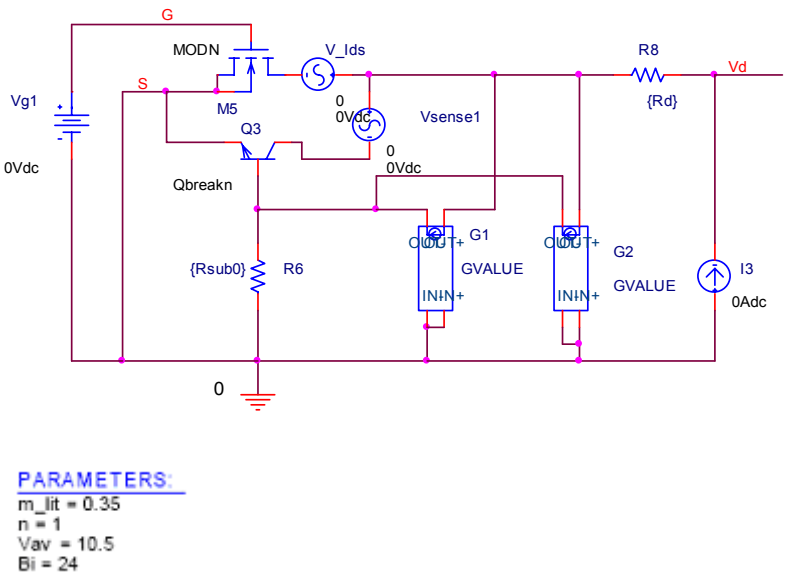

Fig. 3 Spice circuit model of MOSFET and Spice constant parameters

The avalanche multiplication factor M, is introduced according equation 1 in [1] for all cases except when Vg=0, where the correction of M approximation is performed by the following expression:

$$M = \exp(h_1(V_d - V_{d1})) + \exp(h_2(V_d - V_{d2})), (1)$$

where h1=2, Vd1=4, h2=40 and Vd2=10 and these parameters are extracted form fig.4.

Blocks G1 and G2 in Fig.3 are current-controlled-current sources. G1 is used for simulation of the I-V curves for Vg=0.9, 1, 1.5, 2.1, 2.7, 3.3V and is given by the expression:

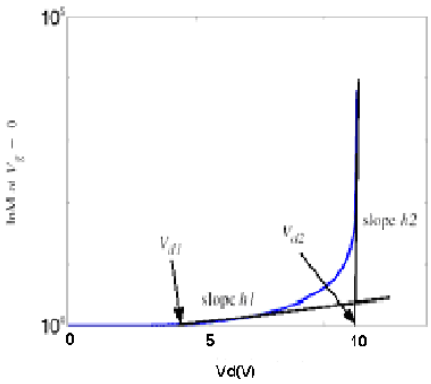

Fig. 4 Characteristic of M=f(Vd) at Vg=0

EXP={if((V(G)<0.1),((exp(2*(V(Vd)-4))+exp(40*(V(Vd)-10)))*(I(Vsense1)+I(V_Ids))), 0)}, (2)

where V(G) is gate voltage and Vd is drain voltage.

Added block G2 is required to simulate Id=f(Vd) characteristics at Vg=0:

EXP={{ if((V(G)>0.1), 1, 0)}*(1/(1-4.5*pwr((V(Vd)-V(MM)),0.35)*exp(-24/pwr((V(Vd)-V(MM)),1)))-1)*(I(Vsense1)+I(V_Ids))}, (3)

where V(MM) is channel drain voltage and is calculated with block ABM (fig.5):

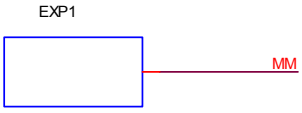

Fig. 5 Additional ABM calculated block

EXP1=0.1*(V(G)-0.465)+0.1*(V(G)-0.465)*(V(G)-0.465), (4)

3. RESULTS

The simulations of compact model with voltage source are presented in fig.6. The relative error of simulated I-V curves does not exceed 5%. The received I-V cures in fig.6 corresponding to all gate voltage values except at Vg=0. This is because SPICE DC Sweep analysis can not approximate decreasing of drain voltage after it has risen up to 10,5V. Avalanche multiplication factor M as function of drain voltage is presented in fig.7.

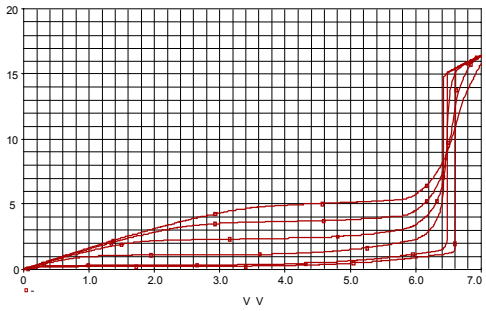

Fig. 6 Simulated Id=f(Vd) characteristics for circuit with voltage source at Vg=0.9,1,1.5,2.1,2.7,3.3

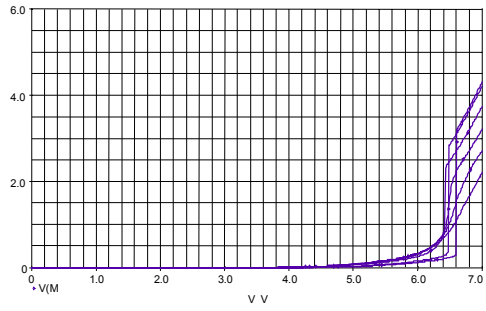

Fig. 7 Simulated M characteristics for circuit with voltage source at Vg=0.9,1,1.5,2.1, 2.7, 3.3

Better results are achieved when the voltage source is replaced by a current source and they are presented in Fig.8. This characteristics correspond to all taken gate voltages (including Vg=0). The relative error of I-V characteristics does not exceed

4% for all gate voltage values. Fig. 9 shows simulated characteristics of M defined with eq. 1 in [1] and equation 1.

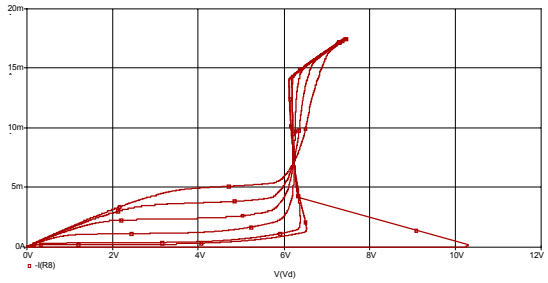

Fig. 8 Simulated Id=f(Vd) characteristics for compact model with current source at Vg=0,0.9,1,1.5,2.1,2.7,3.3

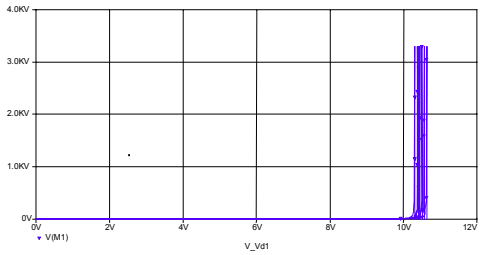

Fig. 9 Simulated M characteristics for compact model with current source at Vg=0.9,1,1.5,2.1, 2.7, 3.3

4. CONCLUSIONS

The compact model presented in this work includes original BSIM3 MOS transistor and parasitic bipolar transistor. The simulations are performed with PSpice OrCAD. The model is optimized to work for all values of Vg including at Vg=0 and it has better accuracy of results in snapback region.

ACKNOWLEDGEMENTS

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