

Features

- Complete variable-gain amplifier complete with output amplifier
- Compensated for Gain ≥ 10
- 50 MHz signal bandwidth
- 50 MHz gain-control bandwidth
- Low 29 nV/ $\sqrt{\text{Hz}}$ input noise
- Operates on $\pm 5\text{V}$ to $\pm 15\text{V}$ supplies
- All inputs are differential
- > 70 dB attenuation @ 5 MHz

Applications

- AGC variable-gain amplifier
- IF amplifier
- Transducer amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4452CN	-40°C to +85°C	14-pin P-DIP	MDP0031
EL4452CS	-40°C to +85°C	14-lead SO	MDP0027

General Description

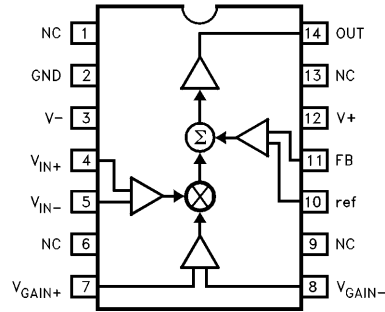
The EL4452 is a complete variable-gain circuit. It offers wide bandwidth and excellent linearity, while including a powerful output voltage amplifier, drawing modest current. The higher gain and lower input noise makes the EL4452 ideal for use in AGC systems.

The EL4452 operates on $\pm 5\text{V}$ to $\pm 15\text{V}$ and has an analog input range of $\pm 0.5\text{V}$. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of -40°C to $+85^\circ\text{C}$ and is packaged in 14-pin P-DIP and SO-14.

The EL4452 is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

Connection Diagram



4452-1

Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation.

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

V_+	Positive Supply Voltage	16.5V	I_{IN}	Current into any Input or Feedback Pin	
V_S	V_+ to V_- Supply Voltage	33V	I_{OUT}	Output Current	4 mA
V_{IN}	Voltage at any Input or Feedback	V_+ to V_-	P_D	Maximum Power Dissipation	30 mA
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_A	Operating Temperature Range	See Curves -40°C to +85°C
			T_S	Storage Temperature Range	-60°C to +150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level Test Procedure

I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^\circ\text{C}$ and QA sample tested at $T_A = 25^\circ\text{C}$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^\circ\text{C}$ for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at $\pm 5\text{V}$, $T_A = 25^\circ\text{C}$, $R_F = 910\Omega$, $R_G = 100\Omega$, $R_L = 500\Omega$

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{DIFF}	Signal Input Differential Input Voltage - Clipping 0.6% Nonlinearity	0.4	0.5 0.4		I V	V V
V_{CM}	Common-Mode Range (All Inputs; $V_{DIFF} = 0$) $V_S = \pm 5\text{V}$ $V_S = \pm 15\text{V}$	± 2.0 ± 12.0	± 2.8 ± 12.8		I V	V V
V_{OS}	Input Offset Voltage			10	I	mV
$V_{OS, FB}$	Output Offset Voltage			10	I	mV
$V_G, 100\%$	Extrapolated Voltage for 100% Gain	1.8	2.1	2.2	I	V
$V_G, 0\%$	Extrapolated Voltage for 0% Gain	-0.16	-0.06	0.04	I	V
$V_G, 1\text{V}$	Gain at $V_{GAIN} = 1$ ($R_f = 910\Omega$, $R_g = 100\Omega$)	4.9	5.35	5.9	I	V/V
I_B	Input Bias Current (All Inputs)	-20	-9	0	I	μA
I_{OS}	Input Offset Current Between V_{IN}^+ and V_{IN}^- , V_{GAIN}^+ and V_{GAIN}^-		0.5	4	I	μA
F_T	Signal Feedthrough, $V_G = -1\text{V}$		-100	-70	I	dB
$R_{IN, Signal}$	Input Resistance, Signal Input	25	60		I	k Ω
$R_{IN, Gain}$	Input Resistance, Gain Input	50	120		I	k Ω
$R_{IN, FB}$	Input Resistance, Feedback	25	60		V	k Ω
CMRR	Common-Mode Rejection Ratio, V_{IN}	70	90		I	dB

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Open-Loop DC Electrical Characteristics — Contd.

Power supplies at $\pm 5V$, $T_A = 25^\circ C$, $R_F = 910\Omega$, $R_G = 100\Omega$, $R_L = 500\Omega$

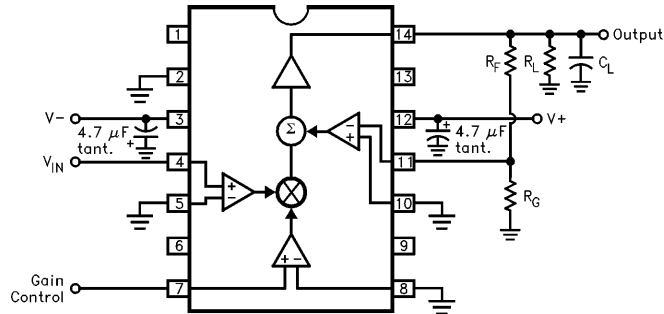
Parameter	Description	Min	Typ	Max	Test Level	Units
PSRR	Power-Supply Rejection Ratio, V_{OS} , FB; Supplies from $\pm 5V$ to $\pm 15V$	65	83		I	dB
E_G	Gain Error, Excluding Feedback Resistors, $V_{GAIN} = 2.5V$	-7		+7	I	%
NL	Nonlinearity, V_{IN} from $-0.25V$ to $+0.25V$, $V_{GAIN} = 1V$		0.3	0.6	I	%
V_O	Output Voltage Swing ($V_{IN} = 0$, V_{REF} Varied)	$V_S = \pm 5V$	± 2.5	± 2.8	I	V
		$V_S = \pm 15V$	± 12.5	± 12.8	I	V
I_{SC}	Output Short-Circuit Current	40	85		I	mA
I_S	Supply Current, $V_S = \pm 15V$		15.5	18	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at $\pm 12V$, $T_A = 25^\circ C$, $R_L = 500\Omega$, $C_L = 15pF$

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, -3dB	-3dB Small-Signal Bandwidth, Signal Input		50		V	MHz
BW, $\pm 0.1dB$	0.1dB Flatness Bandwidth, Signal Input		10		V	MHz
Peaking	Frequency Response Peaking		0.1		V	dB
BW, Gain	-3dB Small-Signal Bandwidth, Gain Input		50		V	MHz
SR	Slew Rate, V_{OUT} between $-2V$ and $+2V$	350	400	550	I	V/ μs
V_N	Input-Referred Noise Voltage Density		29		V	nV/rt-Hz

Test Circuit



4452-2

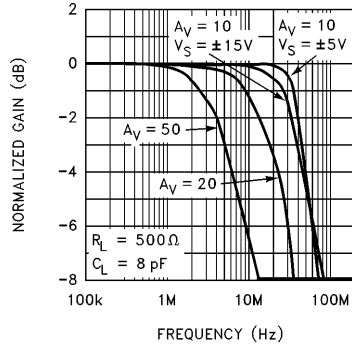
Note: For typical performance curves, $R_F = 910\Omega$, $R_G = 100\Omega$, $V_{GAIN} = 1V$, $R_L = 500\Omega$, and $C_L = 15 pF$ unless otherwise noted.

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

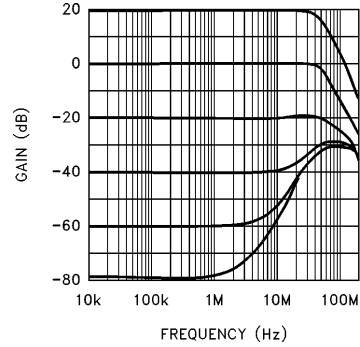
Typical Performance Curves

Frequency Response for Various Feedback Divider Ratios



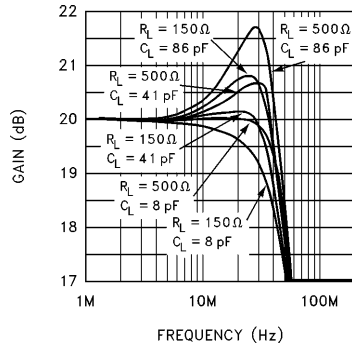
4452-3

Frequency Response for Various Gains



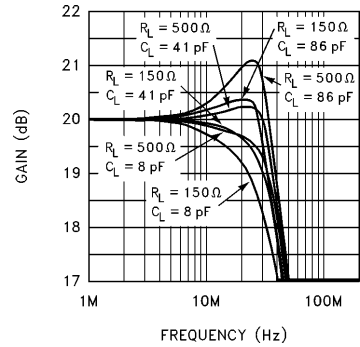
4452-4

Frequency Response for Various R_L , C_L , $V_S = \pm 5V$



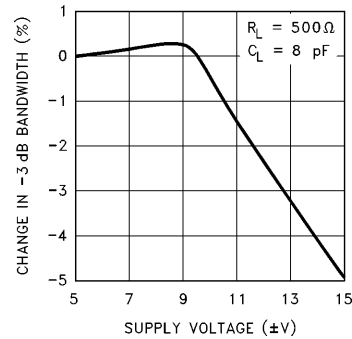
4452-5

Frequency Response for Various R_L , C_L , $V_S = \pm 15V$



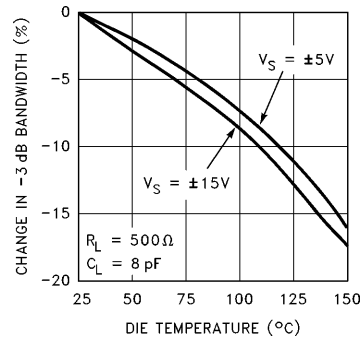
4452-6

-3 dB Bandwidth vs Supply Voltage



4452-7

-3 dB Bandwidth vs Die Temperature

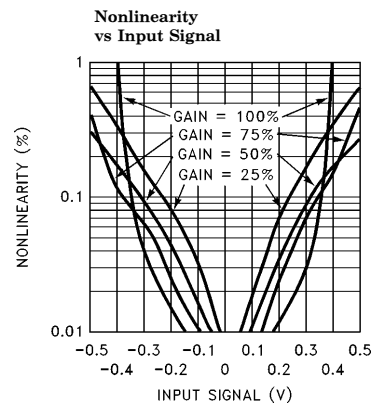
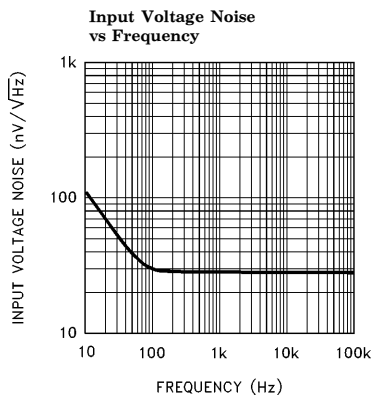
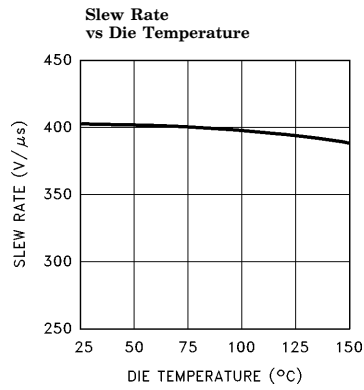
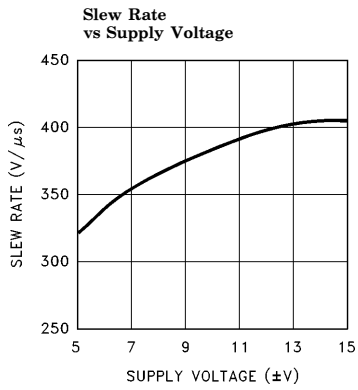
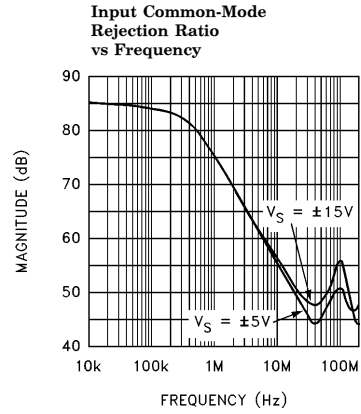
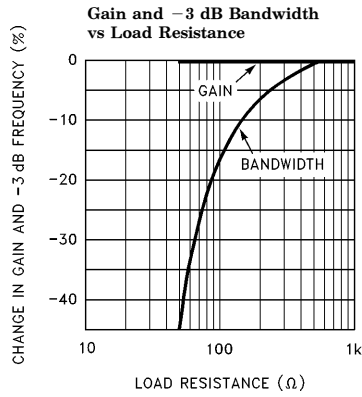


4452-8

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

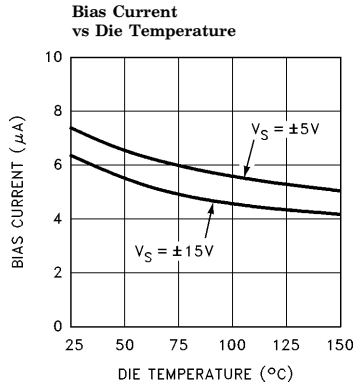
Typical Performance Curves — Contd.



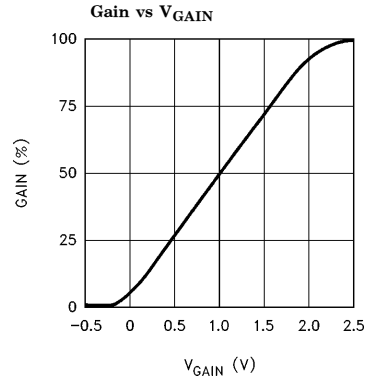
EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

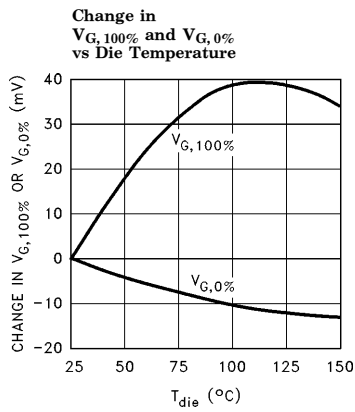
Typical Performance Curves — Contd.



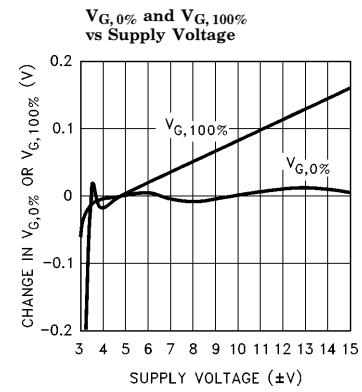
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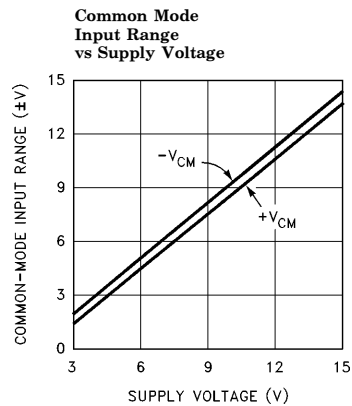
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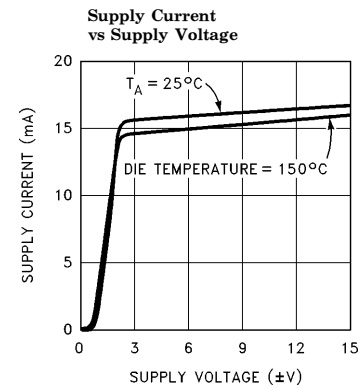
4452-17



4452-18



4452-19

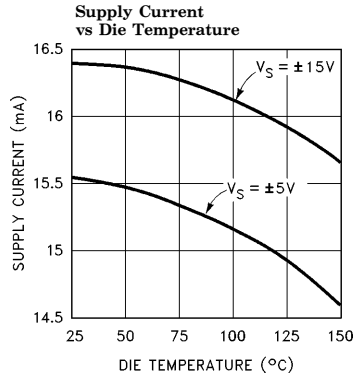


4452-20

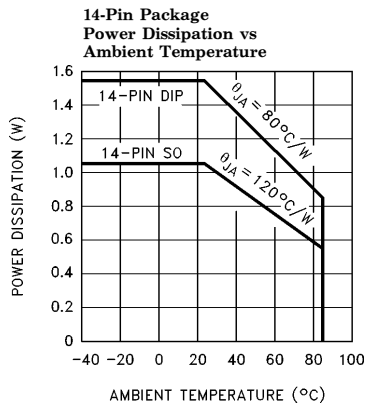
EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Typical Performance Curves — Contd.



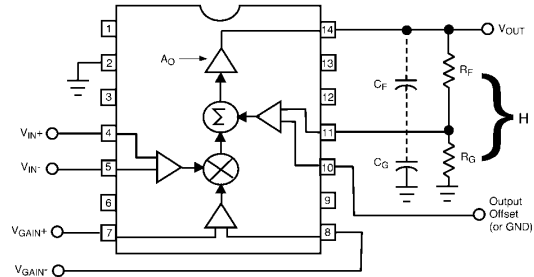
4452-21



4452-22

Applications Information

The EL4452 is a complete two-quadrant multiplier/gain control with 50 MHz bandwidth. It has three sets of inputs; a differential signal input V_{IN} , a differential gain-controlling input V_{GAIN} , and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:



4451-23

The gain of the feedback divider is H . The transfer function of the part is

$$V_{OUT} = A_O \times ((V_{IN+}) - (V_{IN-})) \times ((V_{GAIN+}) - (V_{GAIN-})) + (V_{REF} - V_{FB})$$

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is approximately 3300. The large value of A_O drives

$$((V_{IN+}) - (V_{IN-})) \times \frac{1}{2} ((V_{GAIN+}) - (V_{GAIN-})) + (V_{REF} - V_{FB}) \rightarrow 0$$

Rearranging and substituting for V_{FB}

$$V_{OUT} = (((V_{IN+}) - (V_{IN-})) \times \frac{1}{2} ((V_{GAIN+}) - (V_{GAIN-})) + V_{REF})/H, \text{ or}$$

$$V_{OUT} = (V_{IN} \times \frac{1}{2} V_{GAIN} + V_{REF})/H$$

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Applications Information — Contd.

Thus the output is equal to the difference of the V_{IN} 's times the difference of V_{GAIN} 'S and offset by V_{REF} , all gained up by the feedback divider ratio. The EL4452 is stable for a divider ratio of $\frac{1}{10}$, and the divider may be set for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 130 MHz; typical strays of 3 pF thus require a feedback impedance of 400Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback and the gain resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, a 3 pF capacitor across R_F and 27 pF to ground will dominate parasitic effects in a $\frac{1}{10}$ divider and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, for DC offsetting of the output, or it can be used to sum in another signal.

Gain-Control Characteristics

The quantity V_{GAIN} in the above equations is bounded as $0 \leq V_{GAIN} \leq 2$, even though the externally applied voltages exceed this range. Actually, the gain transfer function around 0 and 2V is "soft"; that is, the gain does not clip abruptly below the 0%- V_{GAIN} voltage nor above the 100%- V_{GAIN} level. An overdrive of 0.3V must be applied to V_{GAIN} to obtain truly 0% or 100%. Because the 0%- or 100%- V_{GAIN} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{GAIN} range of $-0.5V$ to $+2.5V$ will assure the full numerical span of $0 \leq V_{GAIN} \leq 2$.

The gain control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 nsec.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or 6" of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between $(V-) + 2.5V$ and $(V+) - 2.5V$ to ensure linearity. Additionally, the differential voltage on any input stage must be limited to $\pm 6V$ to prevent damage. The differential signal range is $\pm 0.5V$ in the EL4452. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between $(V-) + 2.5V$ and $(V+) - 3.5V$. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and feedthrough over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4452 operates with power supplies from $\pm 3V$ to $\pm 15V$. The supplies may be of different voltages as long as the requirements of the ground pin are observed (see the Ground Pin section). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and $V-$ to ground. The inputs

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Applications Information — Contd.

and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4452 increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S \times I_{S, \max} + (V_S - V_O) \times V_O / R_{PAR}$$

where $I_{S, \max}$ is the maximum supply current

V_S is the \pm supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4452 draws a maximum of 18mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with $\pm 5V$ supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and other parameters is

$$V_{S, \max} = (P_D + V_O^2 / R_{PAR}) / (2I_{S, \max} + V_O / R_{PAR})$$

The maximum dissipation a package can offer is

$$P_{D, \max} = (T_{J, \max} - T_{A, \max}) / \theta_{JA}$$

Where $T_{J, \max}$ is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

$T_{A, \max}$ is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded.

Output Loading

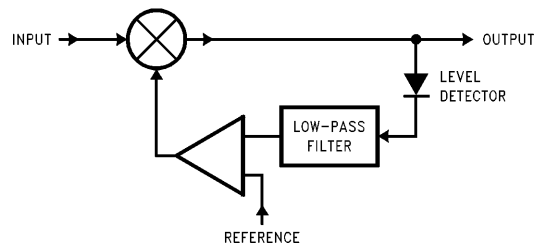
The output stage of the EL4452 is very powerful. It can typically source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to a 100Ω load. Heavy resistive loading will degrade frequency response and distortion for loads < 100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 1 dB with even a 220 pF load.

AGC Circuits

The basic AGC (automatic gain control) loop is this:



Basic AGC Loop

A multiplier scales the input signal and provides necessary gain and buffers the signal presented to the output load, a level detector (shown schematically here as a diode) converts some measure of the output signal amplitude to a DC level, a low-pass filter attenuates any signal ripple present on that DC level, and an amplifier compares that level to a reference and amplifies the error to create a gain-control voltage for the multiplier. The circuitry is a servo that attempts to keep the output amplitude constant by continuously adjusting the multiplier's gain control input.

EL4452C

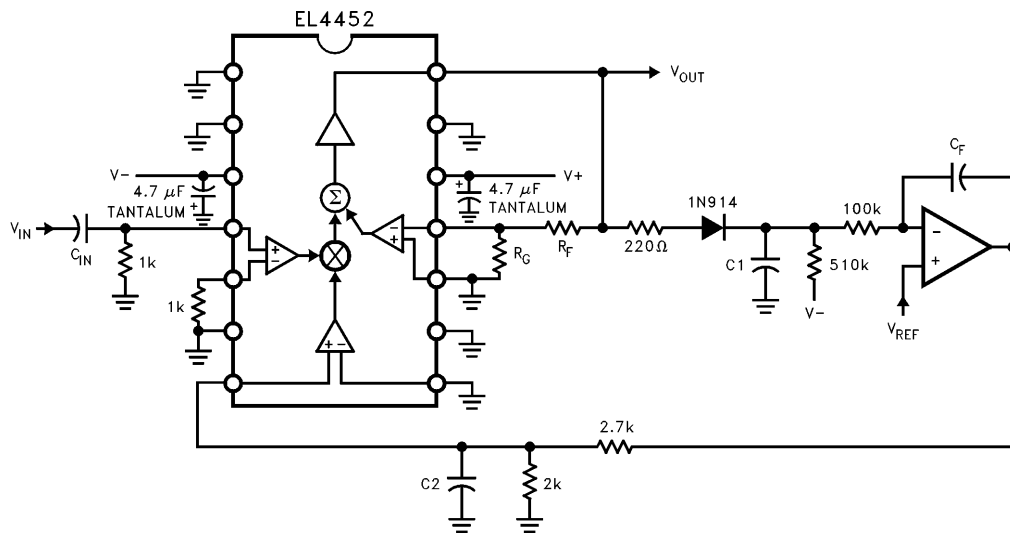
Wideband Variable-Gain Amplifier with Gain of 10

Applications Information — Contd.

Most AGC's deal with repetitive input signals that are capacitively coupled. It is generally desirable to keep DC offsets from mixing with AC signals and fooling the level detector into maintaining the DC output offset level constant, rather than a smaller AC component. To that end, either the level detector is AC-coupled, or the reference voltage must be made greater than the maximum multiplier gain times the input offset. For instance, if the level detector output equaled

the reference voltage at 1V of EL4452 output, the 8 mV of input offset would require a maximum gain of 125 through the EL4452. Bias current-induced offsets could increase this further.

Depending on the nature of the signal, different level detector strategies will be employed. If the system goal is to prevent overload of subsequent stages, peak detectors are preferred. Other strategies use an RMS detector to maintain constant output power. Here is a simple AGC using peak detection:



4452-25

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

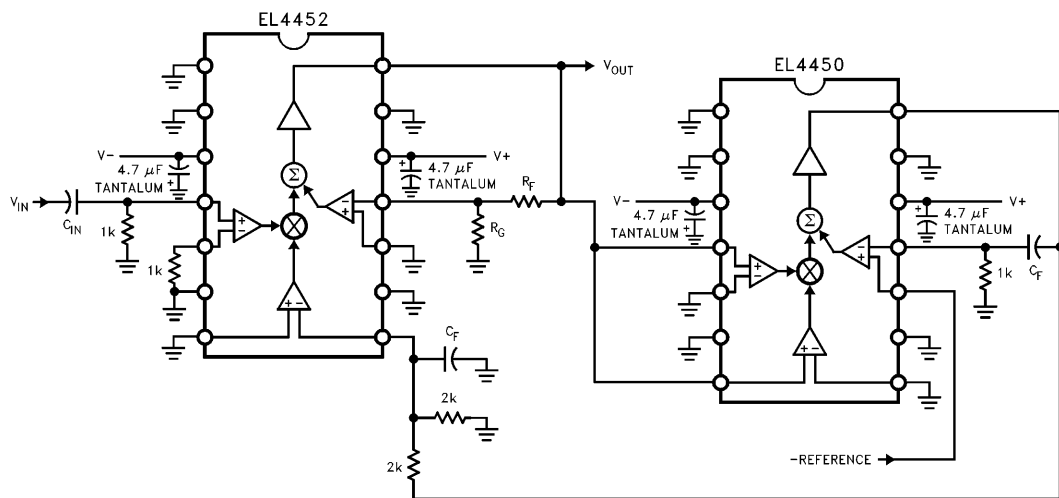
Applications Information — Contd.

The output of the EL4452 drives a diode detector which is compared to V_{REF} by an offset integrator. Its output feeds the gain-control input of the EL4452. The integrator's output is attenuated by the $2\text{ k}\Omega$ and $2.7\text{ k}\Omega$ resistors to prevent the op-amp from overloading the gain-control pin during zero input conditions. The $510\text{ k}\Omega$ resistor provides a pull-down current to the peak level storage capacitor C1 to allow it to drift negative when output amplitude reduces. Thus the detector is of fast attack and slow decay design, able to reduce AGC gain rapidly when signal amplitude suddenly increases, and increases gain slowly when the input drops out momentarily. The value of C1 determines drop-out reaction rates, and the value of C_F affects overall loop time constant as well as the amount of ripple on the gain-control line. C2 can be used to reduce this ripple fur-

ther, although it contributes to loop overshoot when input amplitude changes suddenly. The op-amp can be any inexpensive low-frequency type.

The major problem with diode detectors is their large and variable forward voltage. They require at least a 2 V_{P-P} peak output signal to function reliably, and the forward voltage should be compensated by including a negative V_D added to V_{REF} . Even this is only moderately successful. At the expense of bandwidth, op-amp circuits can greatly improve diode rectifiers (see "An Improved Peak Detector", an Elantec application note). Fortunately, the detector will see a constant amplitude of signal if the AGC is operating correctly.

A better-calibrated method is to use a four-quadrant multiplier as a square-law detector. Here is a circuit employing the EL4450:



4452-26

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Applications Information — Contd.

In this circuit, the EL4450 not only calculates the square of the input, but also provides the offset integrator function. The product of the two multiplier inputs adds to the $-$ Reference input and are passed to the output amplifier, which through C_F behaves as a pseudo-integrator. The "integrator" gain does not pass through zero at high frequencies but has a zero at $1/(2\pi C_F \times 1 \text{ k}\Omega)$. This zero is cancelled by the pole caused by the second capacitor of value C_F connected at the EL4452 $-V_{\text{GAIN}}$ input. The $-$ Reference can be exchanged for a positive reference by connecting it to the ground return of the 1 k Ω resistor at the FB terminal and grounding REF.

As a general consideration, the input signal applied to an EL4452 should be kept below about 250 mV peak for good linearity. If the AGC were designed to produce a 1V peak output, the input range would be 100 mV–250 mV peak when the EL4452 has a feedback network that establishes a maximum gain of 10. This is an input range of only 2.5:1 for precise output regulation. Raising the maximum gain to 25 allows a 40 mV–250 mV input range with the output still regulated, better than 6:1. Unfortunately, the bandwidth will be reduced. Bandwidth can be maintained by adding a high frequency op-amp cascaded with the output to make up gain beyond the 10 of the EL4452, current feedback devices being the most flexible. The op-amp's input should be capacitor coupled to prevent gained-up offsets from confusing the level detector during AGC control line variations.

General Disclaimer

Specifications contained in this data sheet are in effect as of the publication date shown. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

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WARNING — Life Support Policy

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