Proceedings of the 5th International Workshop on Thermal Investigations of ICs and Microstructures (THERMINIC), pp. -, October 4-6, 1999, Rome, Italy.

Effect of PCB Thermal Conductivity on the Operating Temperature of an SO-8 Package in a Natural Convection Environment: Experimental Measurement versus Numerical Prediction

John Lohan[1], Pekka Tiilikka[1], Peter Rodgers[2], Carl-Magnus Fager[1], Jukka Rantala[1]

[1] Nokia Research Center, P.O. Box 407, FIN-00045 NOKIA GROUP, Finland
[2] Department of Mechanical & Aeronautical Engineering, University of Limerick, Limerick, Ireland
john.lohan@nokia.com

Abstract

The steady state thermal performance of an isolated SO-8 package is experimentally characterised on five thermal test Printed Circuit Boards (PCBs) and the results compared against corresponding numerical predictions. The study includes the low and high conductivity JEDEC standard, FR4 test PCBs and typical application boards. With each PCB displaying a different internal structure and effective thermal conductivity, this study highlights the sensitivity of component operating temperature to the PCB, provides benchmark data for validating numerical models, and helps one assess the applicability of standard junction-to-ambient thermal resistance (θ_{ja}) data for design purposes on non-standard PCBs. Measurements of junction temperature and component-PCB surface temperature distributions were used to identify the most appropriate modelling methodology for both the component and the PCB.

1 Introduction

As electronic component power densities continue to rise, every effort is made to control operating junction temperature by optimising the thermal resistance chain from the chip, through the package and PCB to the enclosure. Many techniques are used, but increasing pressure to reduce product design cycle times has lead to the widespread use of Computation Fluid Dynamic (CFD) tools that allow different concepts to be quickly assessed at the design stage. However, relying solely on numerical predictions without supporting experimental data still remains an unreliable design strategy as both the modelling methodology and CFD solver capability need to be carefully evaluated. This paper therefore reports on the development of a pragmatic modelling methodology for components mounted on high conductivity PCBs.

While many numerical studies have helped increase awareness of the relationship between component package design and operating temperature, these have also identified that as much as 40% to 96% of a component's power dissipation can enter the PCB by conduction [1-5]. This is also supported by predominantly experimentally based studies that have showed the sensitivity of component operating temperature to the PCB's thermal properties [6-10]. Therefore, as the PCB plays such a critical role, it is important that an accurate, yet pragmatic modelling strategy be used to represent its thermal characteristics, particularly for the complex PCBs in use today.

The challenges involved in modelling such PCBs have largely gone unreported since the majority of joint experimental-numerical studies of this nature have used low conductivity test coupons [11-13] based on the recognised SEMI (Semiconductor Equipment and Materials International) or JEDEC (Joint Electronic Design Engineering Council) specifications [14, 15]. Both standards specify single copper trace layer PCBs, for which a suitable modelling strategy exists [5, 11]. JEDEC recognised that these test PCBs do not represent the multi-layer builds currently used in many applications and recently introduced a high thermal conductivity test PCB [16]. Besides the development work reported by Edwards [17], the authors are unaware of other studies that validate numerical modelling methodologies for these high conductivity PCBs. This paper therefore investigates the significant and critical heat spreading properties of different PCBs, highlights their impact on the operating temperature of the SO-8 component shown in Figure 1, and probes various methods of representing their effective thermal conductivity in CFD based numerical models. Both the small package size of the SO-8 component and its dependence on lead conduction to the PCB made it an instant choice for such a study, as both attributes combine to amplify the sensitivity of it's operating temperature to the PCB's ability to spread heat [10]. The use of a high-density heat source also challenges the applicability of the PCB modelling methodology. Finally, the use of both JEDEC test PCBs as well as typical application PCBs also allows one assess the applicability of standard junction-to-ambient thermal resistance (θ_{ja}) data for design purposes on system PCBs. While acknowledging that standard θ_{ja} data is not meant for design purposes, it is nearly always known and great interest still surrounds understanding its potential to indicate component performance in applications.

The extent of conductive heat spread in FR4 based PCBs is dominated by the presence of nearly or fully complete power and ground copper layers [18]. These layers also serve to reinforce the strong anisotropic properties of the electrically insulating glass fibre also present [19], producing much larger in-plane ($k_{eff,p}$) thermal conductivity values than in the normal or through-plane ($k_{eff,n}$) direction [20]. Numerous empirical and analytical based methods

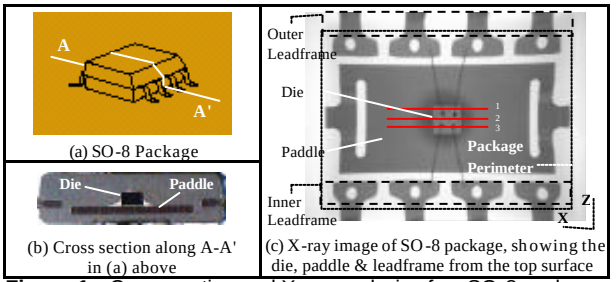


Figure 1– Cross section and X-ray analysis of an SO-8 package.

of estimating these properties have emerged [10, 18, 21] and this study sought to establish the most appropriate calculation method for three different FR4 based PCBs and two based on Insulated Metal Substrate (IMS) technology.

Highlighting the significant difference between the three FR4 PCBs tested, experimental measurements showed a 41°C variation in SO-8 junction temperatures, for the same 0.5 Watt power dissipation level. Based on the calculation method proposed by Punch & Davies [10] the effective, and dominant, in-plane thermal conductivity of these FR4 PCBs ranged from 0.82 W/mK to 36.5 W/mK. However, using these estimates in an anisotropic representation of the PCB lead to a 28°C, or 44%, over prediction in the junction temperature using a validated component model. Such large discrepancies are not uncommon, as Chiriac & Lee [22] reported that prediction accuracy varied from 5%, using a detailed model, to 43% with a simplified model. In this case, the effective thermal conductivity of a Plastic BGA laminate, consisting of similar features to system level PCBs was being investigated, and while an earlier version of the Flotherm CFD code applied in this study was used, these results underline the continued need to verify numerical predictions with experimental data [23].

The present study is seen as a natural progression from the previously published work of Rodgers *et al.* [5, 24], that investigated component behaviour on single-layer, FR4 based PCBs and identified the importance of modelling the surface signal traces. Similar experimental characterisation and pragmatic modelling philosophies are applied in the study, but to higher conductivity test PCBs. Once the heat spreading properties of these boards can be quantified and modeled, it makes it possible to generate design guidelines to minimise PCB thermal resistance in a cost effective and timely manner, early in the design phase.

2 Experimentation

All experimental measurements were performed using SO-8 thermal test components, surface mounted onto single-component PCBs whose design was based on JEDEC standards [15, 16]. All tests were performed in the standard natural convection (still-air) test environment defined by JEDEC [25]. Two samples of each PCB build were tested and while average results are presented in Section 4, maximum variation in junction temperatures between test sample pairs did not exceed 1.8°C, and was typically within 1°C.

2.1 Thermal Test Component

The test component shown in Figures 1 and 2 contained a G423, 0.63 x 0.63mm thermal test die from Infineon [26], with functionality that allowed it dissipate power, while simultaneously allowing the operating junction temperature to be known by monitoring the forward biased voltage across a chip mounted diode [27]. The temperature sensitive diode of each test die was calibrated in accordance with JEDEC standard JESD 51-1 [28] to an accuracy of ±1°C. Package internal architecture details provided by Infineon [29] are presented in Figure 2 and the corresponding thermal conductivity values for each package feature are shown in Table 2.

2.2 Thermal Test PCBs

Cross sectional views of the five test PCBs, showing the location of all signal and plane layers, are presented in Table 1. Two types of signal layers were used and these are both presented in Figure 3, where the size and shape of all the test PCBs is also defined. Figure 3(a) shows the PCB's surface signal layer trace layout defined by JESD 51-3 and 51-7 [15, 16]. This layout is present on one side of FR4 "1", IMS AL and IMS Cu, but on both sides of FR4 "2" and FR4 "3". Note that FR4 "3" also contains two internal signal layers, both covering 20% of the surface area, and the layout of these layers is represented by the hatched pattern in Figure 3(b). Internal plane layers are defined by JESD 51-7 [16] for the high thermal conductivity test PCB and these occupy the area shown by the hatched pattern in Figure 3(b), but have 100% coverage. FR4 "2" and FR4"3" contain 2 and 4 internal plane layers respectively.

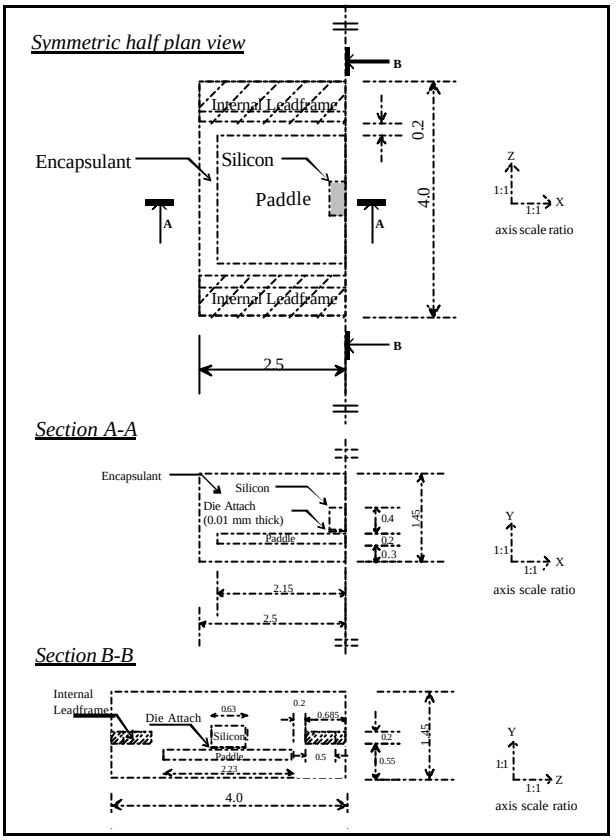
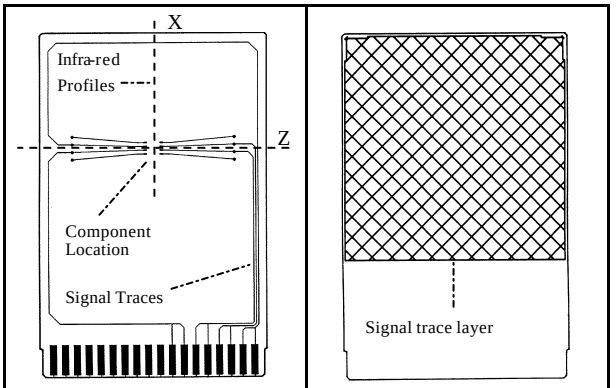


Figure 2 – Internal package architecture for a P DSO-8-1 from Infineon [29].

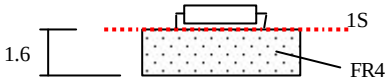
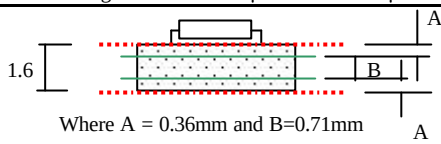
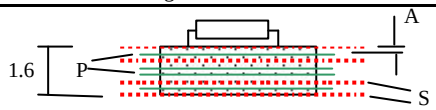
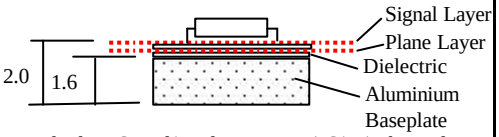
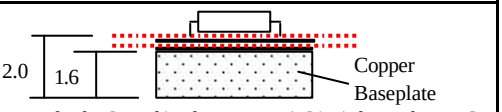


(a) Surface signal layer trace layout to JEDEC standard. Location of the IR profiles is also defined.

(b) Internal signal layer traces in FR4 "3", covering 20% of the area within a 74x74mm region.

Figure 3 – JEDEC Standard single-component thermal test PCB design (76.2 x 114mm) showing recommended surface signal layer trace design [15] and internal signal trace layer in FR4 "3".

Table 1 – Different test PCB constructions used, including both FR-4 based PCBs and IMS based PCBs.

PCB No. & Label	***PCB Constructions :*** *Schematic cross-section and Description*
# 1 – FR4 "1"	 **1S-layer PCB :** Standard 1 Signal-layer (1S) test PCB to JESD 51-3. Cu signal traces are 70 µm thick & 250 µm wide.
# 2 - FR4 "2"	 Where A = 0.36mm and B=0.71mm **2S/2P-layer PCB :** Standard 2 Signal/2 Plane-Layer (2S/2P) thermal test PCB to JESD 51-5. Two 70 µm Cu Signal-layers with 20 % coverage and two internal 35 µm Cu Plane-layers with 100 % Cu coverage.
# 3 - FR4 "3"	 Where A = 0.20 mm, approximately **4S/4P-layer PCB :** Non-standard 4 Signal/4 Plane-Layer (4S/4P) test PCB. Two 70 µm Cu Signal-layers on surfaces and two internal 35 µm Cu Signal-layers with 20 % coverage. Four internal 35 µm Cu Plane-layers with 100 % Cu coverage.
# 4 – IMS Al	 Non-standard 1 Signal/1 Plane-Layer (1S/1P) thermal test PCB. Both the signal and plane layers are 70 µm thick and the dielectric layer is 150 µm thick.
# 5 – IMS Cu	 Non-standard 1 Signal/1 Plane-Layer (1S/1P) thermal test PCB with the same build as IMS Al above.

Note : Signal-layer (S), ·····; Plane-layer (P), ——, Cu refers to Copper and all dimensions are in mm.

2.3 Infra-red Thermography

Infra-red (IR) thermography was used to measure the surface temperature gradients across both the component and PCB. These measurements were used to identify the applicability of the thermal conductivity parameters used to model the PCB and the IR profiles along axes "X" and "Z" shown in Figure 3(a) are presented in Section 4.

Measurements were performed using an Agema Thermovision® 550 infrared imaging system [30], operating in the 3.6 to 5 µm spectral range. The 20° lens used had a field of view of 180 mm that offered a geometric spacial resolution of 0.6 mm at an object distance of 500 mm. In this instance the camera lens was located 400mm from the test PCB surface and the measurement resolution was estimated at 0.45mm. Measurement accuracy was calibrated to an accuracy of ±0.5°C using a cold plate [5, 24].

To avoid emissivity variations all surfaces were covered with a thin layer of paint with a known, uniform emissivity of 0.92. It was noted however that the addition of this paint layer did not change thermal performance, as component operating temperatures remained within 1°C of the original value after the paint was applied.

3 Numerical Analysis

All numerical models were generated using a CFD based tool, Flotherm version 2.1 from Flomerics [31], which is a dedicated software used for thermal analysis of electronic systems. The modelling strategy employed to ensure that predictions were both computational domain and grid independent is outlined by Rodgers et al. [5, 24], and modelling details for the SO-8 component, cold-plate analysis and the PCB convective analysis are presented in the following sections.

3.1 Component Model

Using a pragmatic component modelling approach based on vendor specified nominal package dimensions and material thermal properties presented in Figure 2 and Table 2 respectively, the half-body model of the SO-8 component shown in Figure 4(a) was constructed. However, to avail of symmetrical heat spread indicated by IR measurements in the natural convection environment only a quarter model shown in Figure 4(c) is used. Additionally, it is not possible to model all package elements discretely and in such cases a volume averaged conductivity value is used [5, 11]. This approach was used for both the leadframe and package leads as a comparison of Figure 1(c) with Figure 4(a) indicates.

Table 2 – Vendor specified thermal conductivity values for the various package elements modeled.

Model Element	*Thermal Conductivity, W/mK*
Die	k = 117.5 - (0.42(T'-100))
Die Attach (3 to 5 µm thick)	1.25
Copper Paddle	260
Encapsulant	0.62
Leadframe	260
Package inner leadframe block*	208
Package outer leadframe block*	96.0
Leadframe block*	96.0

Note: * Refers to volume averaged effective thermal conductivity value.

3.2 Cold-Plate Analysis

To build confidence in this component model junction-to-case (θjc) cold-plate measurements, specified by SEMI G30-88 [32], were first conducted. The corresponding numerical model is presented in Figure 4(b) and the grid allocated to the solution domain for both the component and the coldplate is tabulated in Table 3. A complete description of the characterisation technique is provided by Rodgers et al. [5]. However, in this instance a silicone based heat transfer compound with a thermal conductivity of 3.0 W/mK from Electrolube was used.

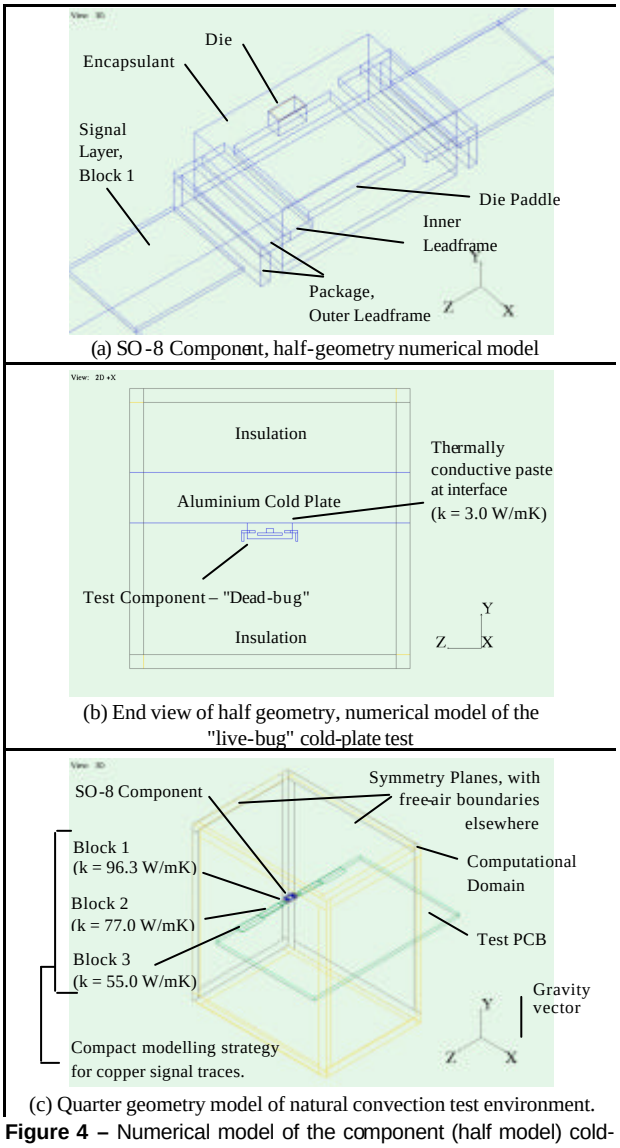
Three test components were studied in both the 'dead-bug', Figure 4(b), and 'live-bug' orientations. Running the cold plate at a steady temperature of 20°C, θjc data was obtained for three power dissipation levels that generated a temperature difference of 25°C, 50°C and 75°C between the junction and the coldplate. Predicted θjc was shown to be very sensitive to the die attach thickness and thermal properties of the molding compound. Experimental measurements in the "dead-bug" orientation gave an average θjc of

82.3°C/W, with maximum variation of ±2.3°C/W, compared with a predicted value of 82.0°C/W, using a vendor specified die attach thickness of 10 µm. In the "live-bug" orientation, predictions overestimated the 51.4°C/W experimental value by 5.6°C/W. However, when the cross sectional inspection shown in Figure 1(b) was carried out on two samples, measurements revealed that the die attach thickness ranged from 3 µm of 5 µm.

Table 3 – Component, coldplate and natural convection enclosure domain sizes and grid allocation.

CA	*Cold Plate*				*Natural Convection*			
	Component		*Full Domain*		*Component*		*Full Domain*	
	(mm)	NC	(mm)	NC	(mm)	NC	(mm)	NC
X	2.5	16	30.0	42	2.5	16	70	51
Y	1.45	12	25.0	56	1.45	12	80	47
Z	4.0	22	25.0	48	2.0	11	50	44

Note: CA = Coordinate Axis in numerical models and
NC = the Number of grid Cells applied



(a) SO-8 Component, half-geometry numerical model

(b) End view of half geometry, numerical model of the "live-bug" cold-plate test

(c) Quarter geometry model of natural convection test environment.

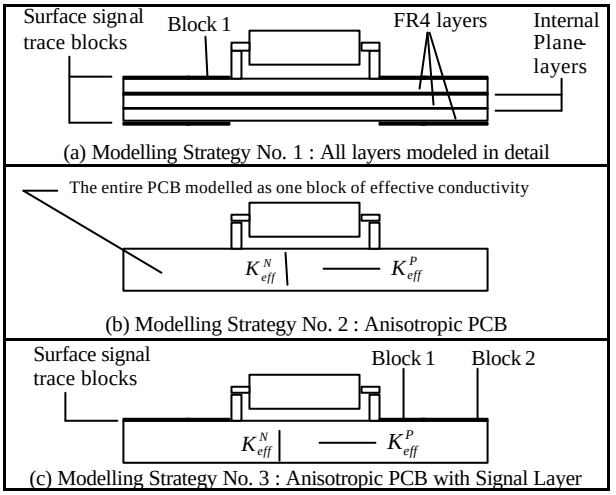
Figure 4 – Numerical model of the component (half model) cold-plate and natural convection test environments.

When the conservative value of 5 µm was modeled, predictions for both the "dead-bug" and "live-bug" orientations underestimated the measured data by 7.3°C/W and 3.4°C/W respectively. Experimental and numerical sensitivity studies showed that variation in the interface resistance due to paste thickness was not an issue. However, this study highlights the sensitivity of junction temperature predictions to the die attach thickness specified and the importance of verifying package internal architecture. As a result, junction temperature predictions for the PCB mounted components were made using both 5 µm and 10 µm die attach thicknesses.

3.3 PCB Convective Analysis

All numerical models of the natural convection environment shown in Figure 4(c) were run using a laminar flow model and the domain size and grid details are presented in Table 3. The volumetric thermal conductivity values used for the PCB surface signal layer were 96.3 W/mK, 77.0 W/mK and 55.0W/mK for blocks 1, 2 and 3 respectively, Figure 4(c). Accepted anisotropic thermal conductivity values of 0.81W/mK and 0.29W/mK were used to represent PCB FR4"1"'s effective thermal conductivity in the in-plane (Keff,p) and through-plane (Keff,n) directions [10, 18].

Recognised modelling strategies for higher conductivity multi-layer PCBs include detailed models as shown in Figure 5(a) [22], anisotropic representations as shown in Figure 5(b) [10,13,18,21] or using isotropic values [21]. However, a fourth option was also investigated and it is presented in Figure 5(c). Based on the cited references the effective thermal conductivity values for FR4"2" and FR4"3" are presented in Table 4.



(a) Modelling Strategy No. 1 : All layers modeled in detail

(b) Modelling Strategy No. 2 : Anisotropic PCB

(c) Modelling Strategy No. 3 : Anisotropic PCB with Signal Layer

Figure 5- Three numerical modelling strategies for representing the effective thermal conductivity of the FR4 test PCBs.

Table 4 – Range of thermal conductivity values used to represent various elements of the FR4 test PCBs modeled.

PCB # and Conductivity		*Effective Thermal Conductivity (W/mK)*			
		(a)	(b)	(c)	(d)
FR4 "2"	Keff,p (XZ)	24.36	17.7	18.6	AM=12.33 GM=2.72
	Keff,n (Y)	0.303	0.32	0.35	
FR4 "3"	Keff,p (XZ)	41.16	34.6	36.5	AM=20.74 GM=3.62
	Keff,n (Y)	0.318	0.34	0.38	

Note: a) standard Series and Parallel resistances [33], b) Azar & Grabner (1996) [18], c) Punch & Davies (1997) [10], d) Culham & Yovanovich (1998) [21]; HM = Harmonic Mean, GM = Geometric Mean.

4 Results and Discussion

To address the objectives of this study the results are presented so that the dependency of the component operating temperature on the test PCB is defined and the effect of using different PCB modelling strategies on prediction accuracy is investigated. Comparing predictions of die junction temperature and component-PCB surface temperature gradients with measurements validated the accuracy of the modelling methodology.

4.1 Effect of the PCB on q_{ja}

Measured junction temperatures are presented in Figure 6 and the corresponding θja data is presented in Figure 7. The significant impact of copper layers in the PCB is shown by a 40% reduction in θja between the FR4 PCBs. A further reduction of 20% is offered by the IMS PCBs. Note also in Figure 7 that θja is independent of power dissipation level and that little reduction is seen as the in-plane effective conductivity exceeds approximately 50 W/mK, Figure 8. However, it is also clear from the 0.5 Watts data in Figure 8 that the sensitivity of the operating temperature to the PCB conductivity increases with component power dissipation level.

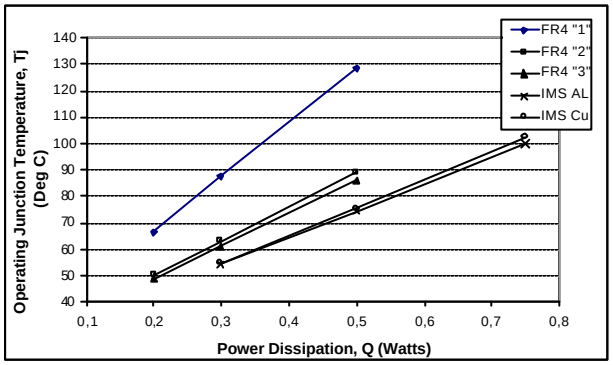


Figure 6 - Effect of Power Dissipation Level on the Operating Junction Temperature, as a function of the PCB Constructions in Table 1.

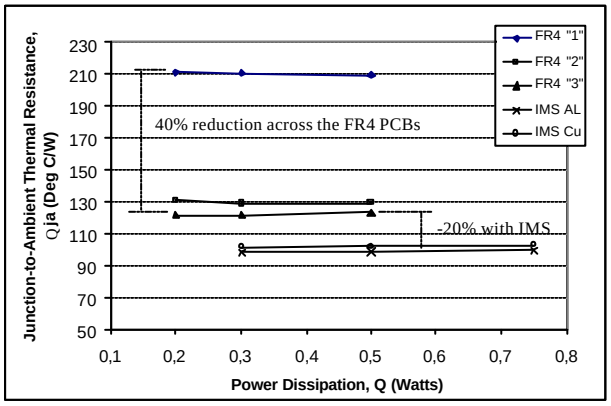


Figure 7 - Effect of Power Dissipation Level on the Junction-to-Ambient Thermal Resistance, as a function of the PCB Constructions shown in Table 1.

The values of in-plane conductivity presented in Figure 8 were based on the expressions defined by Punch and Davies [10] for multi-layer FR4 PCBs, Table 4. The in-plane effective conductivity values used for the IMS PCBs were calculated using parallel resistances [33] and equaled 164 W/mK and 328 W/mK for the aluminium and copper substrates respectively.

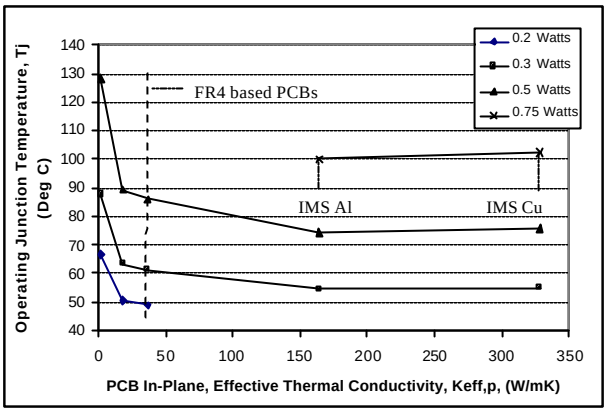


Figure 8 - Operating Junction Temperature versus PCB In-Plane Effective Thermal Conductivity (Keff,p) [10] as a function of power dissipation.

4.2 Effect of PCB on Conductive Heat Spread

The IR surface temperature gradients presented in Figure 9 highlight the dependency of PCB conductive heat spread on it's construction. In this instance the power dissipation is held constant at 0.5 Watts and significant differences exist between both JEDEC based FR4"1" and FR4"2" PCBs, with little difference between the latter and the application PCB FR4"3". This suggests the better applicability of the high conductivity JEDEC standard test PCB to application type PCBs. Reflecting the lowest operating temperatures measured, one notes negligible resistance on the IMS substrates, with approximately 90% of the temperature rise above ambient due to the component's internal resistance.

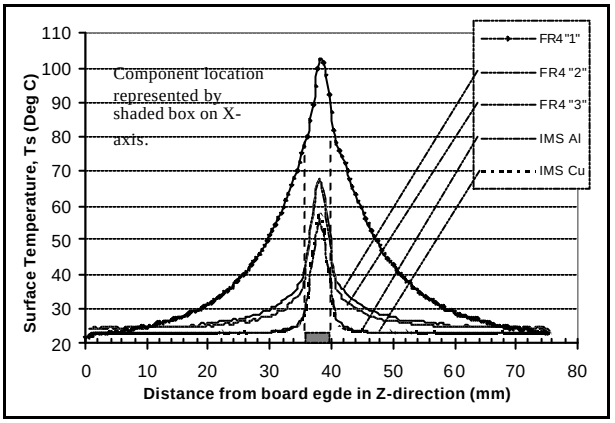


Figure 9 - Infra-Red profiles in Z-direction (Figure 3a), for a 0.5 Watt power dissipation level.

4.3 PCB Effective Thermal Conductivity and Numerical Modelling

The junction temperature prediction accuracy obtained using the different PCB modelling strategies in Figure 5 is presented in Table 5, with the associated temperature gradients in Figures 10 and 11. Using the 5 µm die attach thickness the prediction accuracy using the detailed modelling strategy number 1 is within ±6.8°C.

However, prediction accuracy decays to almost 30°C when the modelling detail is relaxed to a sole anisotropic representation defined by strategy number 2, Figure 5(b), but the addition of the signal trace blocks defined by strategy number 3 produced best accuracy overall. The importance of modelling the signal traces can be seen by comparing the prediction accuracy from strategy number 2 and 3 in Table 5. Therefore, PCB modelling strategy number 3 is proposed for this package type as it approximates the thermal properties of the PCB internal structure, but also includes the direct conduction path from the component leads to the PCB by including the surface signal traces. Edwards' [17] earlier numerical study identified the importance of the latter heat transfer path. The impact of component lead contact area with the PCB was also modeled by including a cuboid representing the leadfoot. This was shown to reduce predicted temperatures, thereby further improving prediction accuracy, but by no more than 1.7°C.

Table 5 - Comparison of measured and predicted junction temperatures for the three different modelling strategies, using a die attach thickness of 5 µm, and 0.5 W power dissipation.

PCB Type	*Measured Temperature (°C)*	*Numerical Discrepancy(°C)*		
		# 1	*# 2*	*# 3*
FR4 "1"	124.3	- 3.1 (+ 0.6)		
FR4 "2"	84.9	+ 6.8 (+ 11.6)	+28.7 (+ 32.6)	+ 3.2 (+ 7.0)
FR4 "3"	83.3	+ 3.7 (+ 7.6)	+24.9 (+ 28.7)	+ 1.5 (+ 5.4)
IMS Cu	71.5	+ 5.0 (+ 8.9)	+ 2.2 (+ 6 .2)	
IMS Al	70.6	+ 6.5 (+ 10.4)	+ 3.9 (+ 7.8)	

Note: Data in Parenthesis relates to a die-attach thickness of 10µm.

Considering the heat spread to the PCB, Figure 10 shows close agreement between measurement and predictions obtained from the detailed modelling of FR4 "1", using anisotropic values of the PCB conductivity. While a discrepancy is shown on the component surface, this results from the poor temperature spatial resolution of the IR camera, which averaged surface temperature over approximately 1.5 mm. As a result, lower peak temperatures are measured, but Table 5 shows that prediction accuracy was within 3.1°C of measurement.

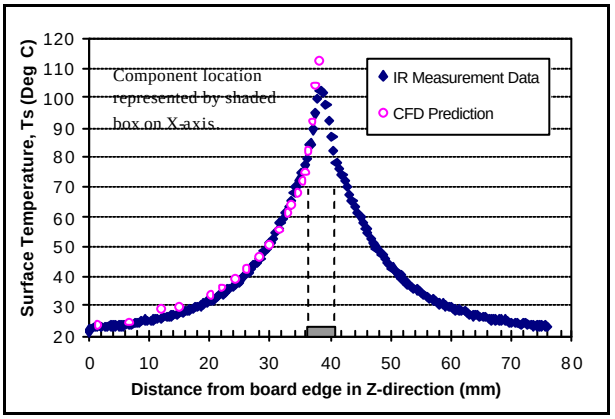
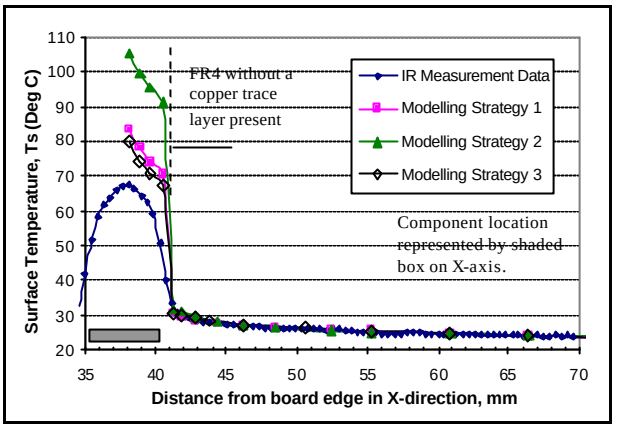
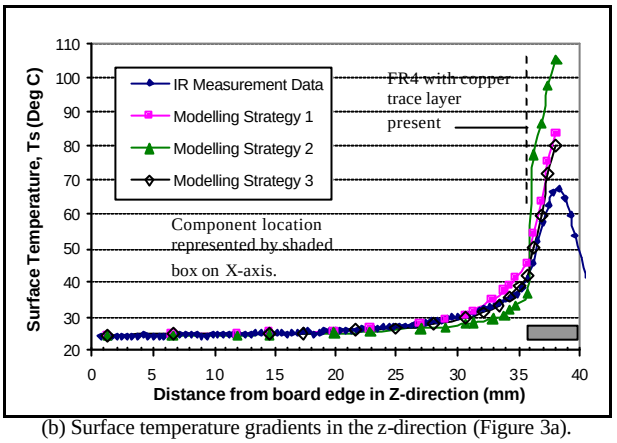


Figure 10 – Comparison of IR surface temperature profile from FR4 "1", with that predicted using anisotropic PCB representation of the FR4 and including the signal traces, for 0.5 Watts power dissipation. Die attach thickness was 5 µm.

The IR temperature profile shown in Figure 11 highlights that the three PCB modelling strategies are capable of capturing the heat spread when surface signal traces are absent, Figure 11(a), but discrepancies exist close to the component when they are present, Figure 11(b). Further work is required to account for these differences.



(a) Surface temperature gradients in the X-direction (Figure 3a).



(b) Surface temperature gradients in the z-direction (Figure 3a).

Figure 11 - Comparison of IR surface temperature profile from FR4 "2", against that predicted by different numerical modelling strategies for the PCB conductivity. Power dissipation was 0.5 Watts and the die attach thickness was 5 µm.

The importance of modelling the leads and PCB signal traces is emphasised by the results of a numerical energy balance study presented in Table 6, that identifies lead conduction as the dominant heat transfer path. Note that this path is sensitive to the PCB boundary condition as the proportion of power dissipated through the leads increases by 7.5% across the range of PCBs studied, bringing the total power loss to the PCB to 94% on the IMS PCBs.

Table 6 – Component energy balance on different PCB constructions for 0.5 W power dissipation level, using PCB Modelling Strategy #1 and a 5 µm die attach thickness.

Heat transfer path	*Percentage of Total Power Dissipation (%)*			
	FR4 # 1	*FR4 # 2*	*FR4 # 3*	*IMS Cu*
Lead	72.4	74.0	75.1	79.9
Base	14.3	16.9	16.6	14.3
Sides	7.9	5.7	5.2	3.5
Pkg. Top Surface	5.4	3.4	3.1	2.3

5 Conclusions

- Highlighting the importance of the PCB construction, measured variation in component operating temperature across the five PCBs studied was 54°C for a 0.5 Watt power dissipation level.
- Component operating temperature displays greatest sensitivity to the PCB construction, when PCB effective thermal conductivity is less than 50 W/mK.
- The high conductivity JEDEC test PCB produced standard junction-to-ambient thermal resistance data that was within 3°C/W of values recorded on the typical application PCB tested. This compares with a difference of 83°C/W using the JEDEC low conductivity test PCB.
- Prediction accuracy was shown to be sensitive to the specification of the package internal architecture, particularly the die attach thickness, which was verified by cross sectional inspection. The use of this type of inspection is advocated for detailed numerical modelling.
- Junction temperature prediction accuracy was also shown to be very sensitive to the modelling strategy employed to represent the PCB construction, with prediction accuracy ranging from 1.5°C to 29°C.
- The importance to modelling the PCB's surface signal layers was highlighted and a new modelling strategy has been proposed which minimises the need for modelling detail and in this case also preserves prediction accuracy. The applicability of this approach to other package types and operating environments is to be further investigated.

Acknowledgements

The authors gratefully acknowledge the cooperation of: Infineon for supplying the thermal test components; Bergquist for supplying the IMS test PCBs; Cai Kabrell (Nokia Professional Mobile Radio) for providing the IR Camera; and both Jianxiong Chen and Timo Autiokari (Nokia Telecommunications) for performing the structural analysis.

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