TECHNICAL PUBLICATION

Controlling Impedances When Nets Branch Out

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ABSTRACT

It is not uncommon for a driver to drive numerous receivers. In some designs it is impractical, or undesirable, to drive every receiver from a single trace segment. In such cases it is common to design a trace that branches out into two or more branches, each serving a select number of receivers. The question then becomes where to place the branch point. Improper placement of the branch point can have serious implications from an impedance discontinuity standpoint, resulting in reflections that can have signal integrity consequences. This paper describes several ways to deal with the branching problem in designs if they come up.

CONTROLLED IMPEDANCE

When a driver sends a signal down a trace, the signal reflects back from the end of the trace toward the driver. In most cases this reflection is inconsequential. In some circumstances, however, the reflection can be significant enough to cause a signal integrity problem.

The magnitude of the reflection depends (in part) on the relationship between the propagation time of the signal down the trace and the rise (or fall) time of the signal. It is generally agreed that signal reflections can become signal integrity issues when the propagation time down the trace approaches or exceeds about one-half the rise time of the signal. The trace length at which the propagation time equals one-half the rise time is called the "critical length." If signal reflections can become a signal integrity issue, there is typically a two-stage process designers go through to control the problem:

- Design the trace to look and perform like a transmission line with characteristic impedance Zo
- Terminate the trace using one of several well known techniques[1] to absorb the reflection.

Traces that are designed to look and act like transmission lines are called "controlled impedance" traces. Impedance control is typically obtained through the control of the geometry of the trace. The characteristic impedance of a trace is primarily determined by the trace width, the distance between the trace and nearby reference plane(s), and the relative dielectric constant of the material(s) surrounding the trace. It is also secondarily affected by the trace thickness. In dealing with controlled impedance traces it is important that the impedance remain constant everywhere along the trace. If there is an impedance discontinuity at any point along the trace, a reflection may be created at that point which may then cause a signal integrity problem for the circuit.[2]

Constant impedance generally means uniform geometry, something that is not hard to maintain if the trace is totally contained on one individual trace layer. When signal traces move from one trace layer to another, however, some aspects of the geometry may change (the distance to the plane(s), the relative dielectric coefficient, etc.) In such cases, it is entirely possible that the trace width may need to be different on different layers in order to achieve a constant impedance at all points along the trace. Most board designers understand this and have no problems with this aspect of board design.

There is a situation, however, where the rule "the impedance must be constant everywhere along the trace" confuses some designers, especially those without a strong technical background. Consider the situation illustrated in Figure 1. The figure illustrates a driver, UA, driving a signal down a trace with characteristic impedance ZoA. The trace branches into two or more branches, each with its own characteristic impedance shown in Figure 1 as ZoB1, ZoB2, …, ZoBn. A designer may interpret the rule as meaning that each of these individual branches must have the same impedance as the initial segment from the driver. That is, as meaning that:

ZoB1 = ZoB2 = --- = ZoBn = ZoA

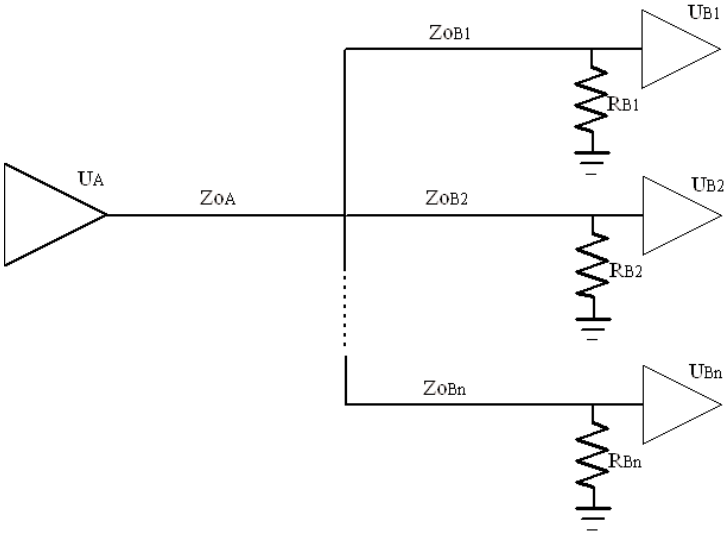
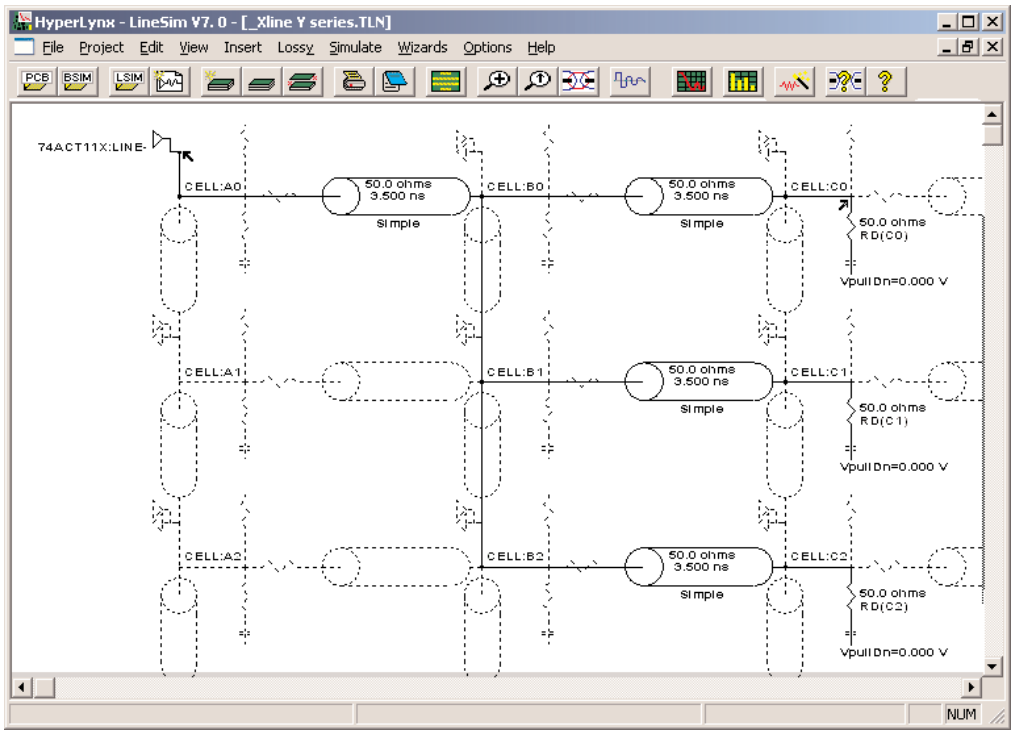


Figure 1: A trace branching into several other traces.

People with a strong technical background understand that this is an incorrect interpretation of the rule. The trace segments after the branch point are all in parallel. If they all have the same impedance, and if that impedance is equal to ZoA, then the parallel combination of all of them appears to the system as being a single trace segment with characteristic impedance ZoA /n. Thus, the system sees an impedance discontinuity at the branch point, and a reflection may well develop at that point.

Mentor Graphics HyperLynx tool is well suited for simulating this situation. Figure 2a illustrates a Hyperlynx model for such a simulation with a single trace branching into three others, all with the same characteristic impedance (in this case, 50 Ohms), and Figures 2b and 2c illustrate the result of this simulation.

The result of the simulation illustrates the classic characteristics of a transmission line terminated with an impedance significantly less than the characteristic impedance of the trace.3



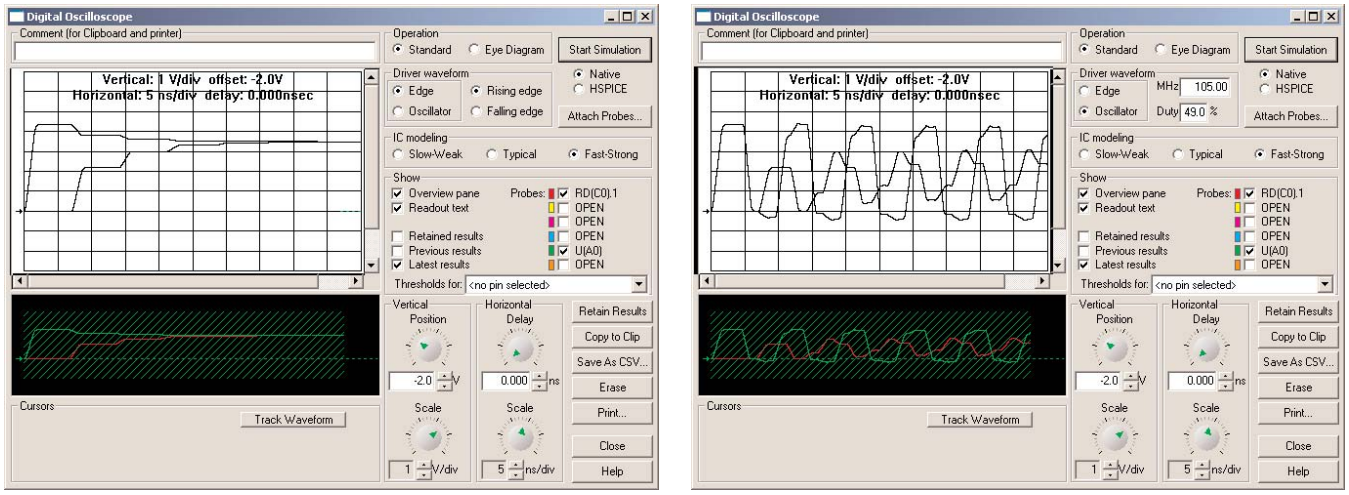


Figure 2: Hyperlynx simulation of one trace branching into three. The model is shown in a (top). Simulation results are shown for step function b (left) and for a square wave c (right)

There are three possible ways to correct the design issue illustrated in Figure 1. These are shown in Figure 3 for the simple case (for convenience) where a single trace branches into two. They are:

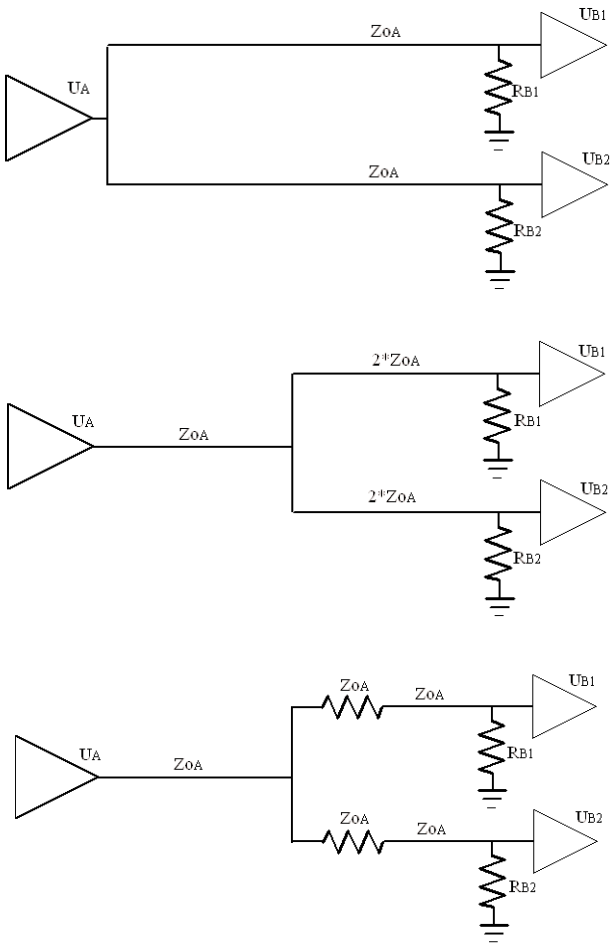


Figure 3: Here are three solutions to the branching problem. Bring the branch back close to the driver (a, top). Increase the impedance of the traces after the branch (b, middle). Add a series resistor to each branch immediately after the branch point (c, bottom).

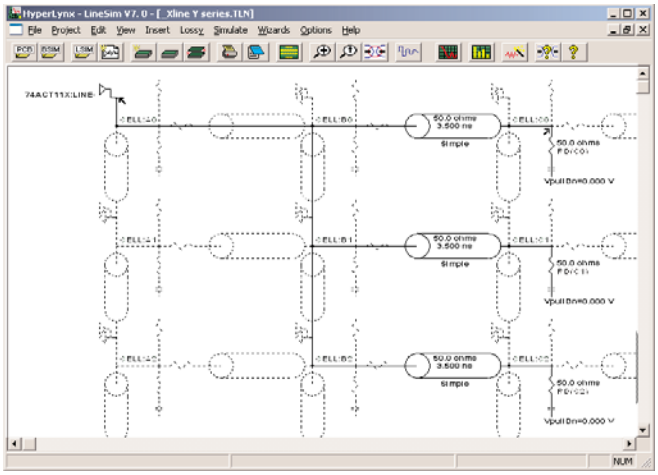
There are three alternatives to consider.

1. Move the branch point back near the driver UA. In general, designs are usually acceptable if the first segment length from UA to the branch point is less than the critical length of the trace, although most engineers and designers would opt for a trace segment much shorter than that --- ideally as short as practical. Most drivers are fairly tolerant of the loads they are driving (up to the maximum output of the driver), so that the impedance at the drive point is normally not an issue. There are a small number of special cases, however, where the driver must drive a trace with a specific impedance, making this solution more difficult. The practical issue with this solution is that layout constraints may make it difficult to move the branch point suitably close to the driver.

2. Adjust the trace impedances after the branch so that each segment has an impedance equal to n times ZoA. Each segment would then be terminated in a resistor whose value was equal to the adjusted impedance, also n times ZoA. That is, as shown in the Figure, RB1 = RB2 = 2*ZoA. This is a very nice approach, except that increasing the impedance of these trace segments typically means reducing their width (unless it is possible to move the segments do a different trace layer with different impedance characteristics.) It is sometimes impractical to fabricate trace widths small enough to achieve the impedance targets.

3. Add a resistor to each trace segment immediately after the branch point whose value is (n-1)* ZoA. The impedance of each individual trace after the branch as seen by the driver at the branch point becomes (n-1)* ZoA + ZoA = n* ZoA. The parallel combination of all branches is then equal to n* ZoA /n = ZoA, and there is no impedance discontinuity at the branch point. The practical issue with this solution is the addition of n resistors to the circuit. Each resistor also forms a voltage divider with the trace reducing the ultimate signal level at the receiver.

The Hyperlynx tool can easily simulate each of these alternatives. Figures 4, 5 and 6 illustrate the simulations for each of these solutions for cases where a single trace branches into three. In each case the improvement over the simulation in Figure 2 is apparent.



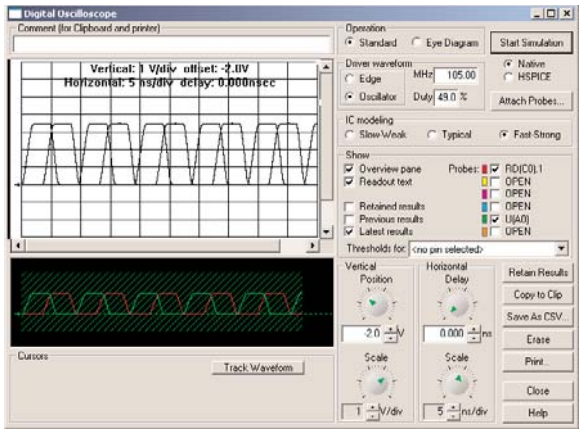
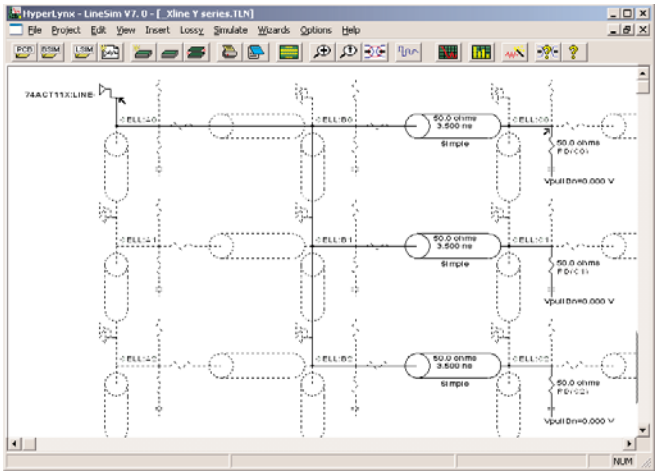


Figure 4: One solution is to bring the branch point back close to the driver. A (top) illustrates the model used and b (above) illustrates the result of the simulation.



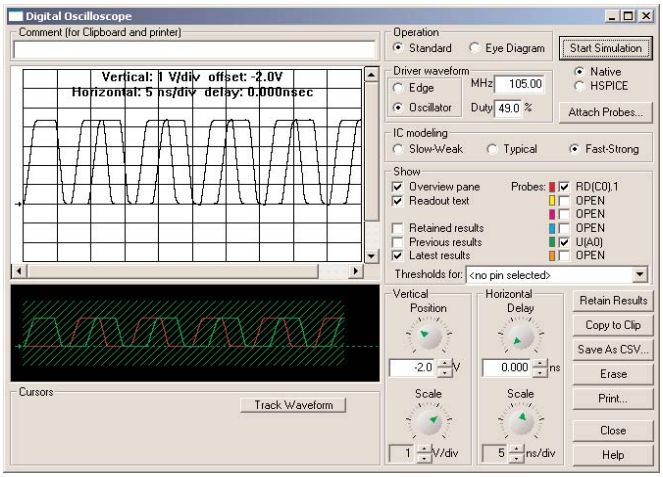
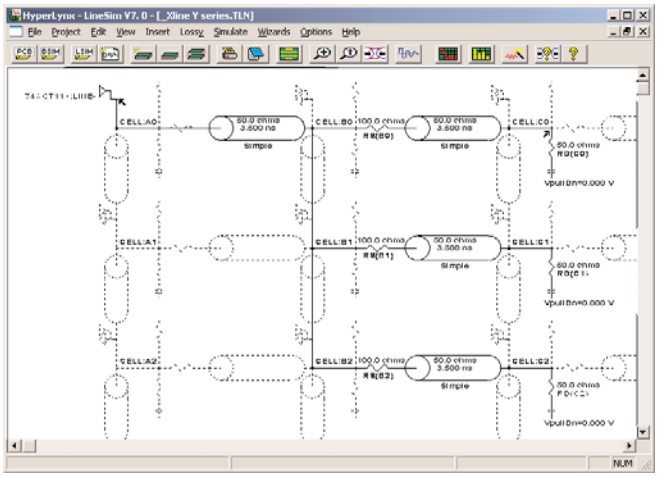


Figure 5: A second solution is to increase the characteristic impedance of the traces following the branch. The model is illustrate in a, (bottom left) and the results of the simulation in b (above). In some designs it may not be practical to achieve the higher impedances needed.



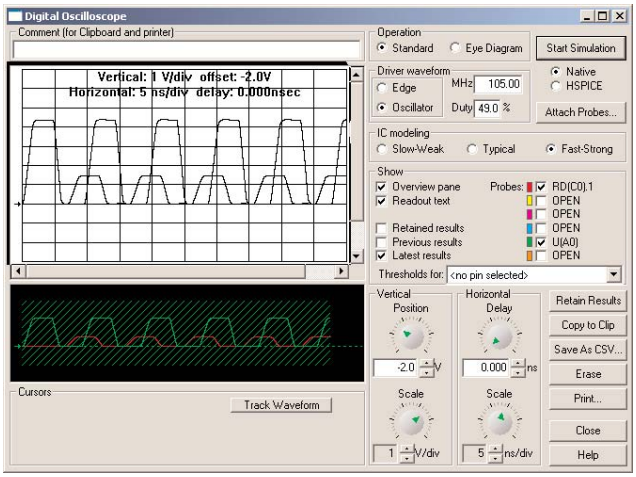


Figure 6: A third possible solution is to add a series resistor in each branch immediately after the branch. A (middle) illustrates the model used and b (above) illustrates the result of the simulation. Note that this solution results in a smaller signal waveform at the receiver.

We have designed boards for customers where the practical constraints prevented us from fully implementing any of these solutions. It was necessary to find the best compromise that allowed the circuit to work "well enough" to meet overall system requirements. Customers with the Hyperlynx simulation tool are able to model different alternatives and evaluate the simulation results, helping them zero in on the best practical design criteria.

SUMMARY

When it is necessary to divide a net into two or more branches, the best approach is to bring the branch point back as close as possible to the driver. If the branch point is some distance away from the driver, especially as distant as the critical length or more, special design techniques are required. Otherwise, impedance discontinuities and damaging reflections might result. Two other possible alternatives are:

1. Increase the controlled impedance of each branch to a level equal to n*Zo, where n is the number of branches and Zo is the impedance of the first trace segment between the driver and the branch. Each branch would then be terminated in a resistor equal to n times Zo. This approach results in a clean signal at each receiver, but it can be difficult to implement if the target impedance requires traces that are too narrow.

2. Add a series resistor to each brance at the branch point equal to (n-1)*Zo, where n and Zo are defined as in the previous paragraph. This technique results in a clean, but reduced, signal at each receiver.

FOOTNOTES

1. For an excellent discussion on termination techniques see Ethirajan and Nemec, "Termination Techniques for High Speed Buses," EDN, February 16, 1998, p. 135. (This article is available through the EDN on-line archives.)
2. See Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Chapters 10 and 11 for a thorough discussion of reflections and transmission line design principles on circuit boards.
3. See Brooks (footnote 2) Chapter 11 for several illustrations of simulations of a variety of improperly terminated traces.

ABOUT THE AUTHOR

Douglas Brooks has a BS and an MS in Electrical Engineering from Stanford University and a PhD from the University of Washington. During his career has held positions in engineering, marketing, and general management with such companies as Hughes Aircraft, Texas Instruments and ELDEC.

Brooks has owned his own manufacturing company, and he formed UltraCAD Design Inc. in 1992. UltraCAD is a service bureau in Bellevue, WA, that specializes in large, complex, high density, high-speed designs, primarily in the video and data processing industries. Brooks has written numerous articles through the years, including articles and a column for Printed Circuit Design magazine. Prentice Hall published his book *Signal Integrity Issues and Printed Circuit Board Design* in 2003. He has been a frequent seminar leader at PCB Design Conferences, and has presented seminars around the world, including Moscow, China, Japan, and Taiwan. His primary objective in his speaking and writing has been to make complex issues easily understandable to those individuals without a technical background. You can visit his web page at http://www.ultracad.com and e-mail him at doug@ultracad.com.

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