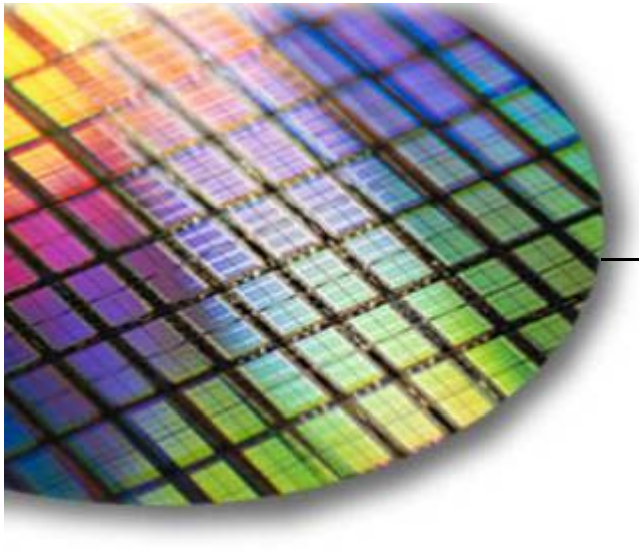

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A Practical Guide to High-Speed Printed Circuit Board Layout

John Ardizzoni
Analog Devices

Dennis Falls
Avnet Electronics Marketing

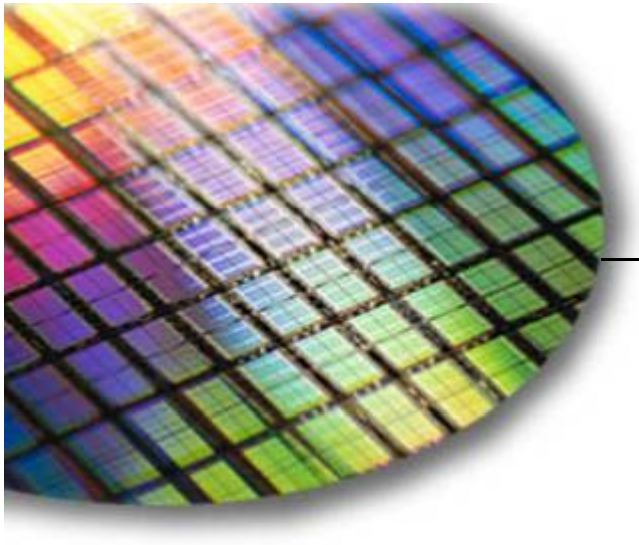
ANALOG DEVICES

Agenda

- Overview
- Schematic
- Location, location, location
- Trust no one
- Power supply bypassing
- Parasitics
- Ground and power planes
- Packaging
- RF Signal routing and shielding
- Checking the layout
- Summary

Overview

- PCB layout is one of the last steps in the design process and often one of the most critical
- High-speed circuit performance is heavily dependant on layout
- A high-performance design can be rendered useless due to a poor or sloppy layout
- Today's presentation will help:
  - Improve the layout process
  - Ensure expected circuit performance is achieved
  - Reduce design time
  - Lower cost
  - Lower stress for you and the PCB designer



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Schematic

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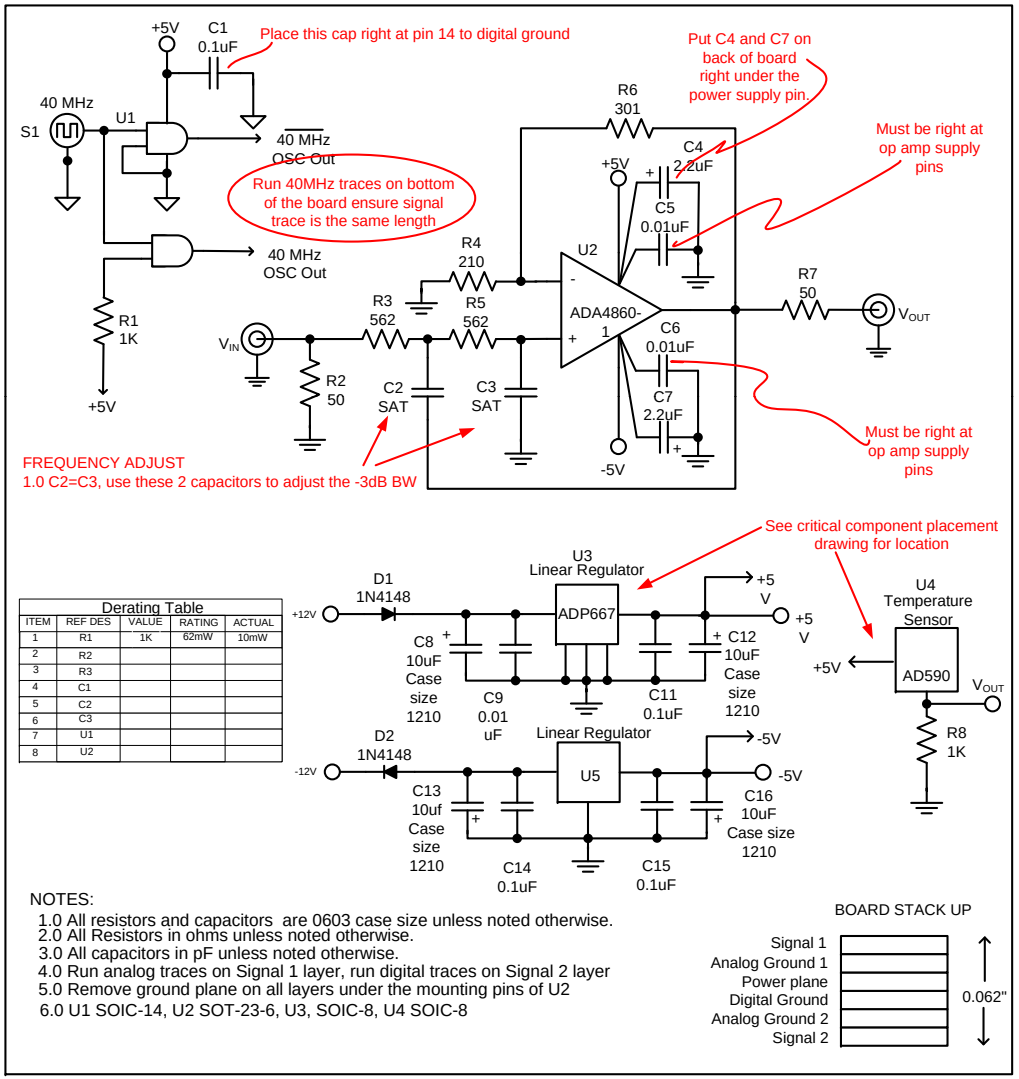
Schematic

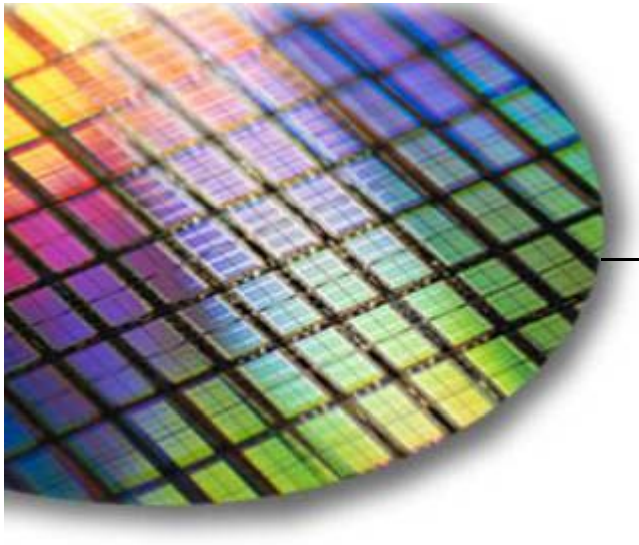
- The strength of any structure (including PCB's) is only as good as the foundation on which it built upon!
- A good layout starts with a good Schematic!
- Schematic flow and content
- Include as much information as you can
- What should you include?

Items to Include on a Schematic

- Notes
- Component tolerances and case sizes
- Part numbers (internal/external/alternative)
- Board stack up
- Tests or alignment procedures
- Power dissipation
- Controlled impedance and line matching
- Component de-rating
- Thermal requirements
- Keep outs
- Mechanical considerations
- Critical component placement
- Warning flags
- What ever else you can think of!

Schematic


+5V
C1
0.1uF
Place this cap right at pin 14 to digital ground
Put C4 and C7 on back of board right under the power supply pin.
40 MHz
S1
U1
40 MHz
OSC Out
Run 40MHz traces on bottom of the board ensure signal trace is the same length
R6
301
C4
2.2uF
C5
0.01uF
Must be right at op amp supply pins
R4
210
R3
562
R5
562
U2
ADA4860-1
R7
50
VOUT
VIN
R1
1K
R2
50
C2
SAT
C3
SAT
C6
0.01uF
C7
2.2uF
-5V
Must be right at op amp supply pins
FREQUENCY ADJUST
1.0 C2=C3, use these 2 capacitors to adjust the -3dB BW
See critical component placement drawing for location
U3
Linear Regulator
D1
1N4148
+12V
ADP667
+5 V
C8
10uF
Case size
1210
C9
0.01 uF
C11
0.1uF
C12
10uF
Case size
1210
U4
Temperature Sensor
AD590
VOUT
R8
1K
D2
1N4148
-12V
Linear Regulator
U5
-5V
C13
10uf
Case size
1210
C14
0.1uF
C15
0.1uF
C16
10uF
Case size
1210
Derating Table
ITEM
REF DES
VALUE
RATING
ACTUAL
1
R1
1K
62mW
10mW
2
R2
3
R3
4
C1
5
C2
6
C3
7
U1
8
U2
NOTES:
1.0 All resistors and capacitors are 0603 case size unless noted otherwise.
2.0 All Resistors in ohms unless noted otherwise.
3.0 All capacitors in pF unless noted otherwise.
4.0 Run analog traces on Signal 1 layer, run digital traces on Signal 2 layer
5.0 Remove ground plane on all layers under the mounting pins of U2
6.0 U1 SOIC-14, U2 SOT-23-6, U3, SOIC-8, U4 SOIC-8
BOARD STACK UP
Signal 1
Analog Ground 1
Power plane
Digital Ground
Analog Ground 2
Signal 2
0.062"



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Location, location, location!

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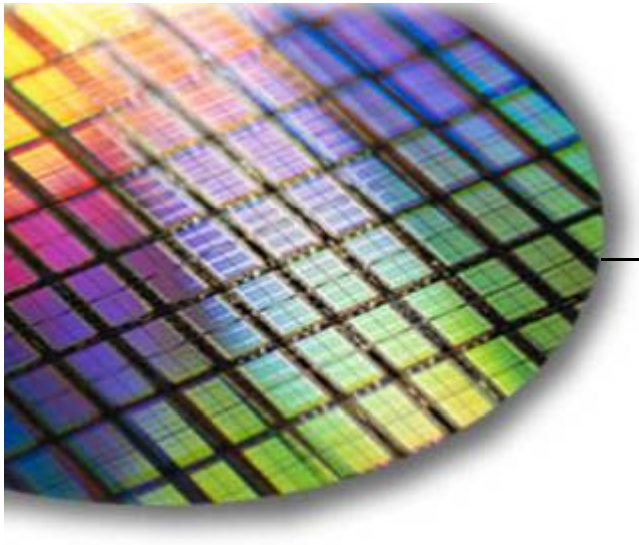
Location, Location, Location

- ***Just as in real estate location is everything!***
- ***Input/output and power connections are typically defined…Everything else is undefined***
  - ***Critical component placement***
  - ***Signal routing***
  - ***Circuit and component proximity***



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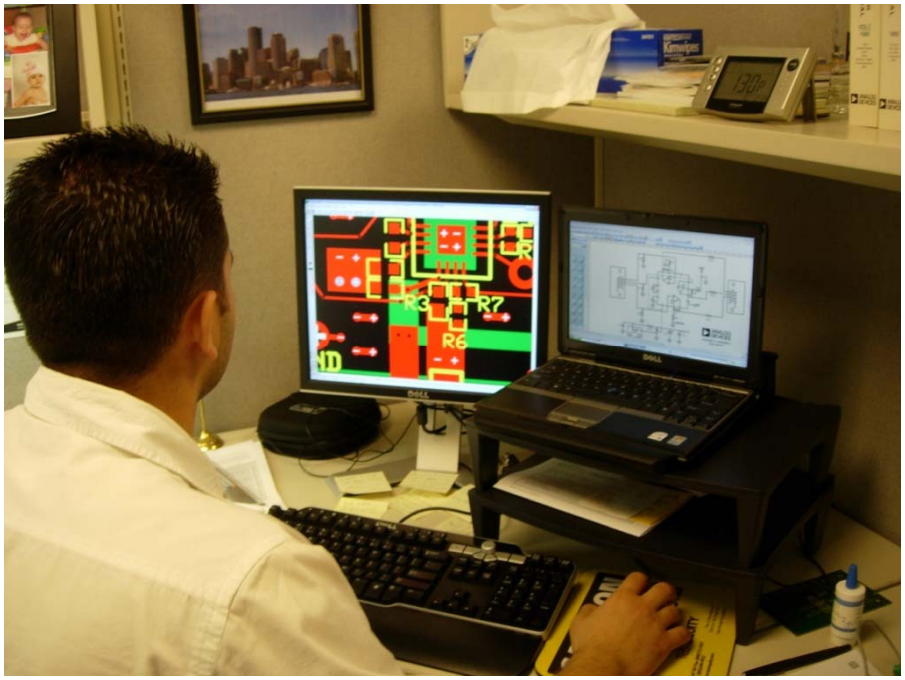
Trust No One

ANALOG DEVICES

Trust No One

- If you're doing your own layout, that's one thing.
- If you're not ….



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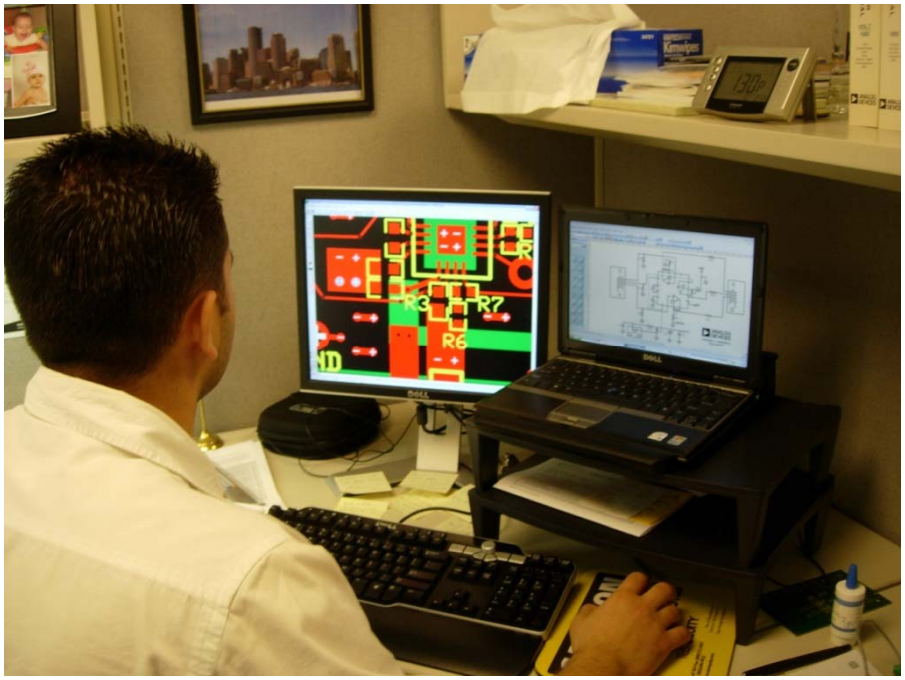

Trust No One

- If you're doing your own layout, that's one thing.
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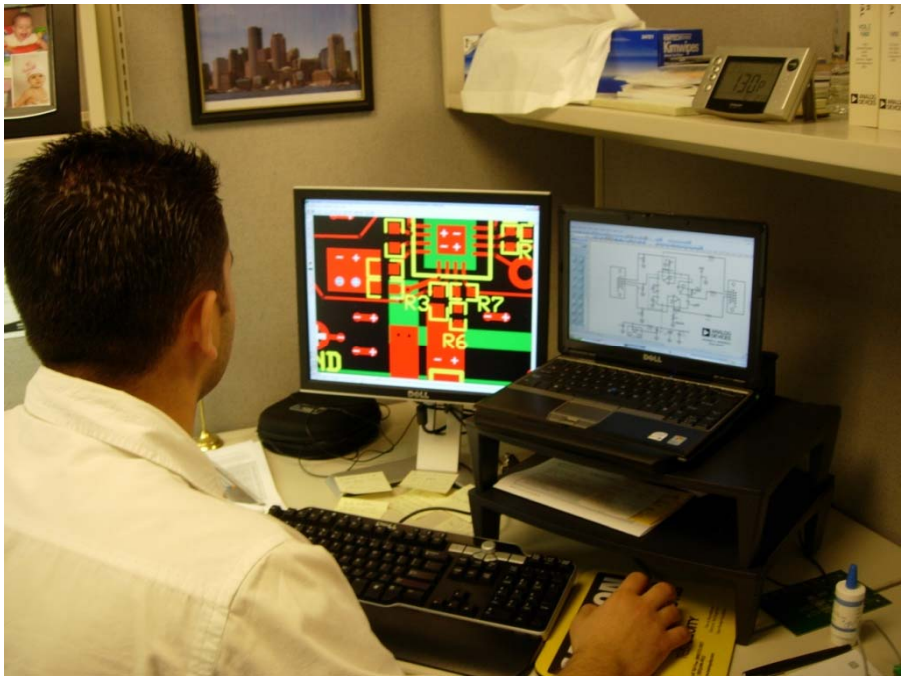
  - In the end you're responsible for making it work!



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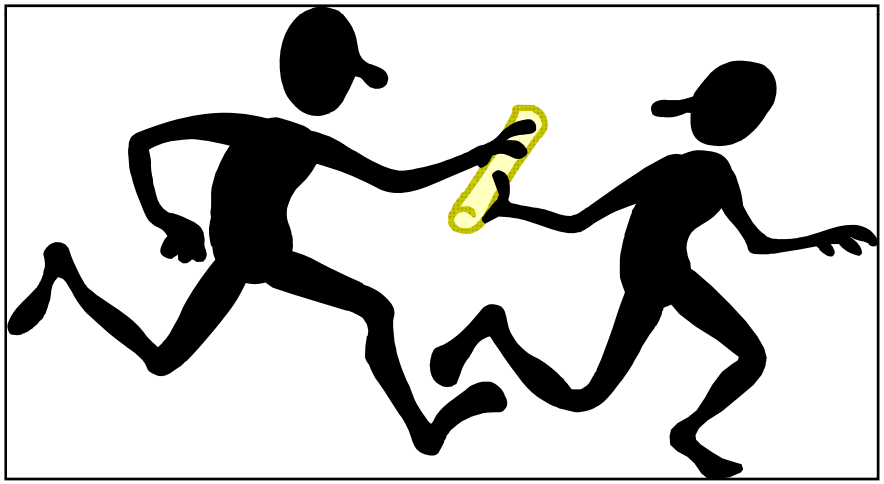
  - You're responsible for making it work!
- When working with the CAD Group



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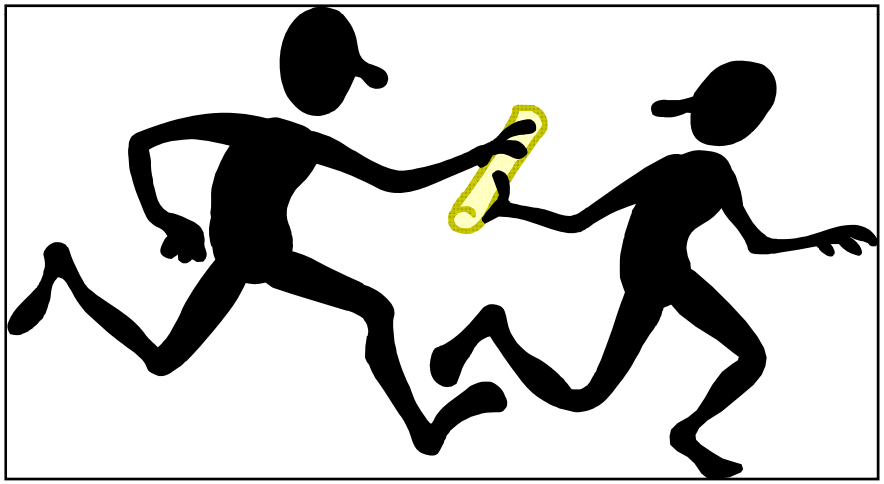
- When working with the CAD Group
  - Make sure you and the designer are on the same page



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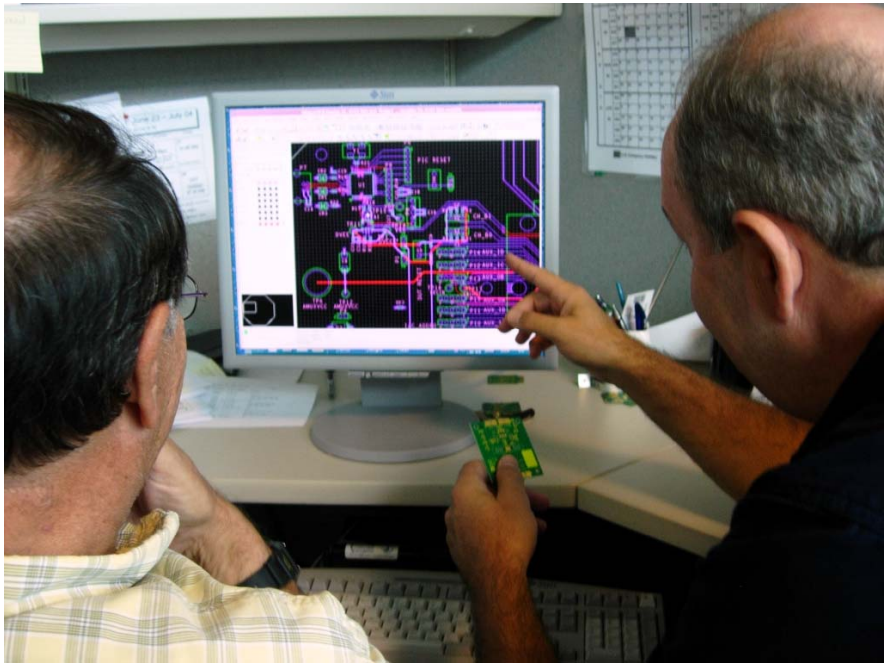
- When working with the CAD Group
  - Make sure you and the designer are on the same page
  - Brief circuit explanation



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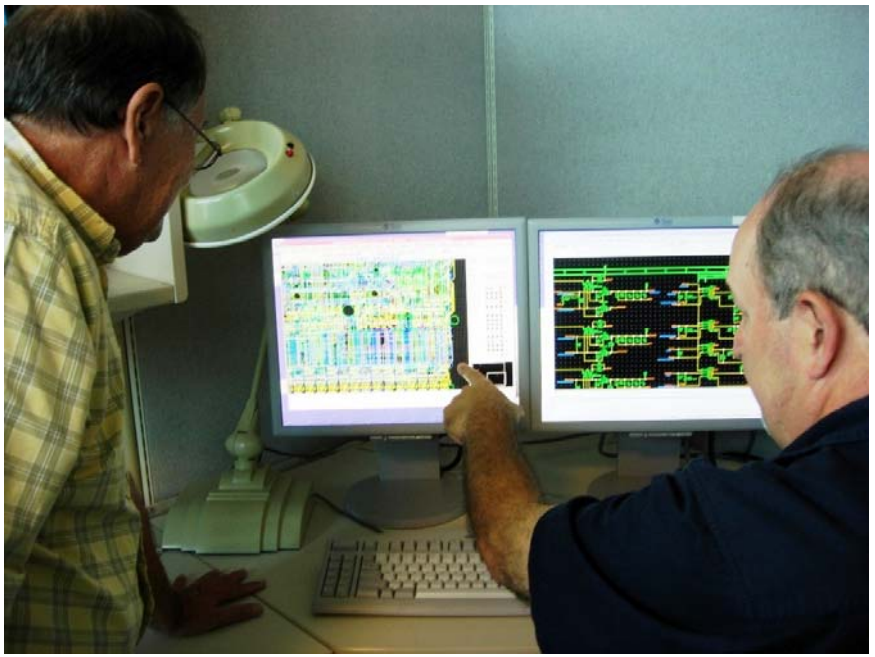
  - Critical component placement



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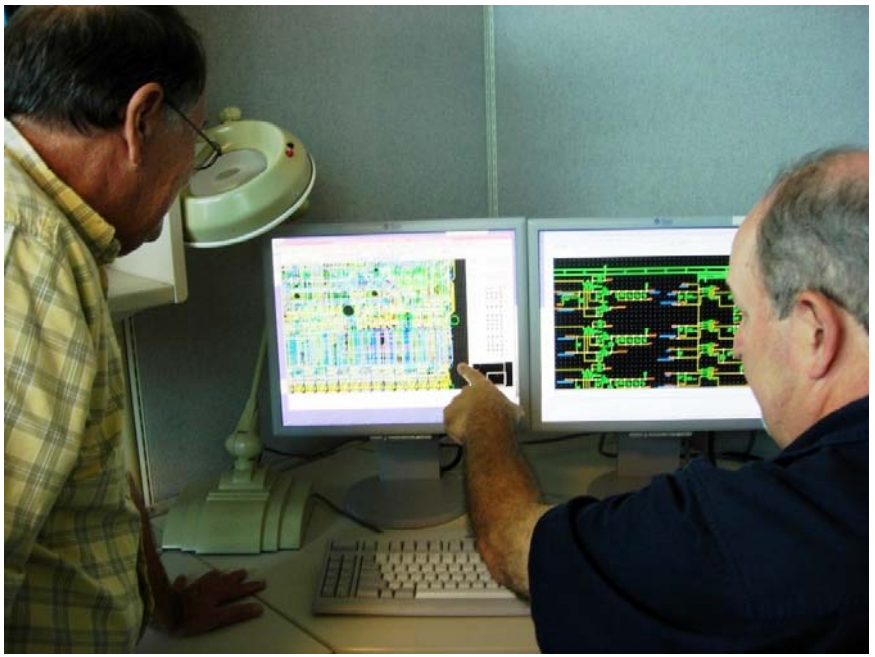
  - Make sure you and the designer are on the same page
  - Brief circuit explanation
  - Critical component placement
  - Input/Output connections



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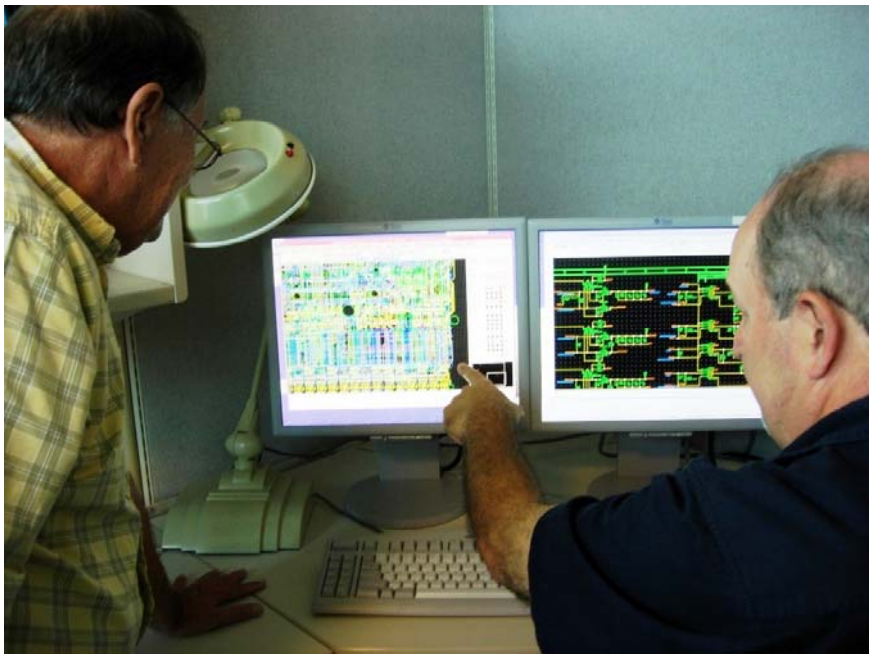
  - Make sure you and the designer are on the same page
  - Brief circuit explanation
  - Critical component placement
  - Input/Output connections
  - Board outline drawing and stack up



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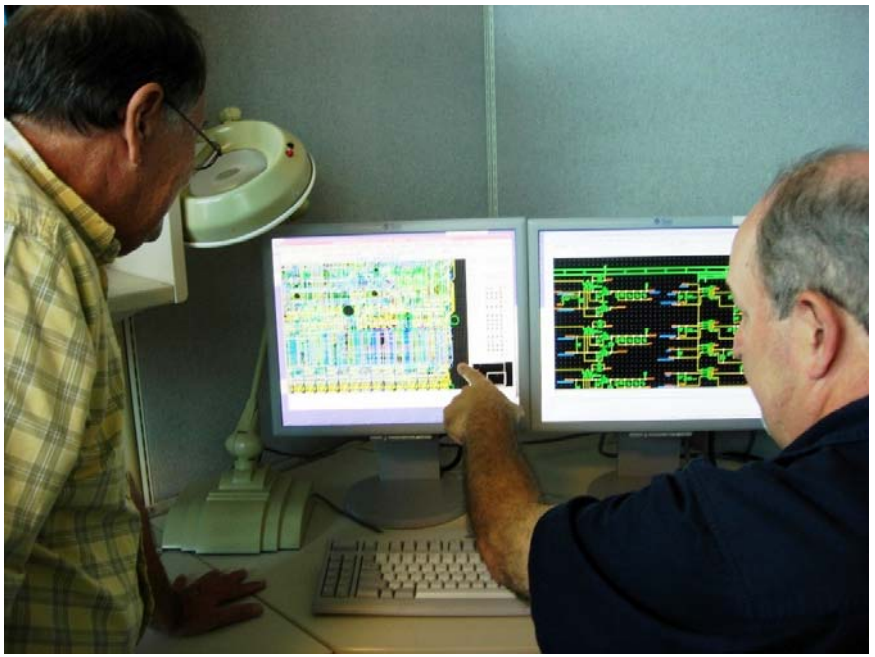
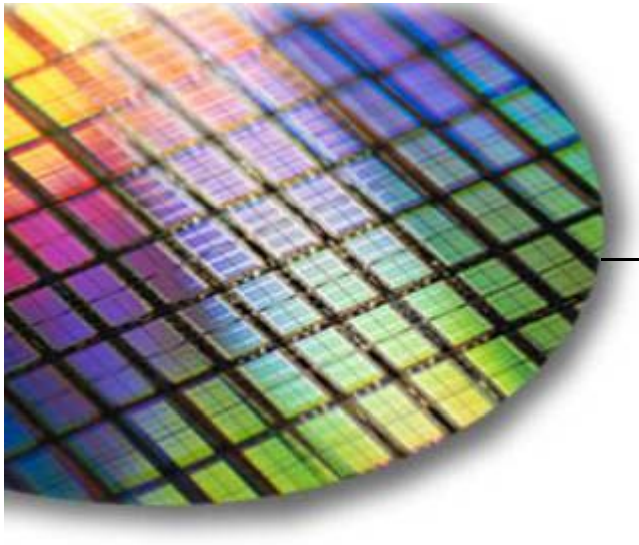
  - You're responsible for making it work!
- When working with the CAD Group
  - Make sure you and the designer are on the same page
  - Brief circuit explanation
  - Critical component placement
  - Input/Output connections
  - Board outline, stack up
  - Tell them to call you if they have a question!





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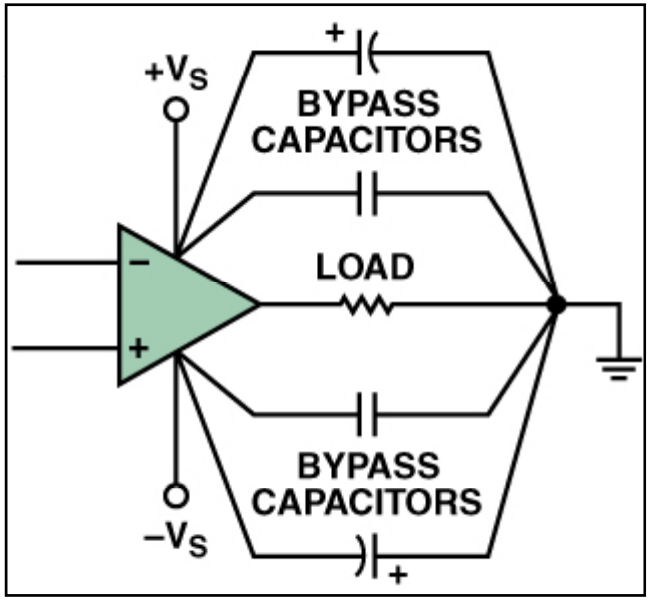
Power Supply Bypassing

ANALOG DEVICES

Power Supply Bypassing

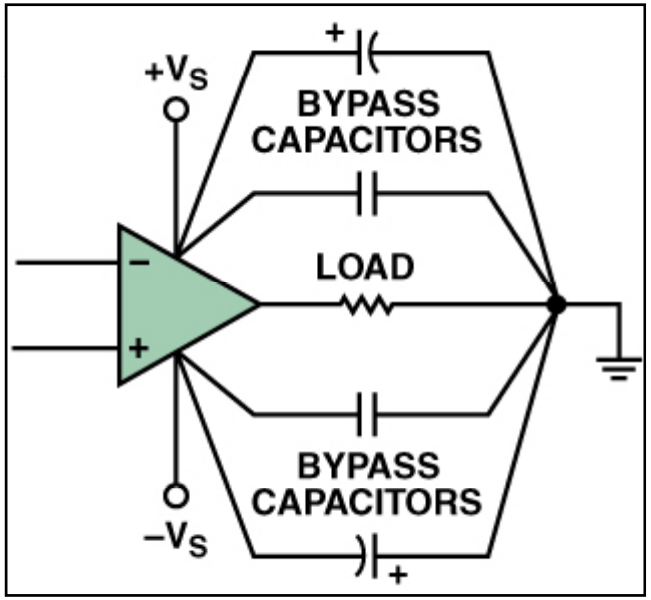
- **Bypassing is essential to high speed circuit performance**



ANALOG DEVICES

Power Supply Bypassing

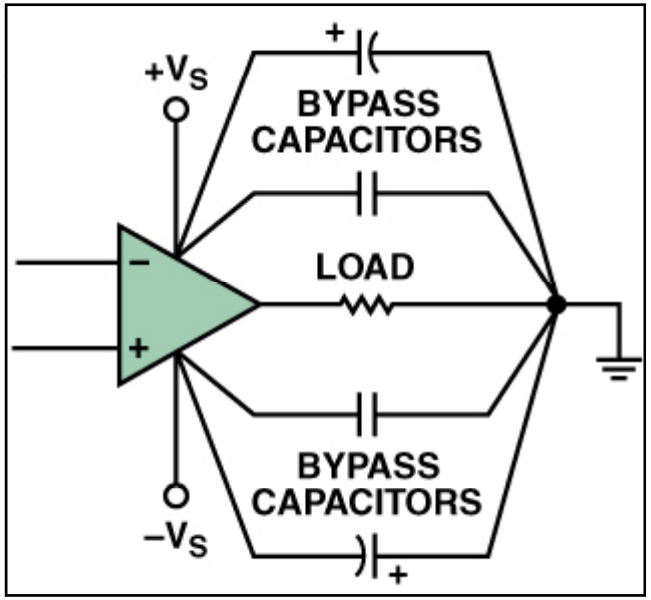
- **Bypassing is essential to high speed circuit performance**
- **Capacitors right at power supply pins**



ANALOG DEVICES

Power Supply Bypassing

- **Bypassing is essential to high speed circuit performance**
- **Capacitors right at power supply pins**
  - **Capacitors provide low AC impedance to ground**
  - **Provide local charge storage for fast rising/falling edges**



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- **Bypassing is essential to high speed circuit performance**
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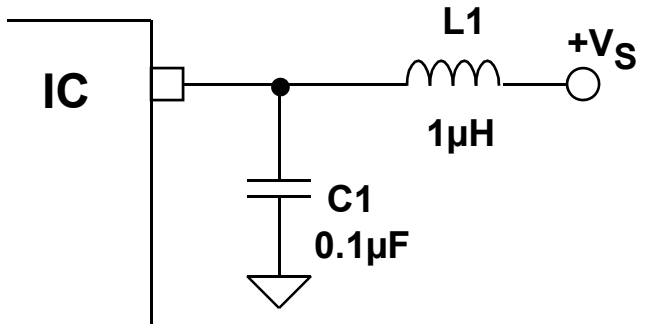
  - **Provide local charge storage for fast rising/falling edges**
- **Keep trace lengths short**



EQUIVALENT DECOUPLED POWER LINE CIRCUIT RESONATES AT:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

f = 500kHz

ANALOG DEVICES

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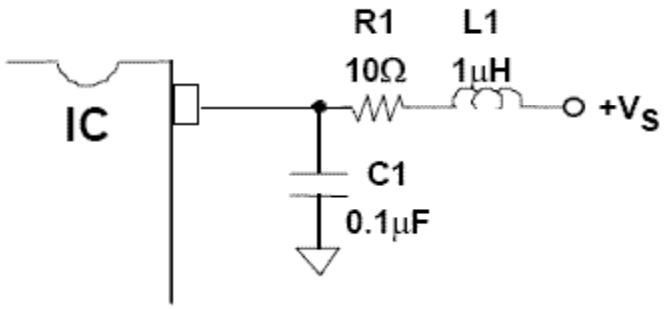

SMALL SERIES RESISTANCE CLOSE TO IC REDUCES Q

ANALOG DEVICES

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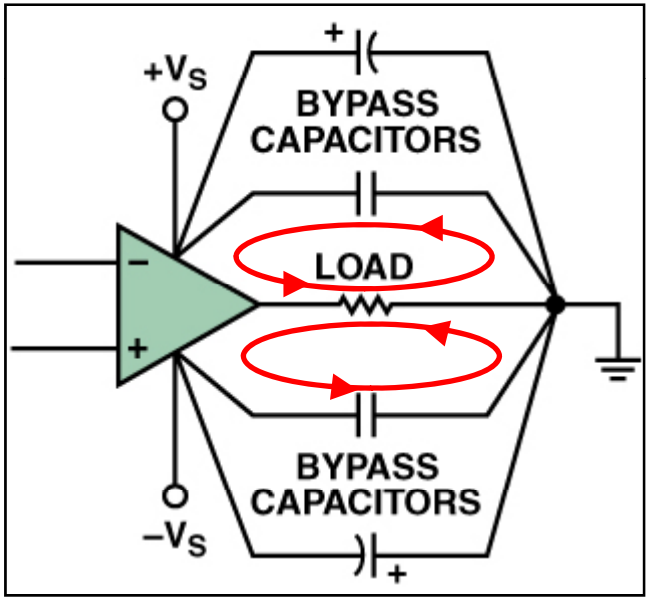
  - **Provide local charge storage for fast rising/falling edges**
- **Keep trace lengths short**
- **Close to load return**
  - **Helps minimize transient currents in the ground plane**



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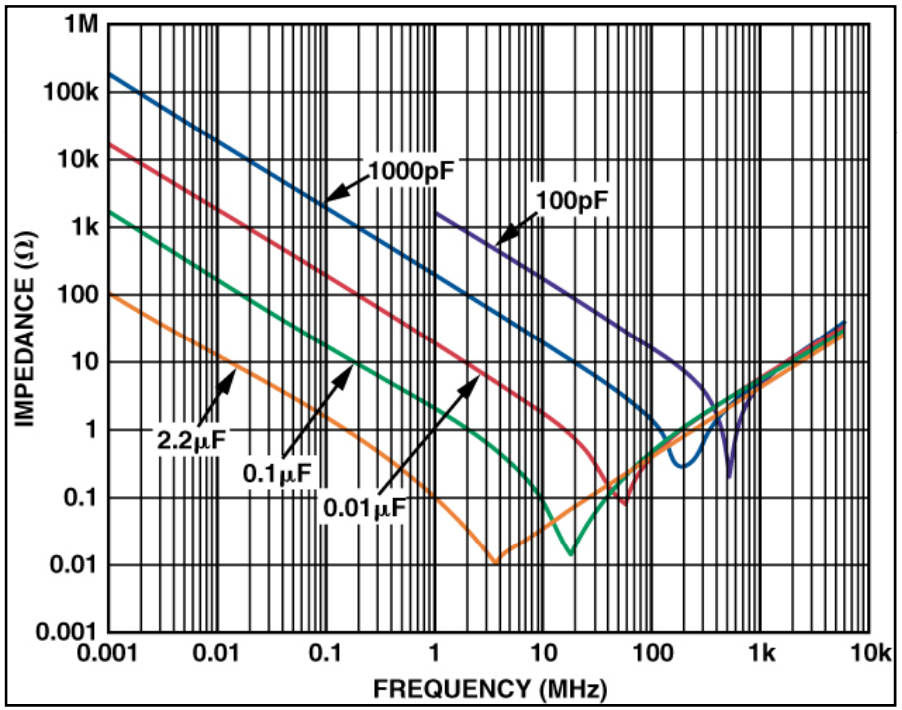
- **Values**
  - Individual circuit performance



ANALOG DEVICES

Power Supply Bypassing

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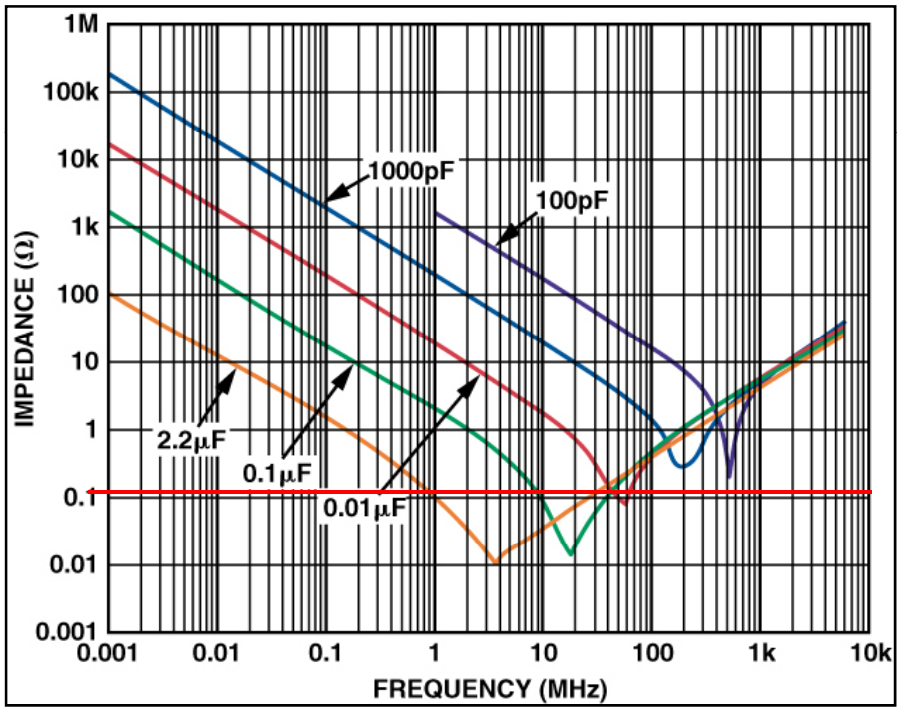
- **Keep trace lengths short**
- **Close to load return**
  - Helps minimize transient currents in the ground plane
- **Values**
  - Individual circuit performance
  - Maintains low AC impedance



ANALOG DEVICES

Power Supply Bypassing

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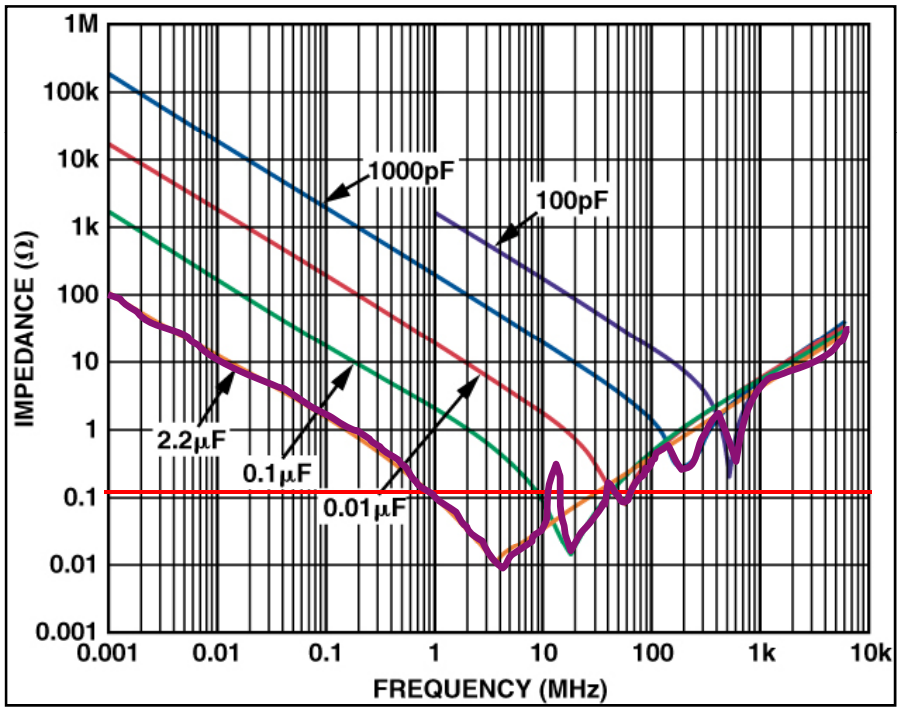
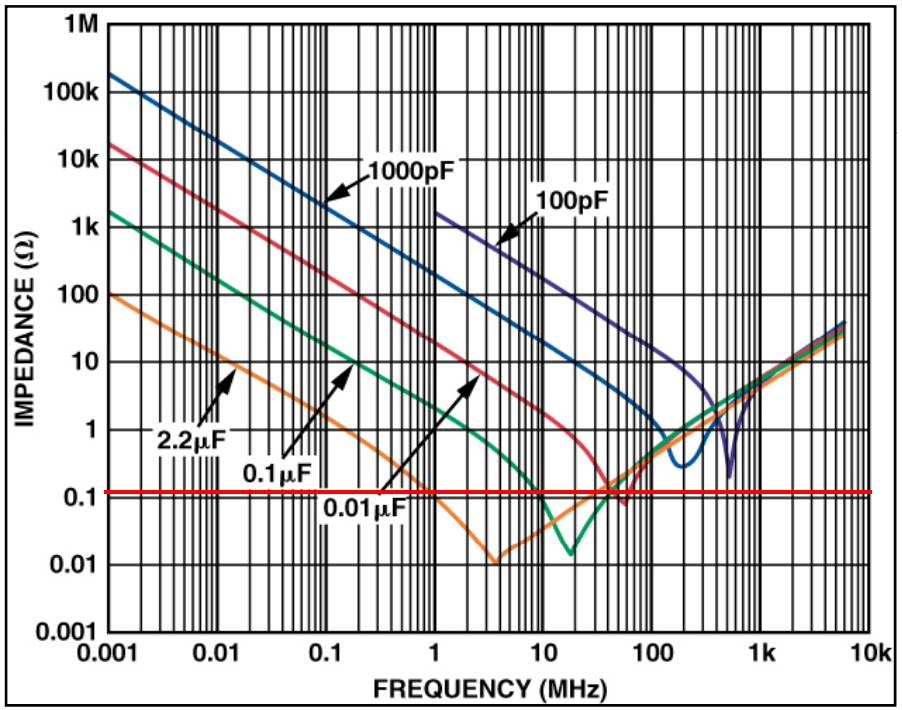
- **Capacitors right at power supply pins**
  - Capacitors provide low AC impedance to ground
  - Provide local charge storage for fast rising/falling edges
- **Keep trace lengths short**
- **Close to load return**
  - Helps minimize transient currents in the ground plane
- **Values**
  - Individual circuit performance
  - Maintains low AC impedance
  - Multiple resonances



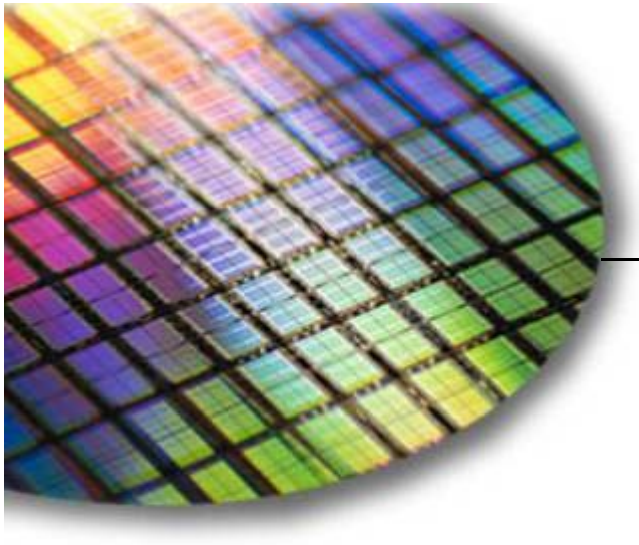
ANALOG DEVICES

Power Supply Bypassing

- **Bypassing is essential to high speed circuit performance**
- **Capacitors right at power supply pins**
  - Capacitors provide low impedance AC return
  - Provide local charge storage for fast rising/falling edges
- **Keep trace lengths short**
- **Close to load return**
  - Helps minimize transient currents in the ground plane
- **Values**
  - Individual circuit performance
  - Maintains low AC impedance
  - Multiple resonances
- **Ferrite beads**



ANALOG DEVICES



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Parasitics

ANALOG DEVICES

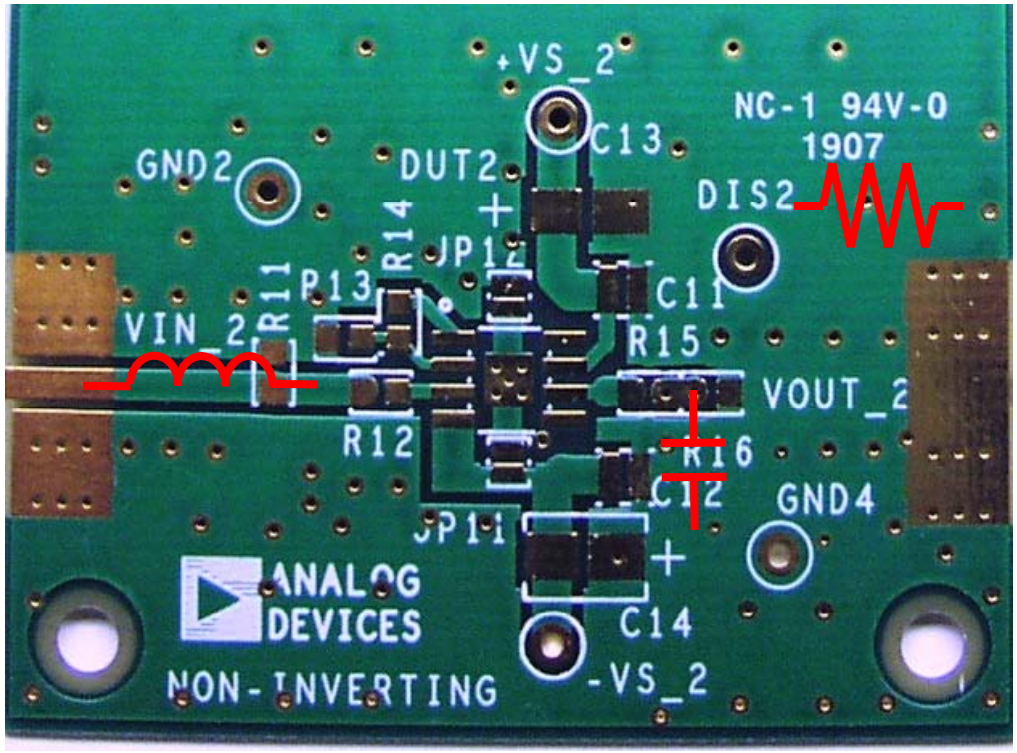
Parasitics

- **Parasite –** ***An organism that grows, feeds, and is sheltered on or in a different organism while contributing nothing to the survival of its host.***

- ***Parasitics in high-speed PCB's, can destroy circuit performance!***

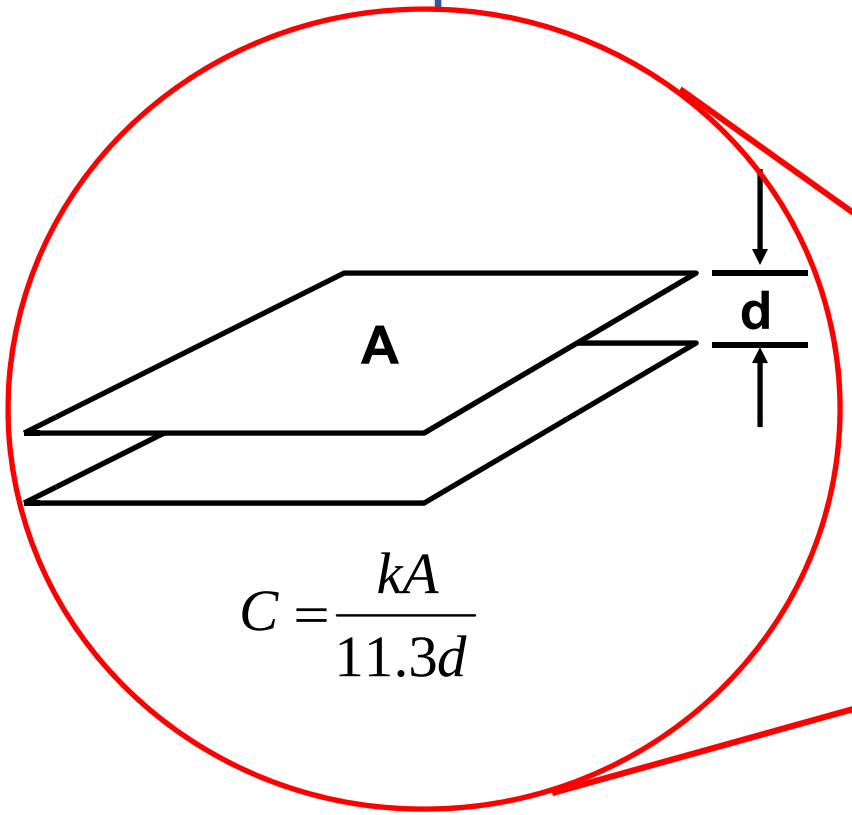
Parasitics

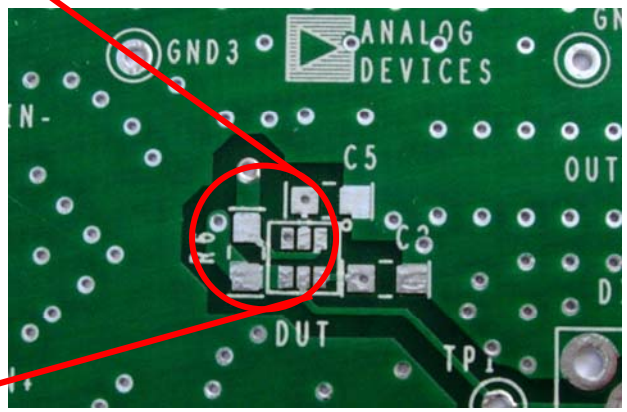
- PCB parasites take the form of undesired capacitors, inductors and resistors embedded within the PCB
- Parasitics are extremely difficult to remove from a PCB
- Prevention is the best method to minimize parasitics



ANALOG DEVICES

Trace/Pad Capacitance





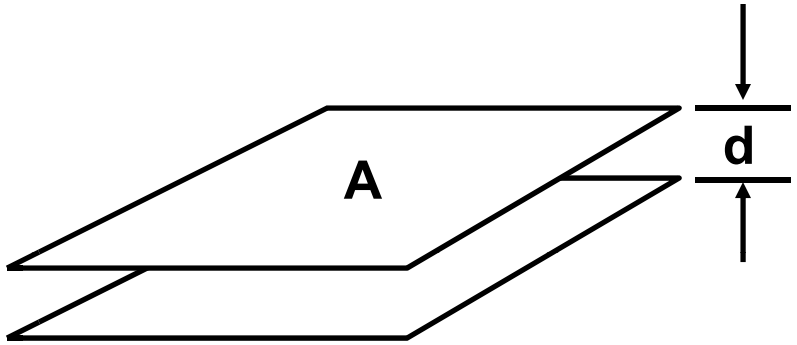
K = relative dielectric constant

A = area in cm²

d = spacing between plates in cm

ANALOG DEVICES

Trace/Pad Capacitance



$$C = \frac{kA}{11.3d}$$

K = relative dielectric constant
A = area in cm²
d = spacing between plates in cm

Example: Pad of SOIC

L = 0.2cm W = 0.063cm

K= 4.7

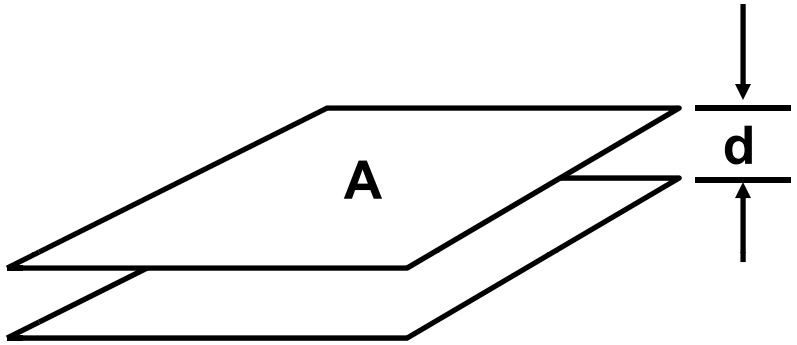
A = 0.0126cm²

d = 0.073cm

C = 0.072pF

ANALOG DEVICES

Trace/Pad Capacitance



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Example: Pad of SOIC

L = 0.2cm W = 0.063cm

K= 4.7

A = 0.0126cm²

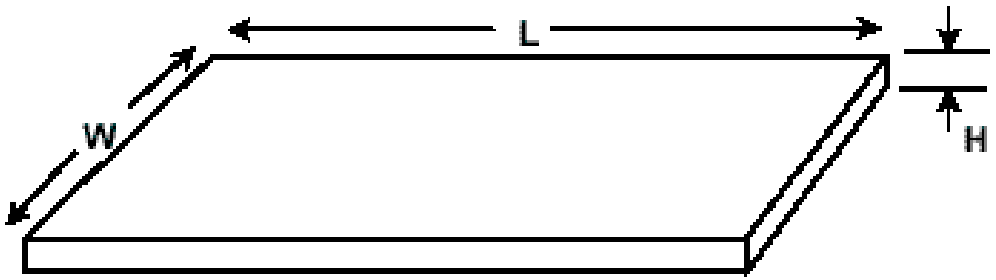
d = 0.073cm

C = 0.072pF

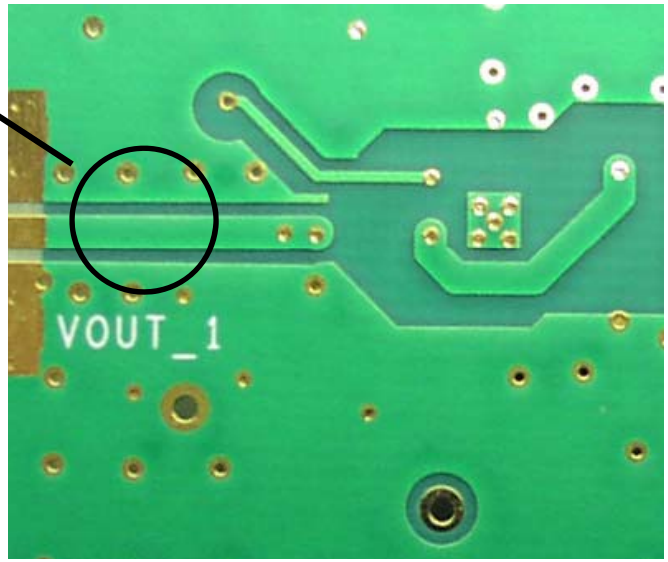
Reduce Capacitance
1) Increase board thickness or layers
2) Reduce trace/pad area
3) Remove ground plane

ANALOG DEVICES

Approximate Trace Inductance



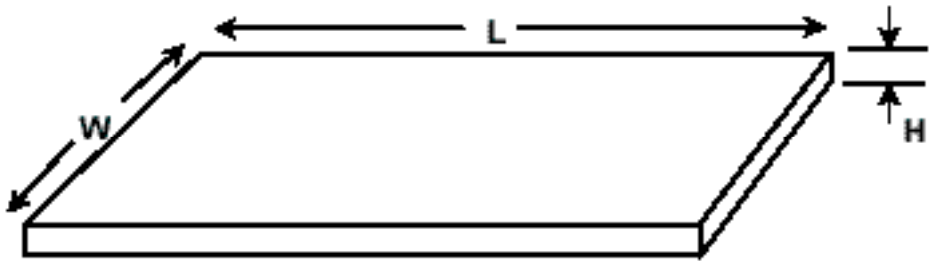
$$\text{STRIP INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H$$



All dimensions are in mm

ANALOG DEVICES

Approximate Trace Inductance



$$\text{STRIP INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H$$

All dimensions are in mm

Example

L= 25.4mm

W = .25mm

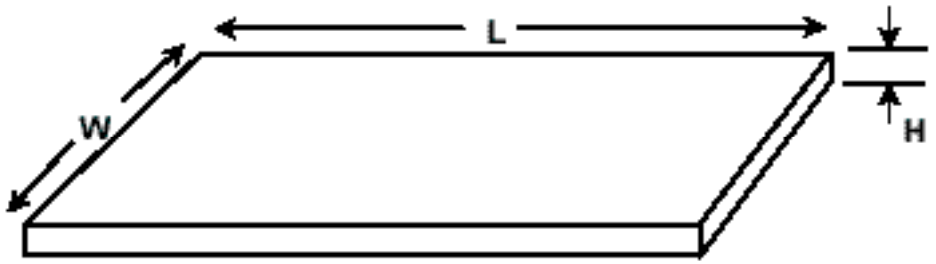
H = .035mm (1oz copper)

Strip Inductance = 28.8nH

At 10MHz Z_L = 1.86 Ω a 3.6% error in a 50Ω system

ANALOG DEVICES

Approximate Trace Inductance



$$\text{STRIP INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H$$

All dimensions are in mm

Example

L= 2.54cm =25.4mm

W = .25mm

H = .035mm (1oz copper)

Strip Inductance = 28.8nH

At 10MHz Z_L = 1.86 Ω a 3.6% error in a 50Ω system

Minimize Inductance

1) Use Ground plane
2) Keep length short (halving the length reduces inductance by 44%)
3) Doubling width only reduces inductance by 11%

ANALOG DEVICES

Via Parasitics

Via Inductance

$$L \approx 2h\left[\ln\left(\frac{4h}{d}\right)+1\right] nH$$

L = inductance of the via, nH

H = length of via, cm

D = diameter of via, cm

Given:

H= 0.157 cm thick board,

D= 0.041 cm

L ~ 1.2nh

Via Capacitance

$$C \approx \frac{0.55\varepsilon_r T D_1}{D_2 - D_1} \; pF$$

D_2 = diameter of clearance hole in the ground plane, cm

D_1 = diameter of pad surrounding via, cm

T = thickness of printed circuit board, cm

ε_r = relative electric permeability of circuit board material

C = parasitic via capacitance, pF

Given:

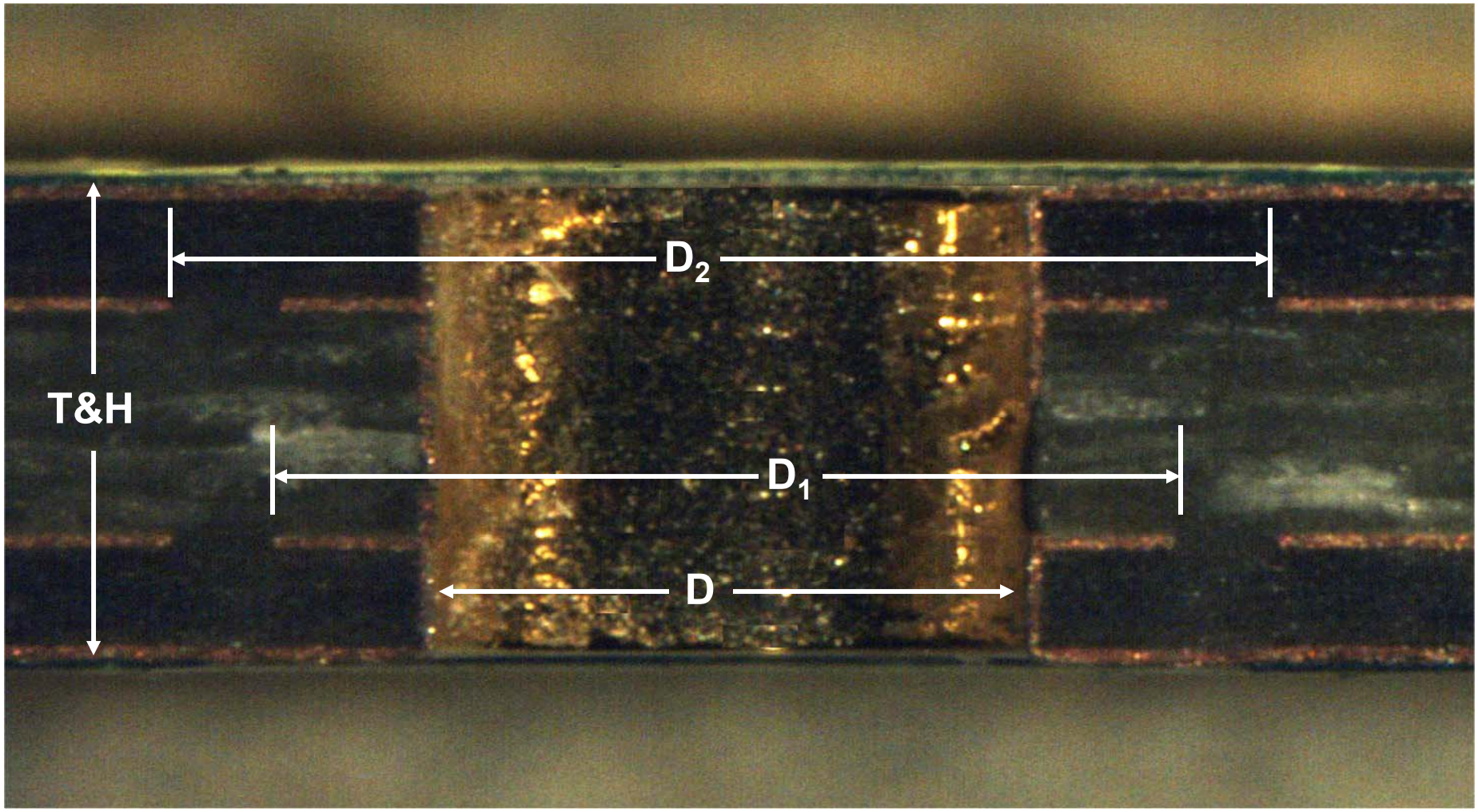
T = 0.157cm,

D_1=0.071cm

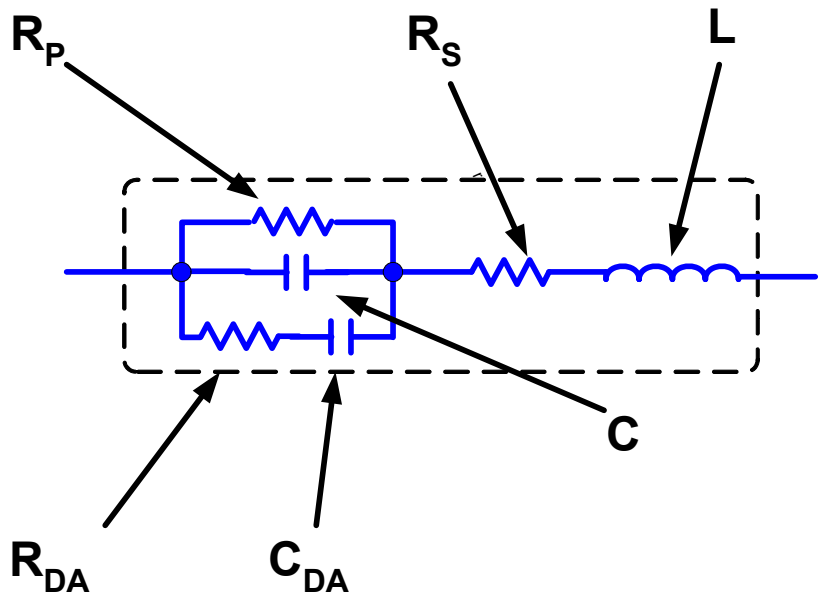
D_2 = 0.127

C ~ 0.51pf

Via Cross Section

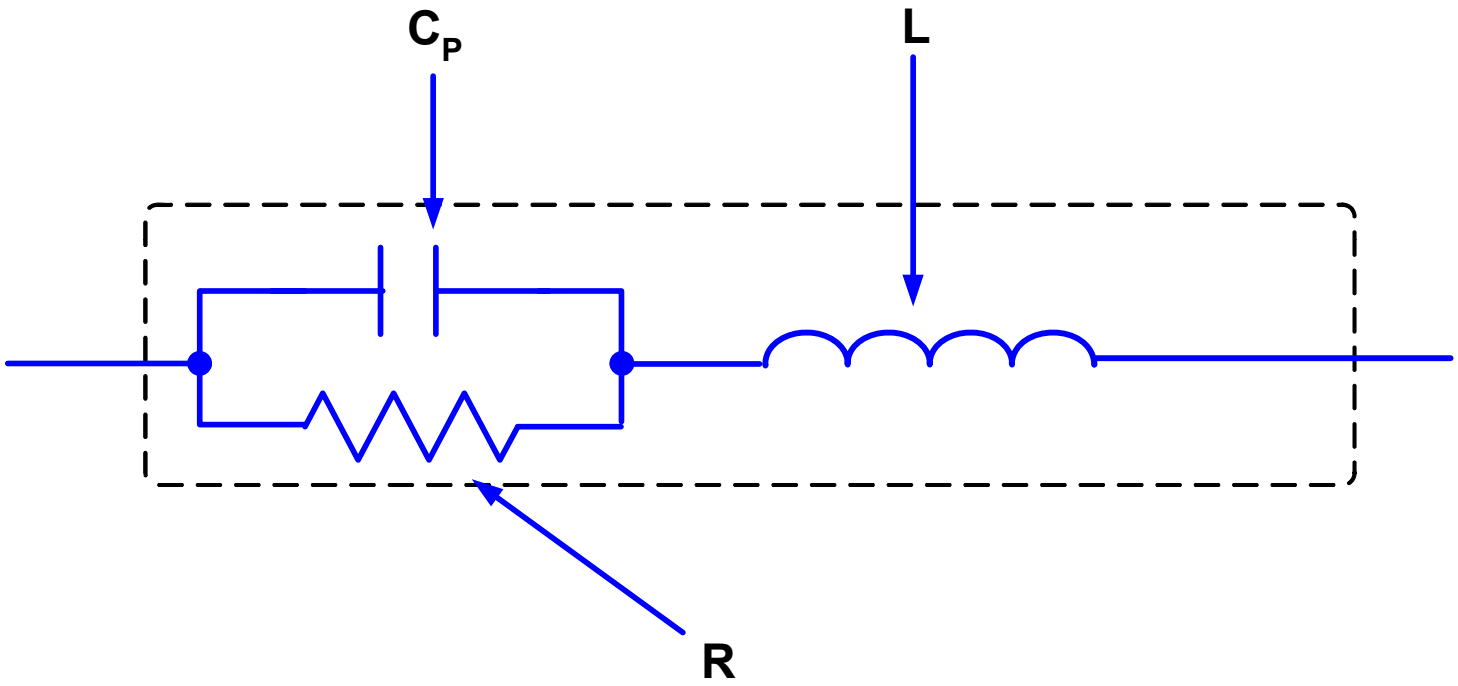


Capacitor Parasitic Model



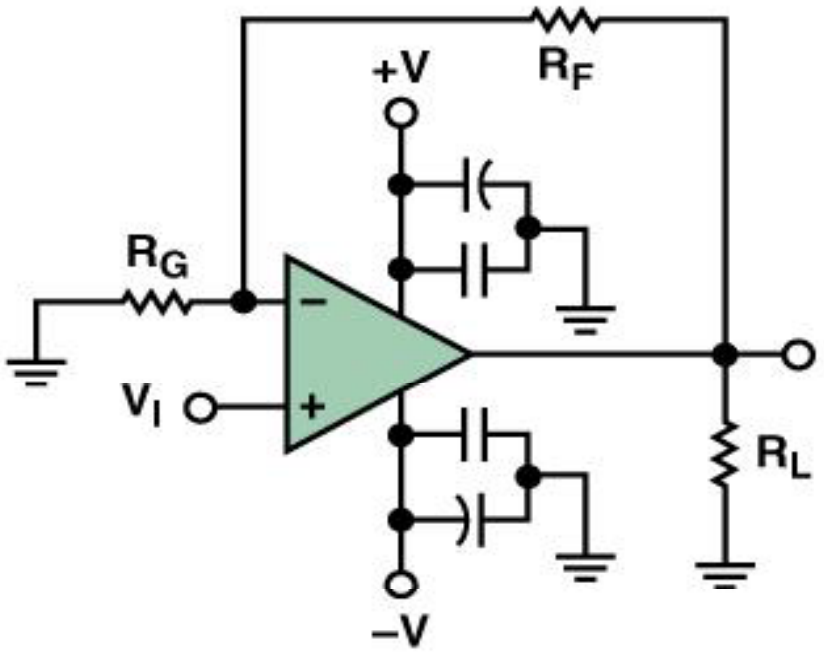
C = Capacitor
R_P = insulation resistance
R_S = equivalent series resistance (ESR)
L = series inductance of the leads and plates
R_{DA} = dielectric absorption
C_{DA} = dielectric absorption

Resistor Parasitic Model



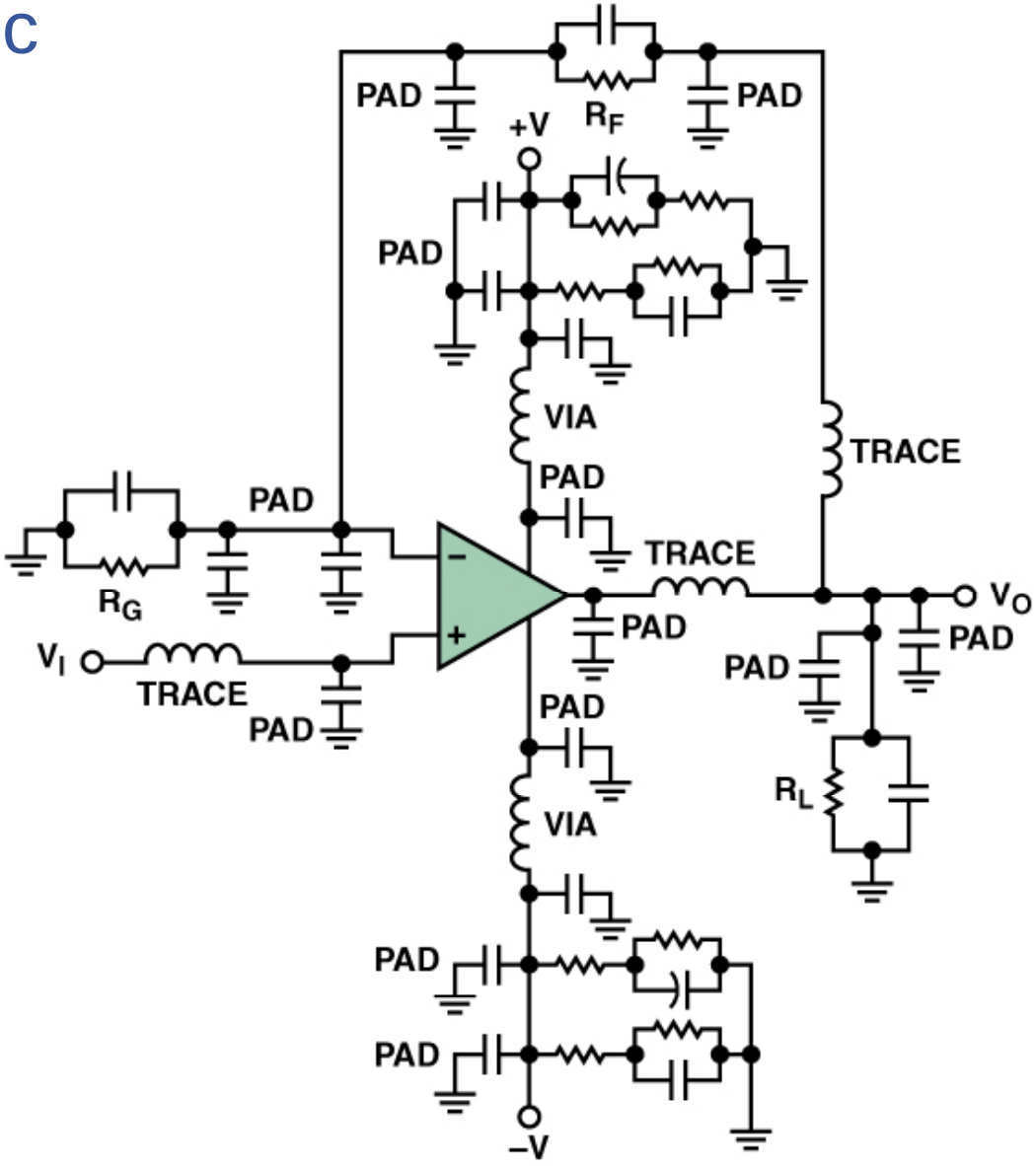
R = Resistor
C_P = Parallel capacitance
L= equivalent series inductance (ESL)

Low Frequency Op Amp Schematic



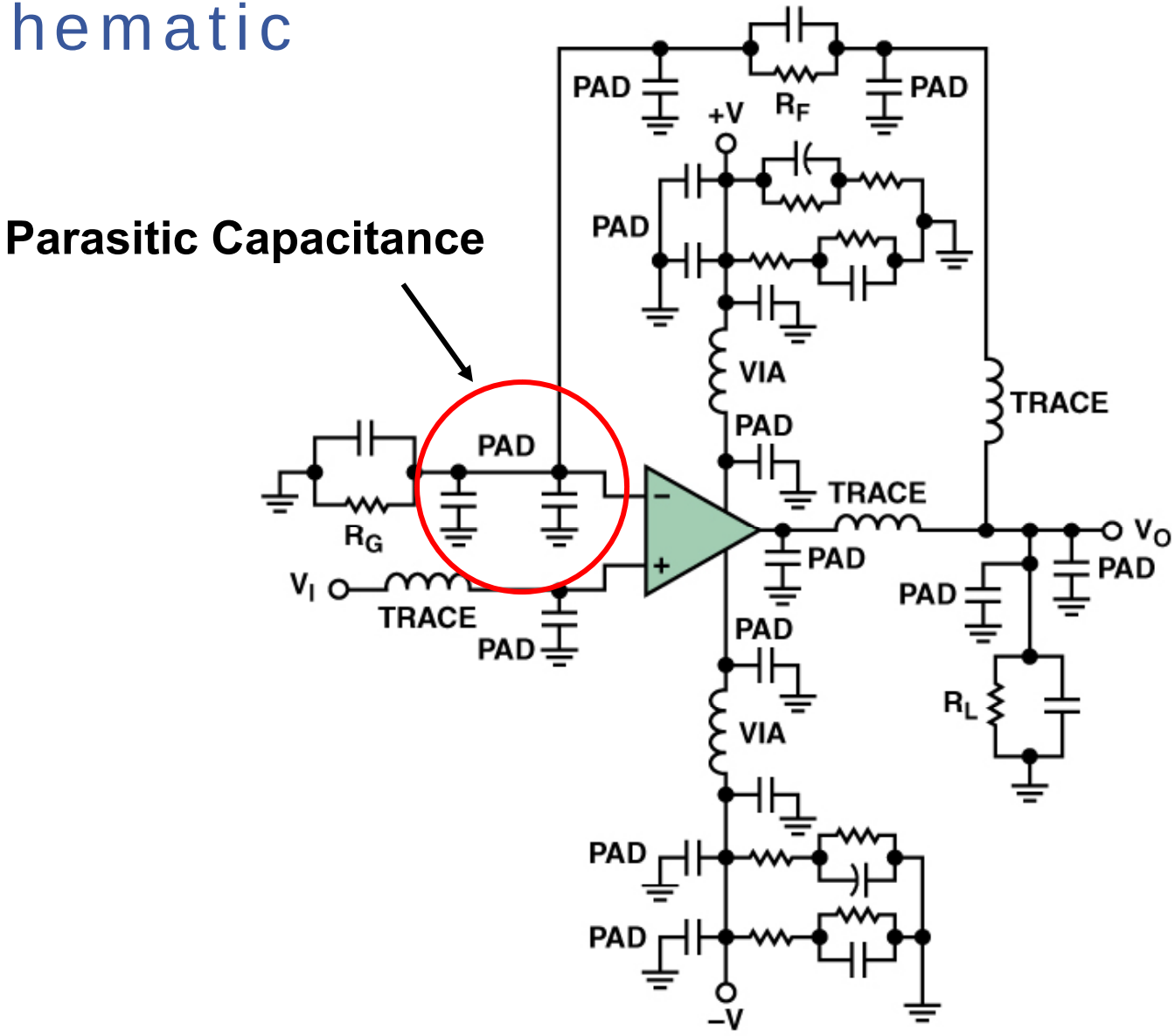
ANALOG DEVICES

High Speed Op Amp Schematic



ANALOG DEVICES

High Speed Op Amp Schematic



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- Instantly access product pages and datasheets of each Analog Devices component
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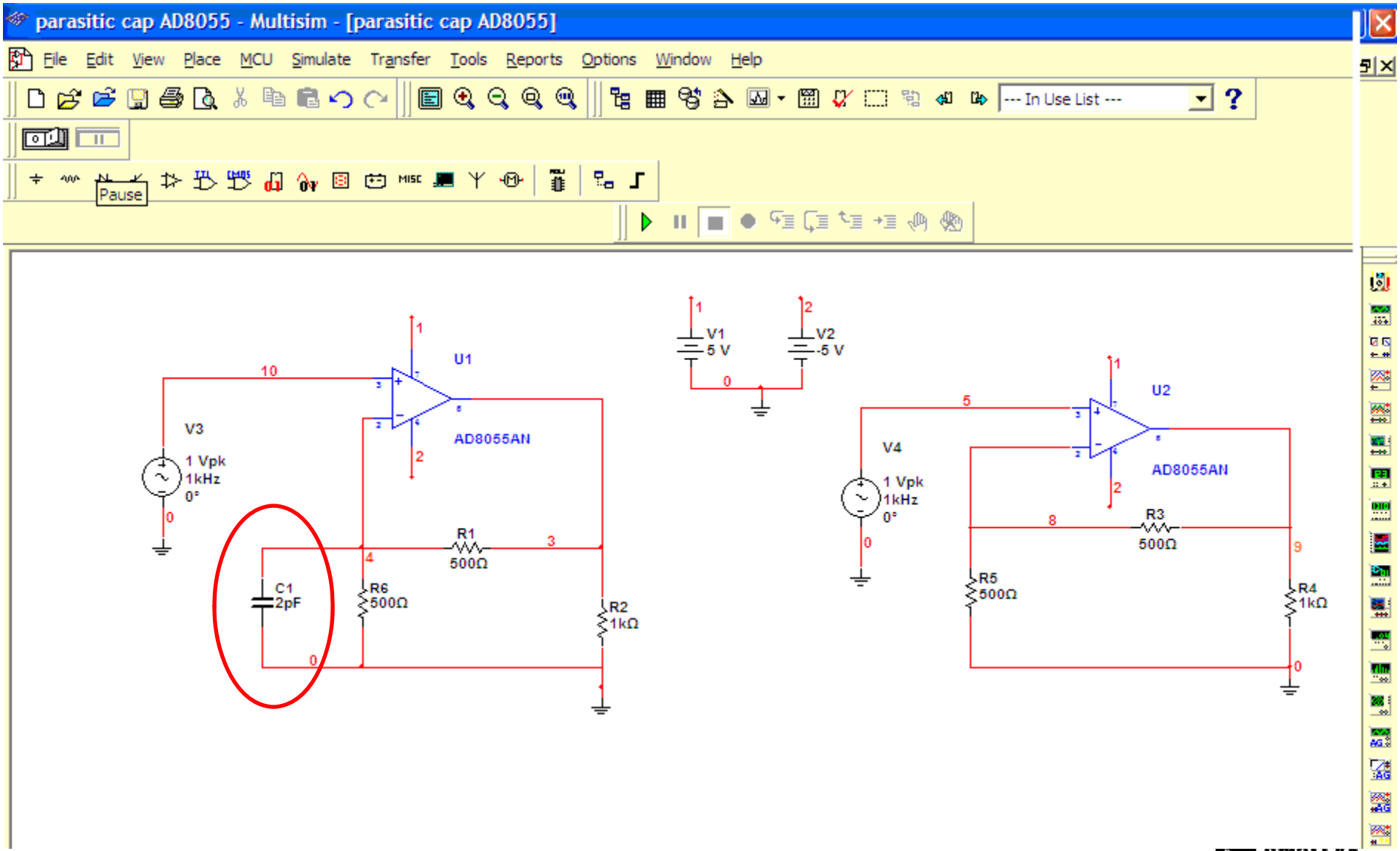
Other Resources:

- Application Circuits: Ready-built reference designs (.zip, 2,913,219 bytes)
- Upgrade to the NI Multisim Professional Edition
- Multisim Technical Support

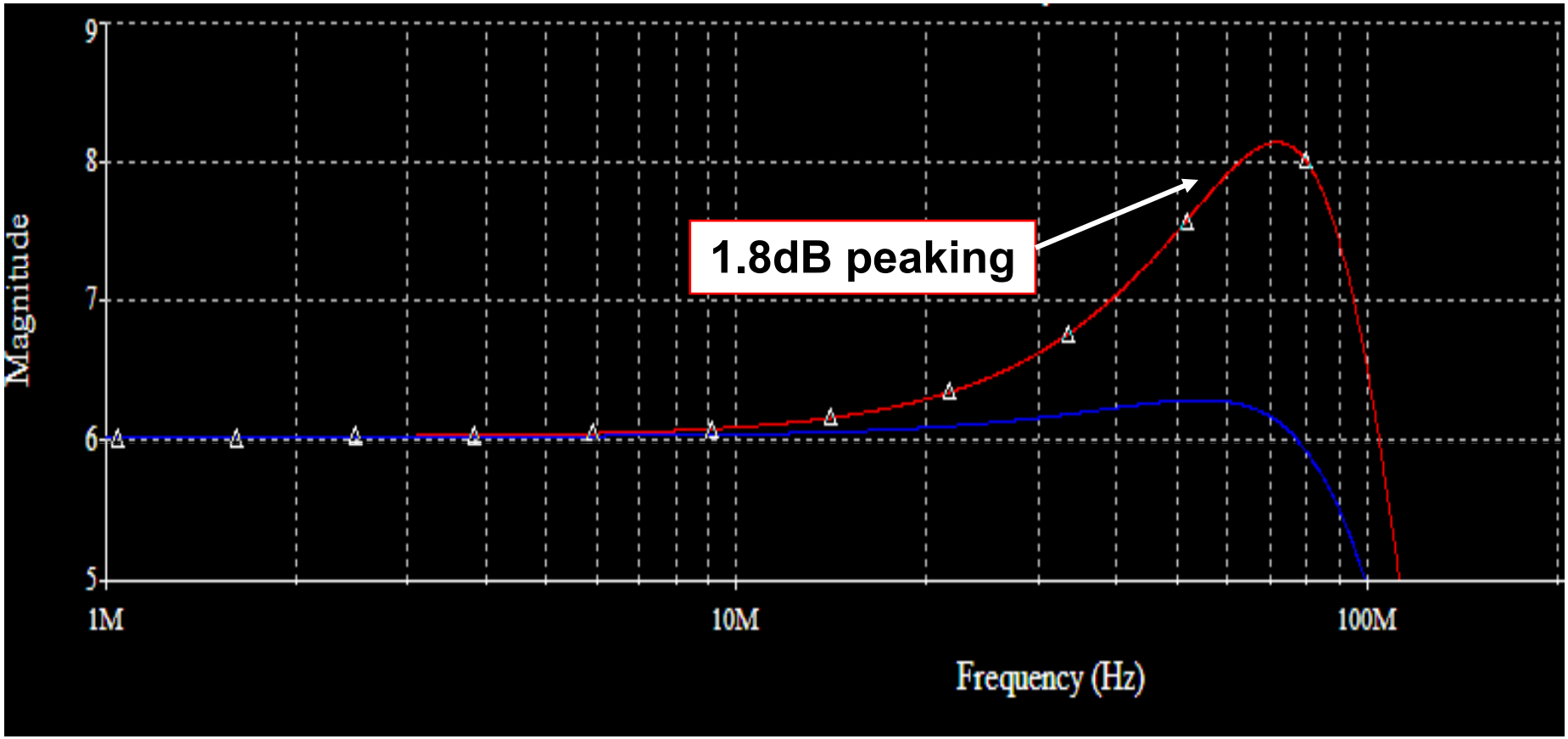
http://www.analog.com/en/design-tools/dt-multisim-spice-program-download/design-center/index.html

ANALOG DEVICES

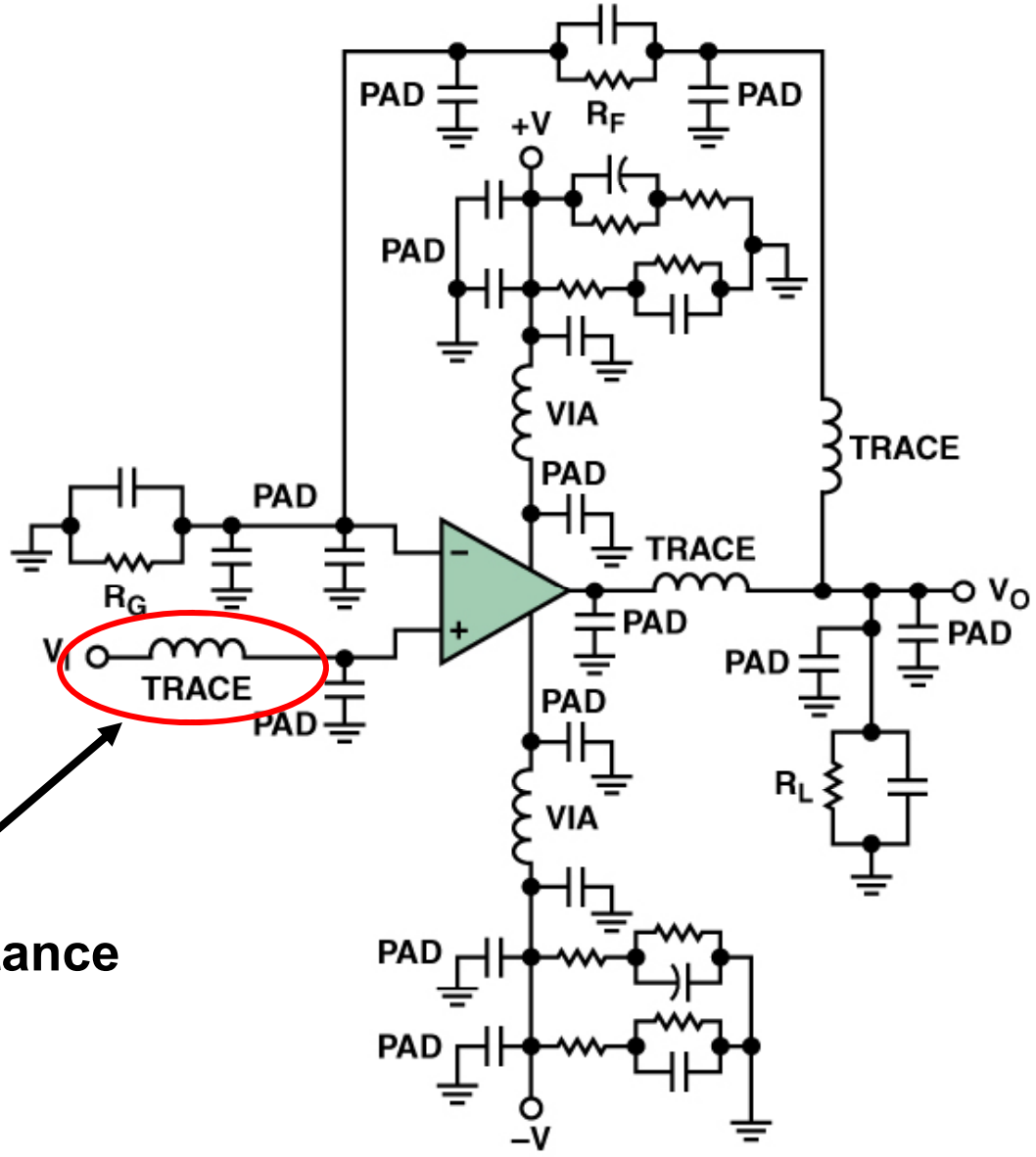
Stray Capacitance Simulation Schematic



Frequency Response with 2pF Stray Capacitance



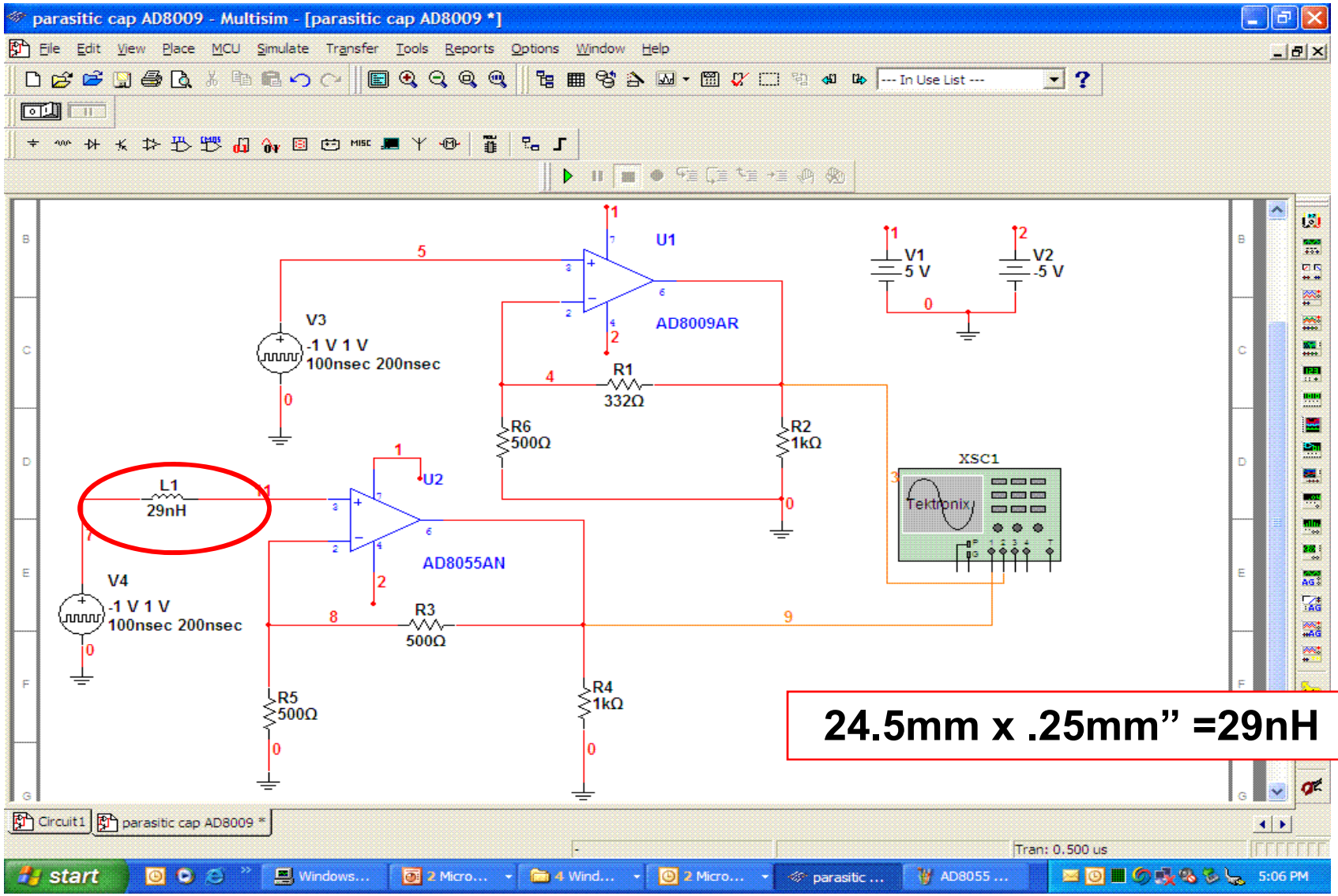
Stray Inductance



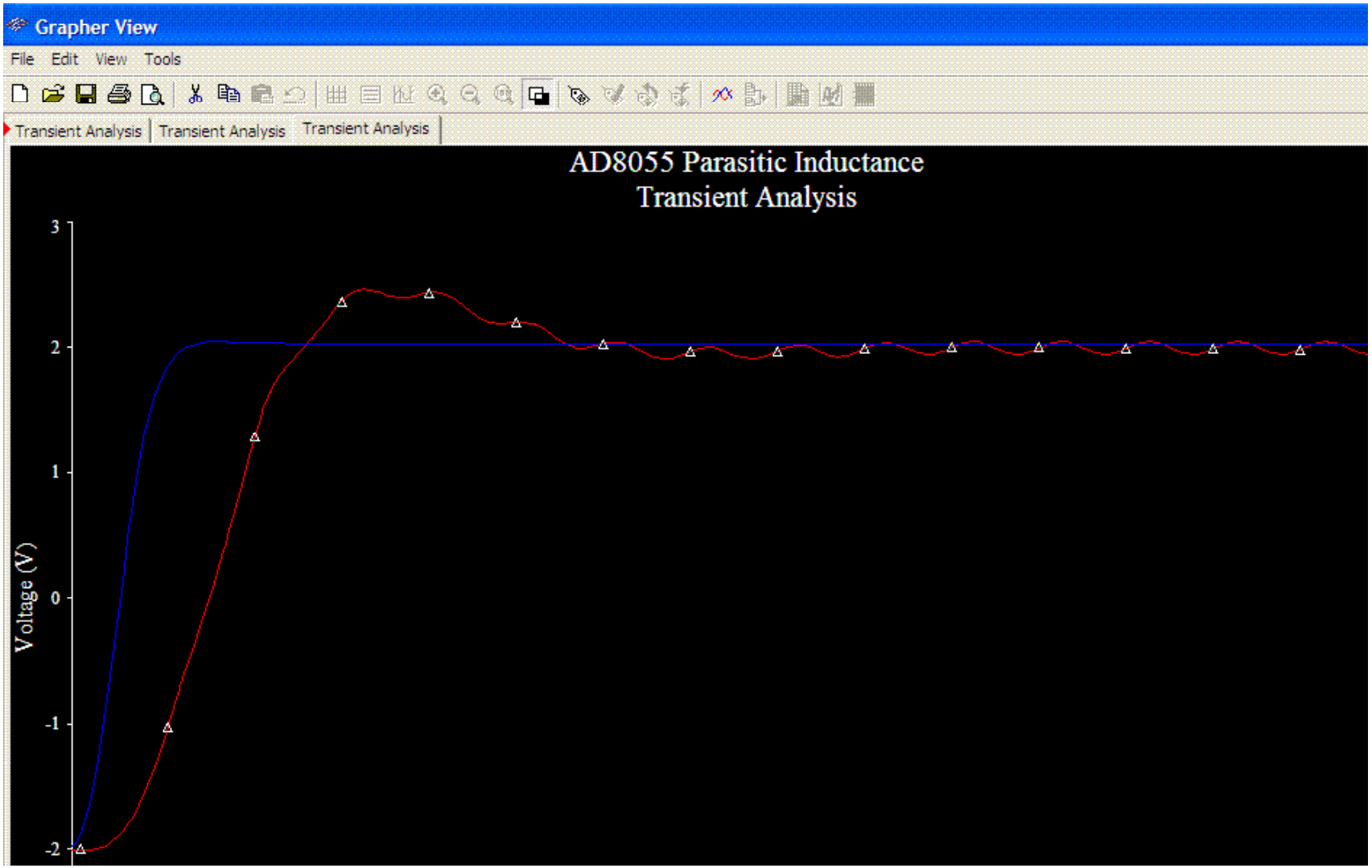
Parasitic Inductance

ANALOG DEVICES

Parasitic Inductance Simulation Schematic

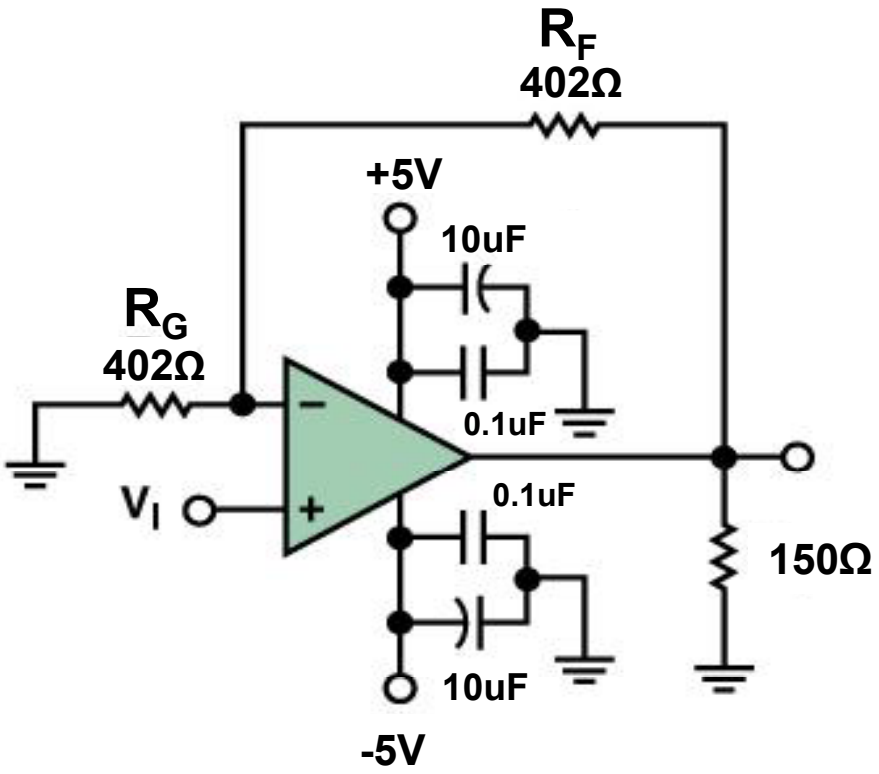


Pulse Response With and Without Ground Plane



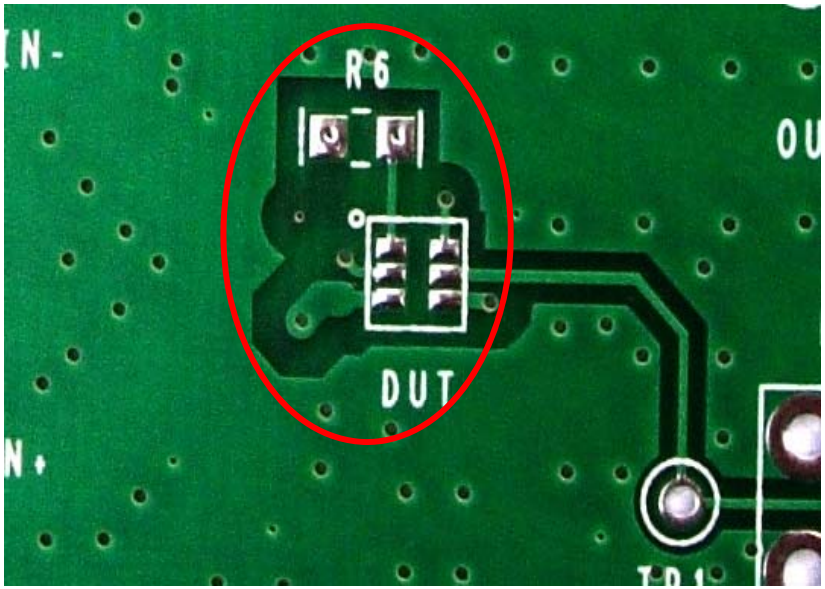
ANALOG DEVICES

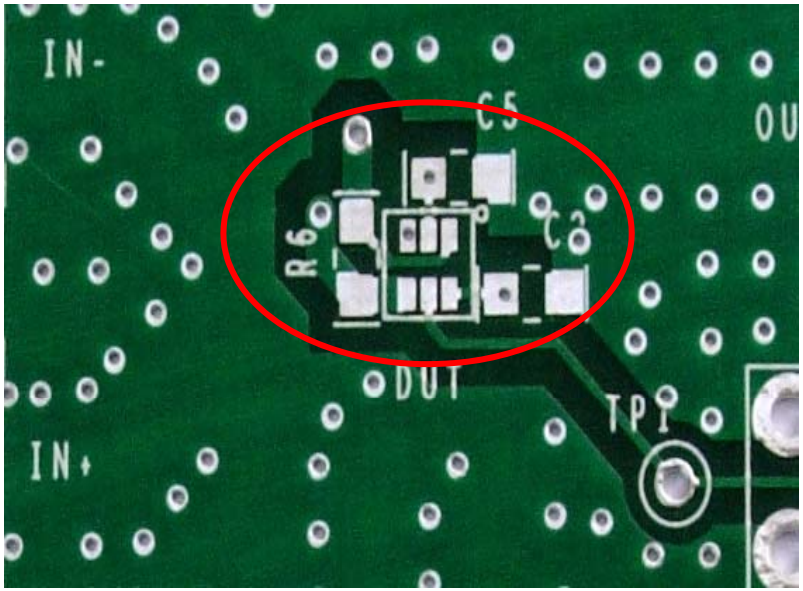
Transient Response AD8009 1GHz Current Feedback Amplifier



ANALOG DEVICES

Small Changes Can Make a Big Difference!

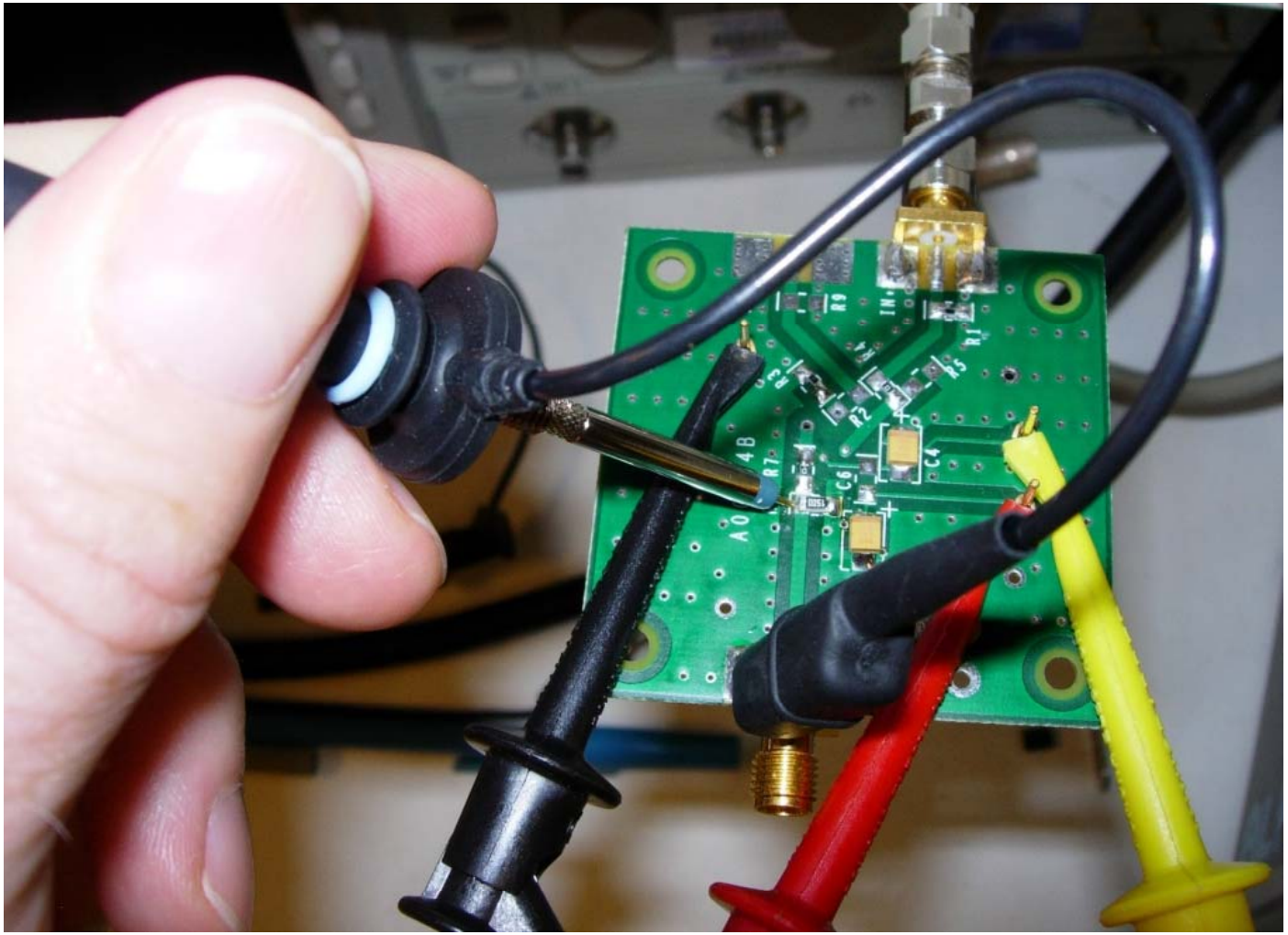




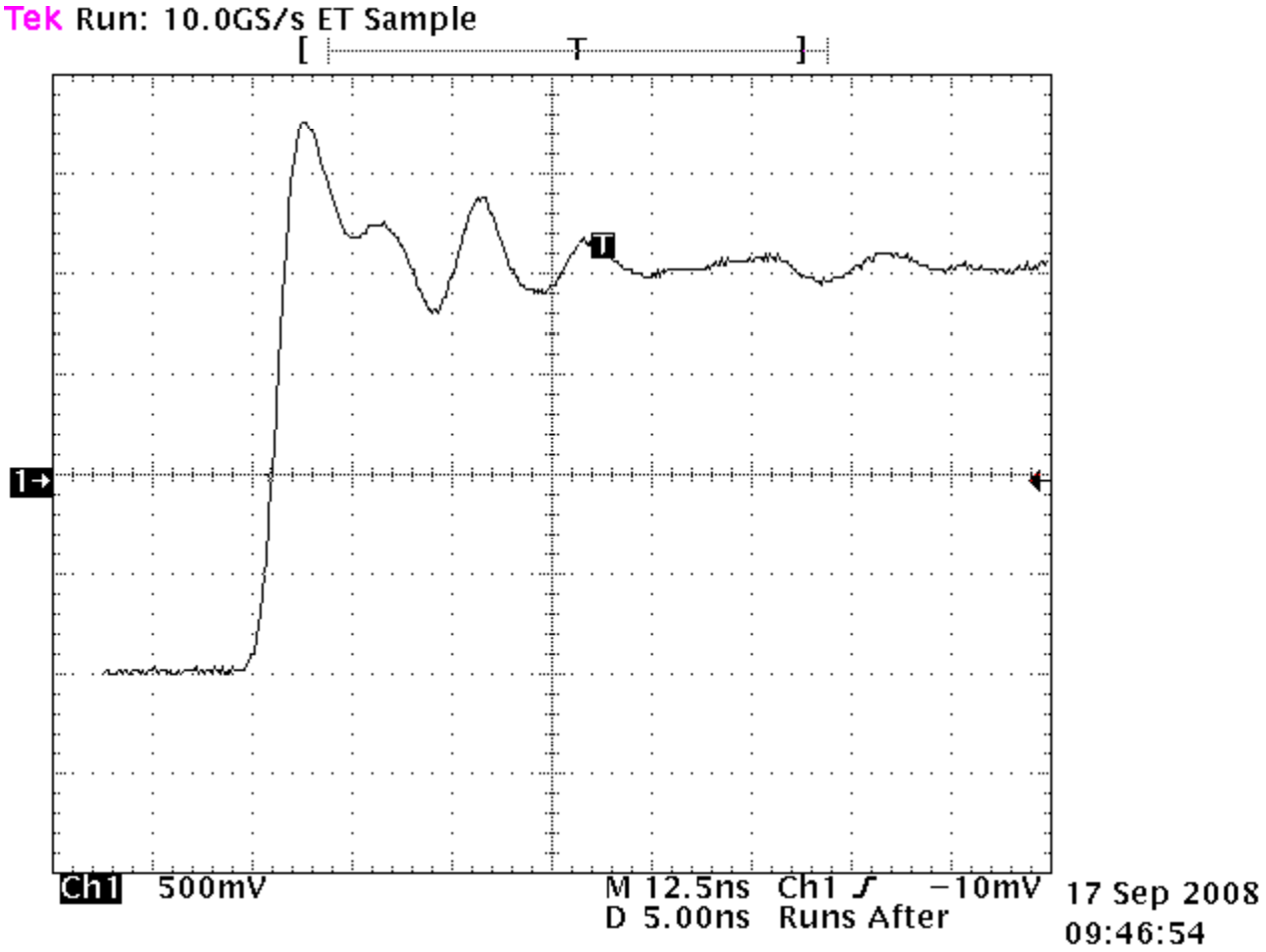
Circuit A

Circuit B

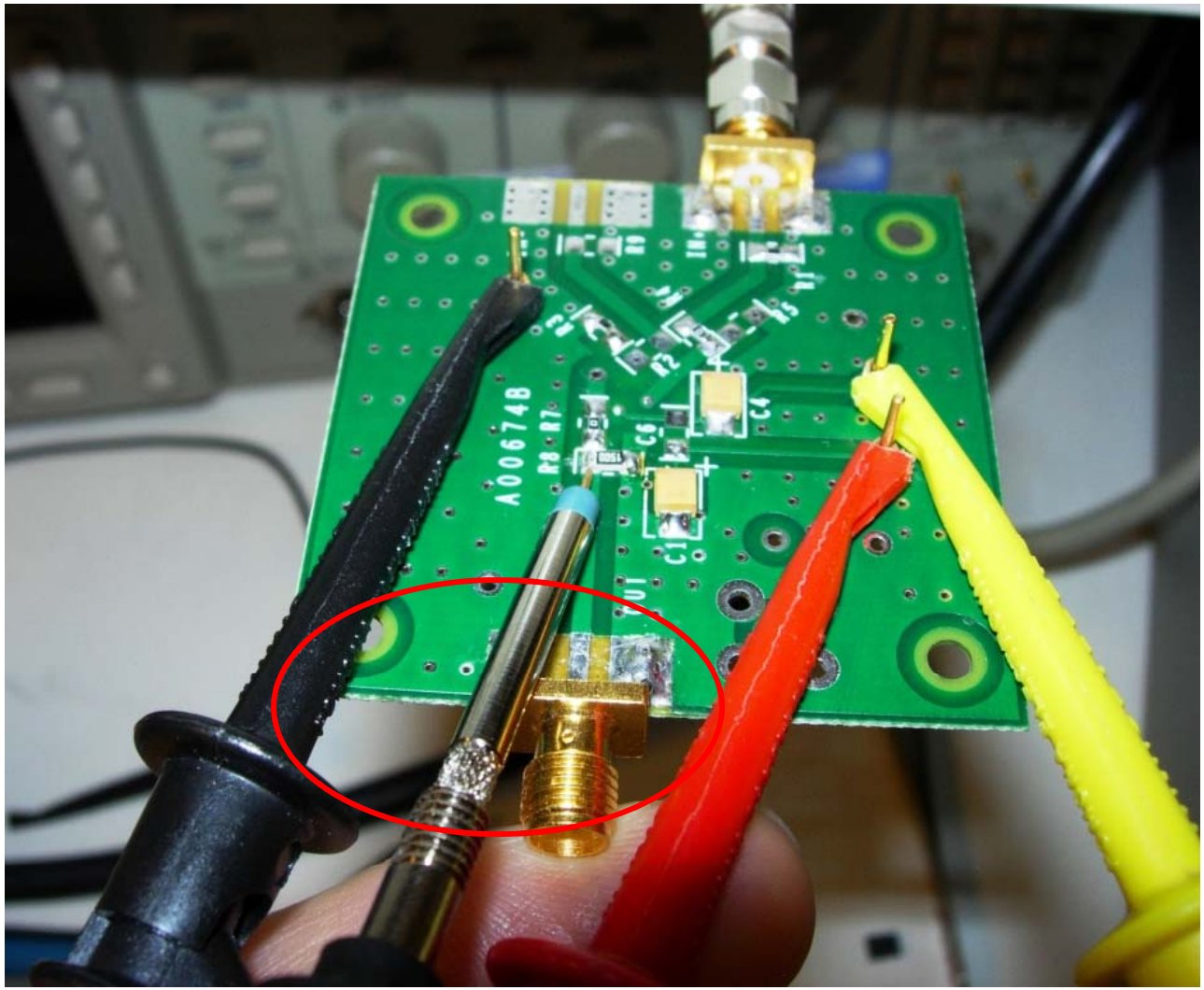
Improper Use of Scope Probe Ground Clip



Effect of Clip Lead Inductance

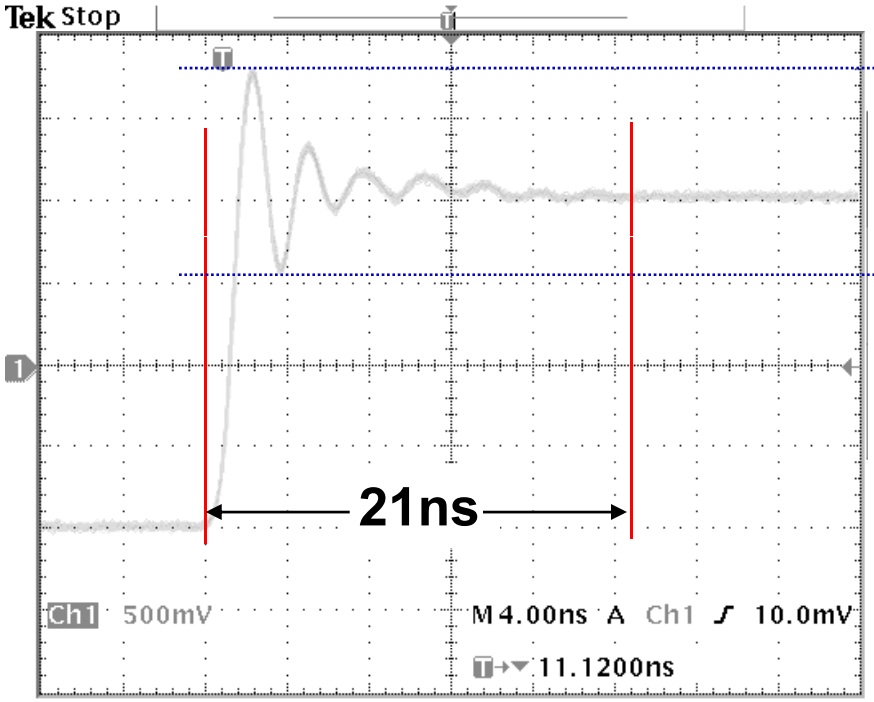


Proper Grounding for Scope Probe in High-Speed Measurments

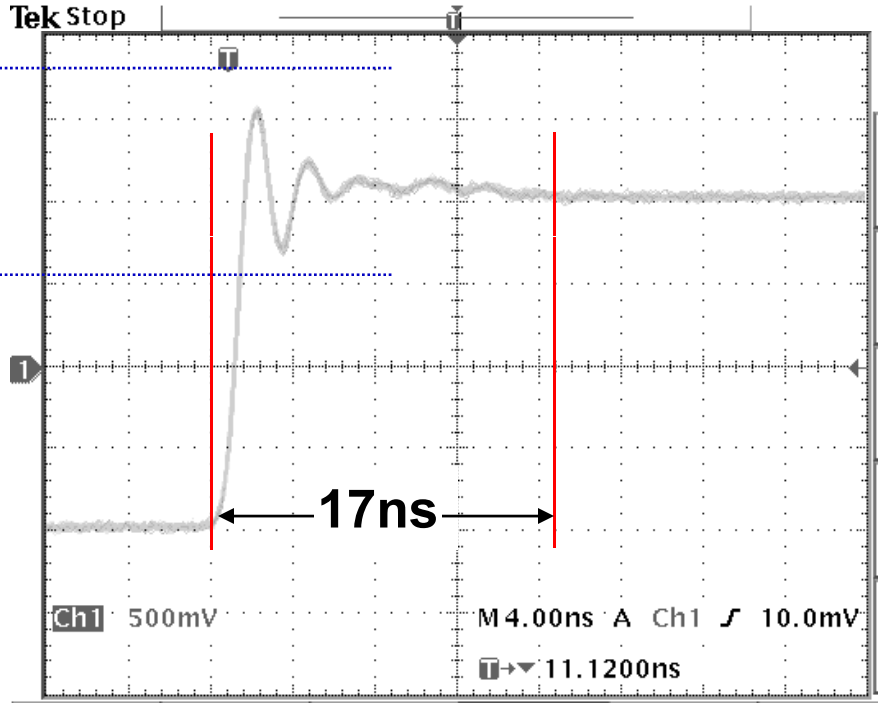


Small Changes Make Big Differences

Circuit A

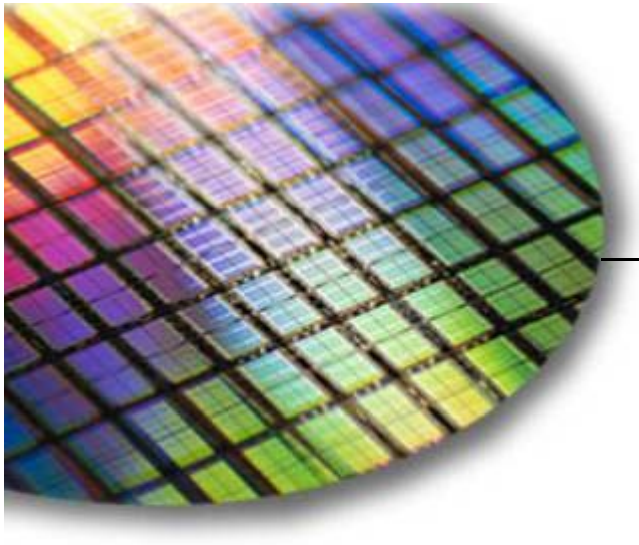


Circuit B



25% reduction in ringing duration and amplitude

ANALOG DEVICES



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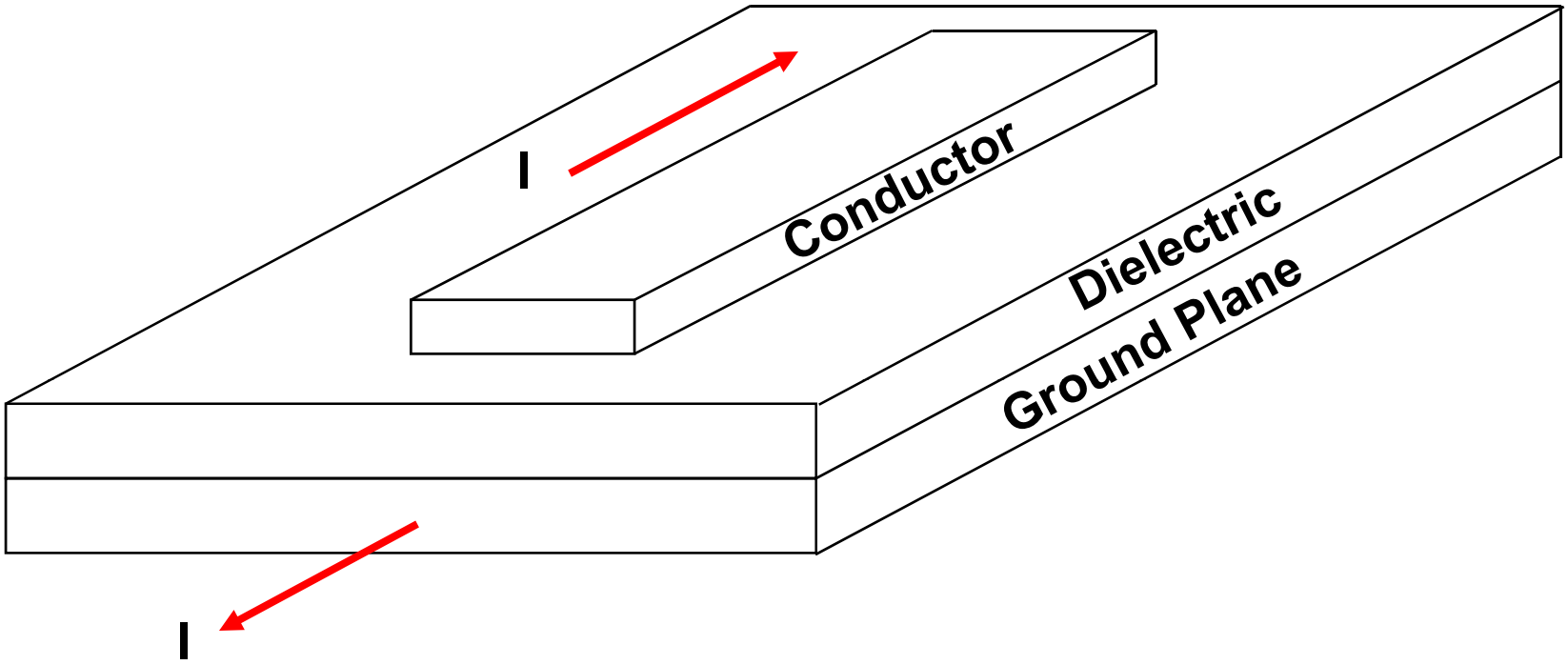
Ground and Power Planes

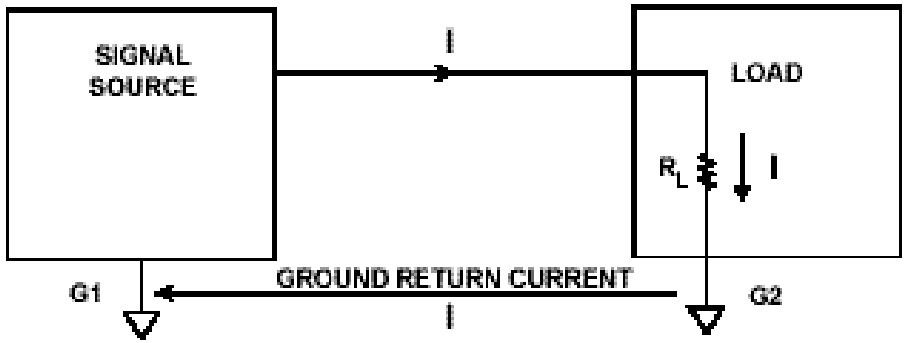
ANALOG DEVICES

Ground and Power Planes Provide

- A common reference point
- Shielding
- Lower noise
- Lower resistance
- Lower impedance
- Reduces parasitics
- Heat sink
- Power distribution

Ground Plane

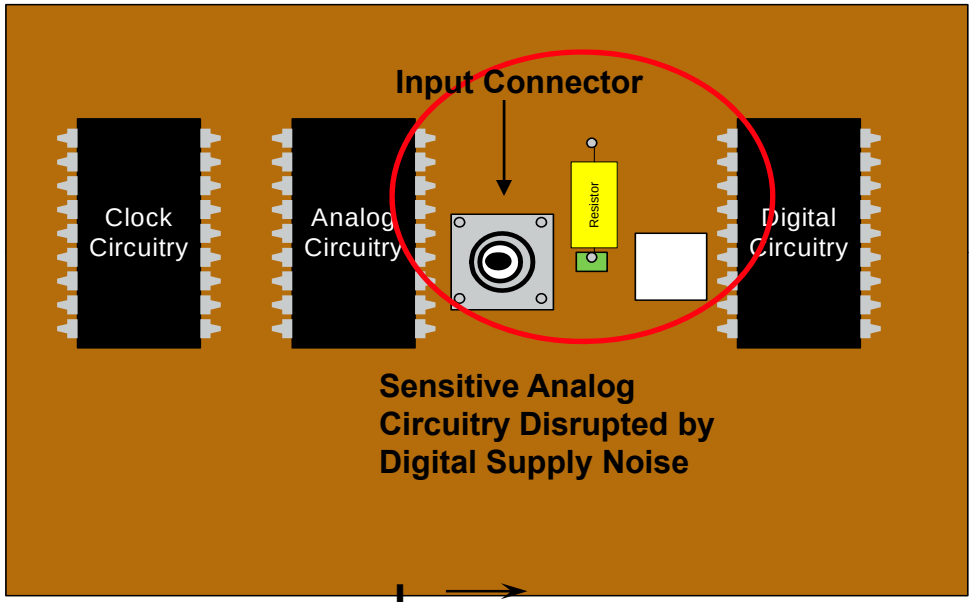


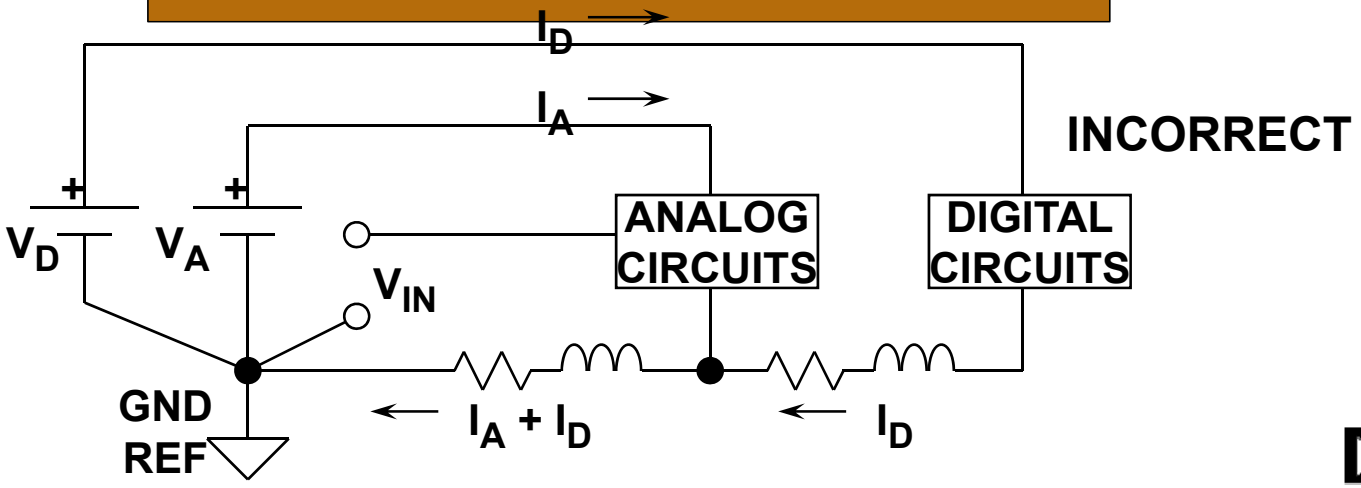


ANALOG DEVICES

Ground Plane and Trace Routing

Wrong Way





ANALOG DEVICES

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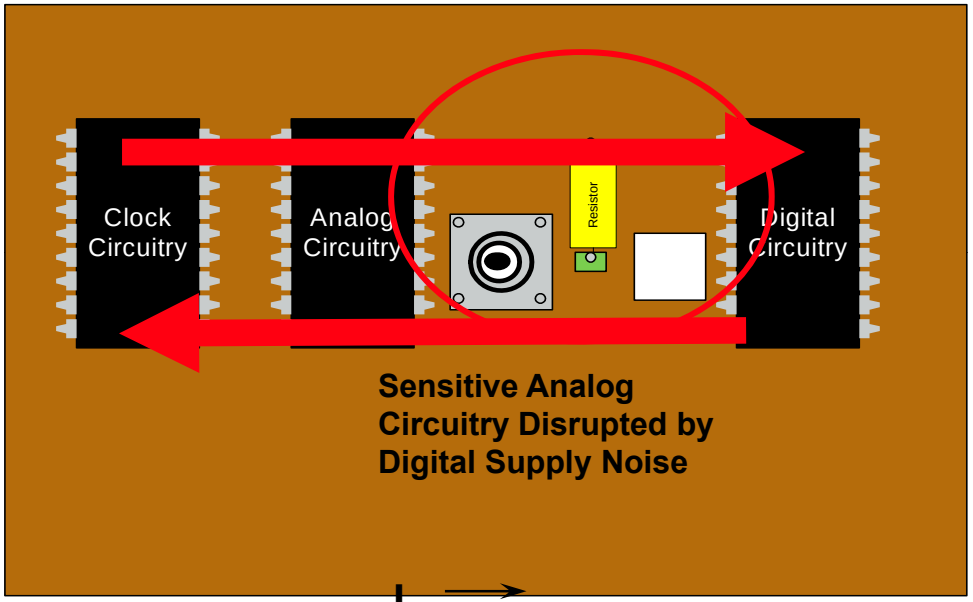
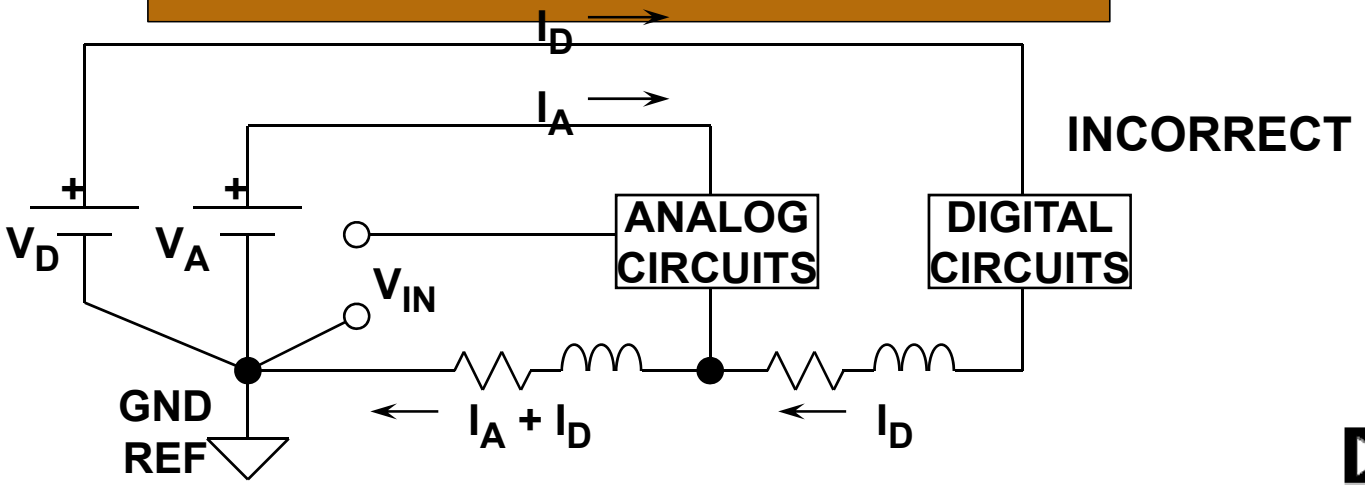
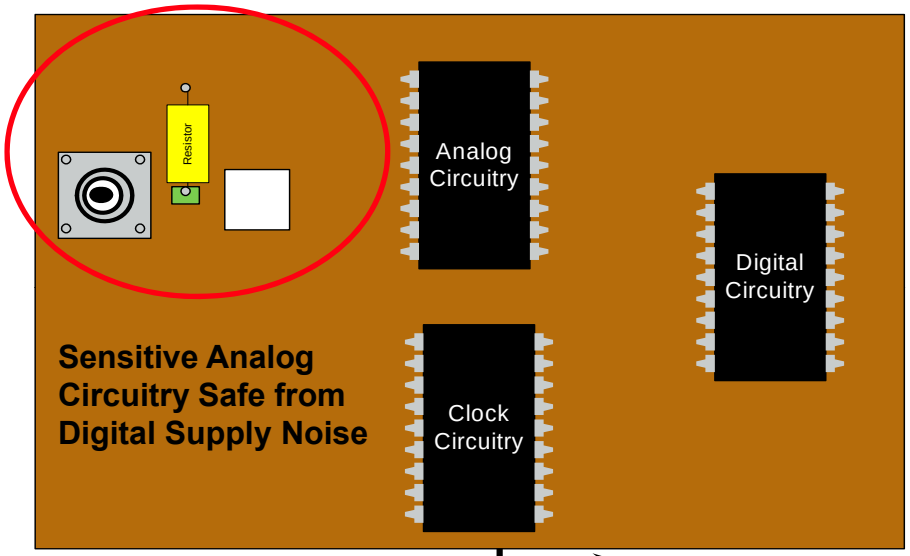


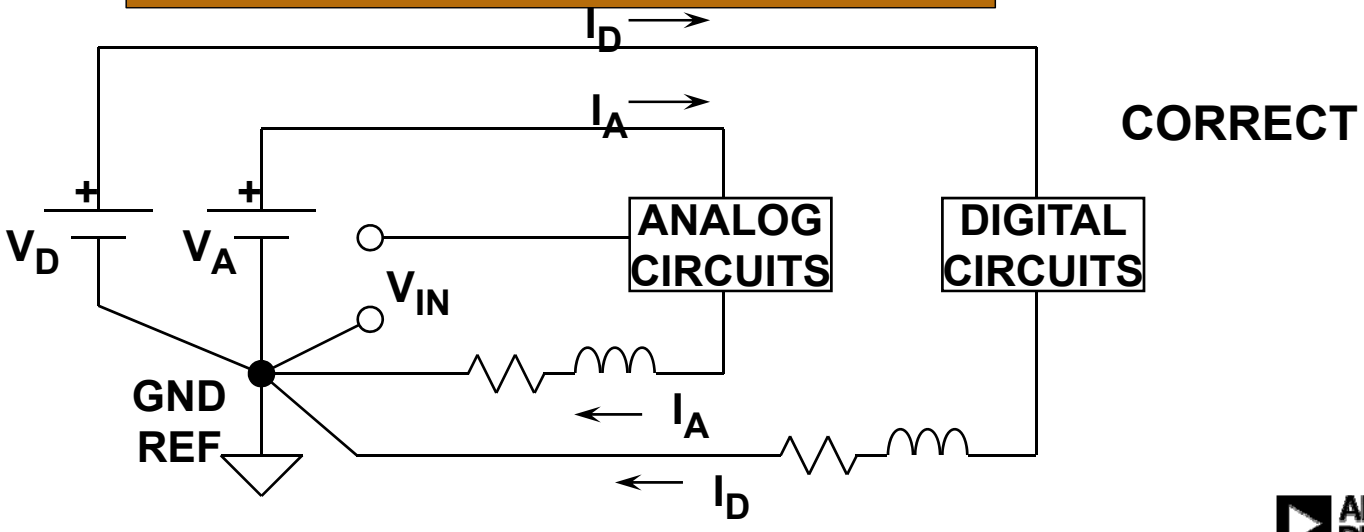


ANALOG DEVICES

Ground Plane and Trace Routing

Right Way



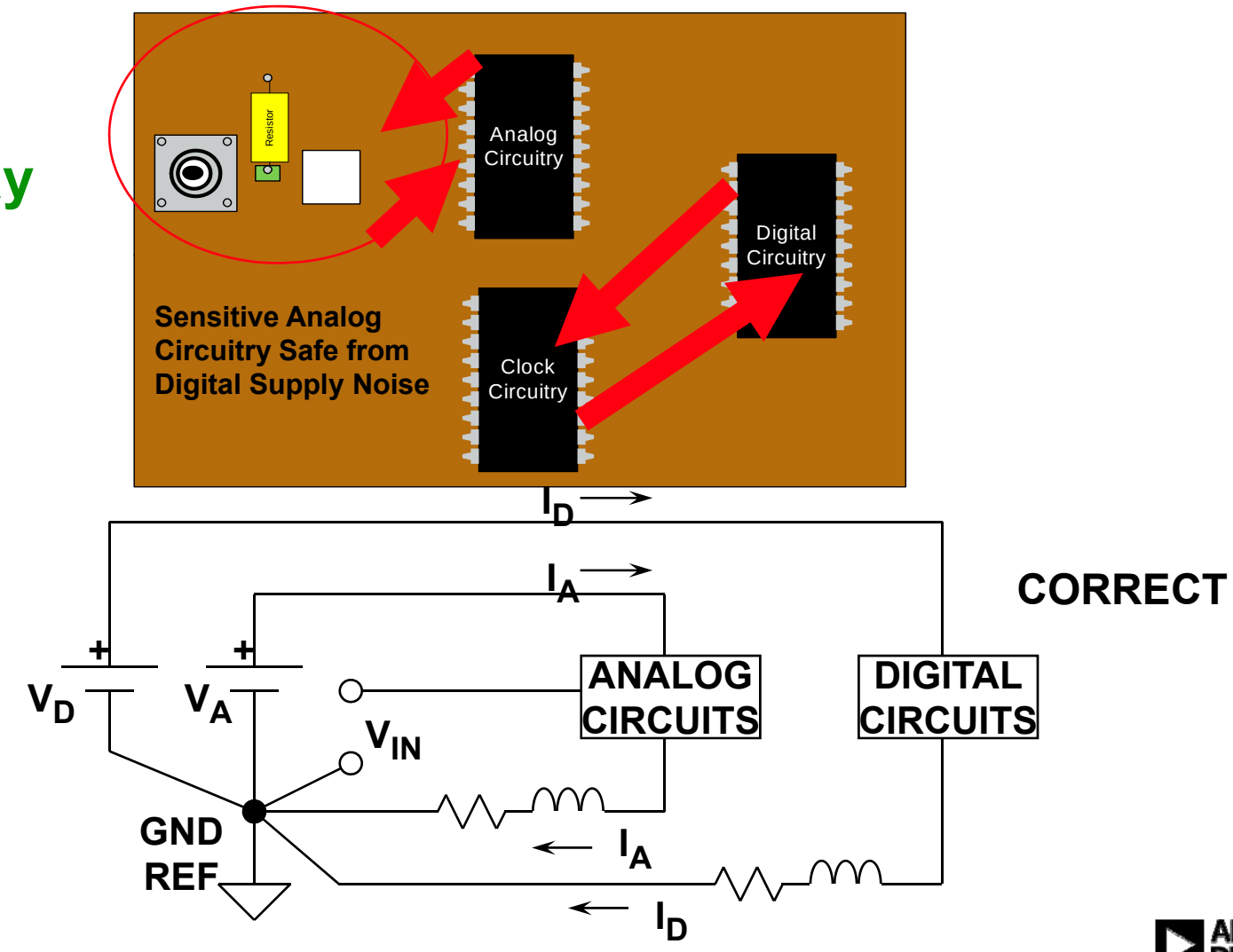


CORRECT

ANALOG DEVICES

Ground Plane and Trace Routing

Right Way

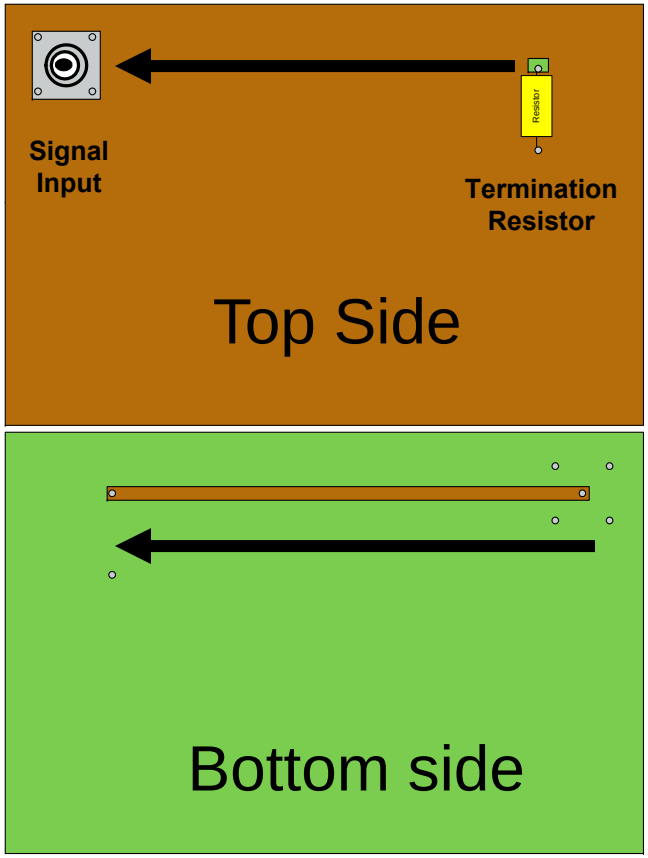


ANALOG DEVICES

Ground Plane and Trace Routing

Grounding Example:

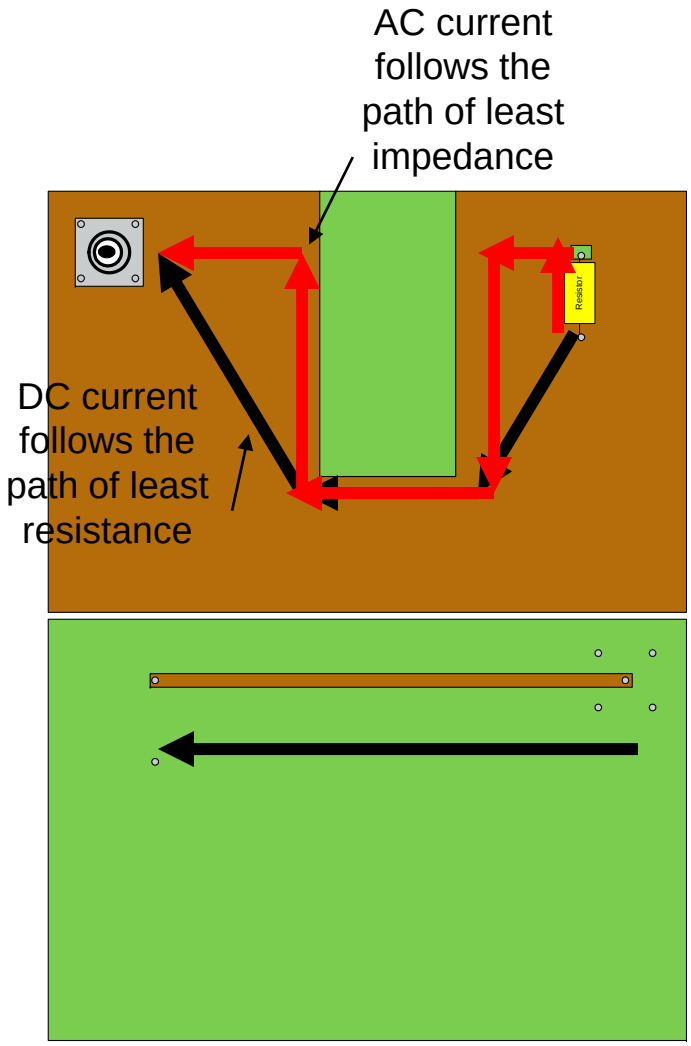
- **Top layer is solid ground.**
- **Bottom has a trace/transmission line connecting the RF connector to the load.**
- **Return current flows in the top layer ground plane directly above the trace on the opposite side.**



Ground Plane and Trace Routing

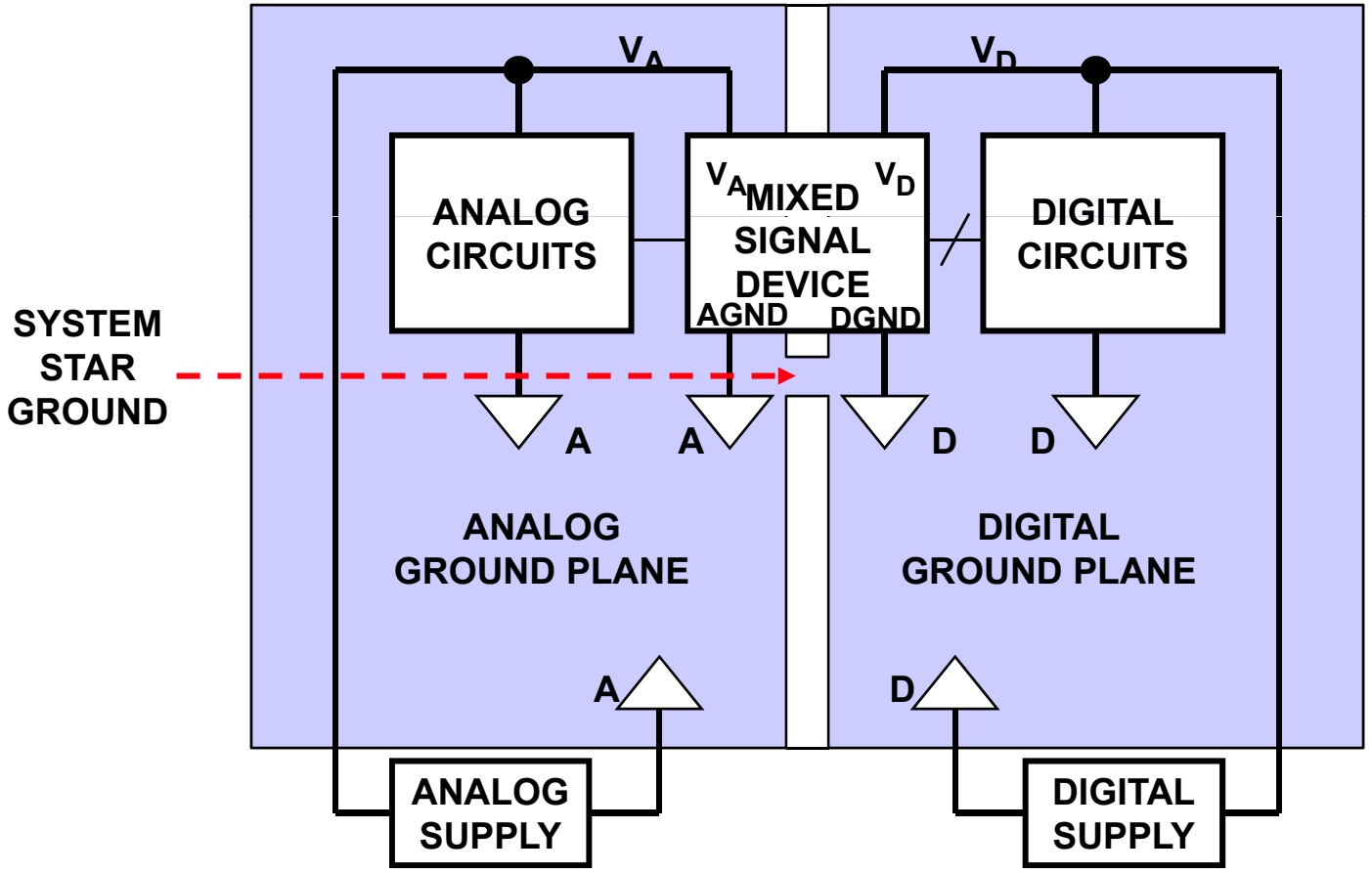
Grounding Example: DC Current vs. AC Current:

- **In a split or broken ground, the return currents follow the path of least impedance**
- **At DC, the current follows the path of least resistance**
- **As the frequency increases, the current follows the path of least inductance**
- **Since there is now a 'loop' the inductance can be quite high and the circuit can now propagate EMI/RFI**



ANALOG DEVICES

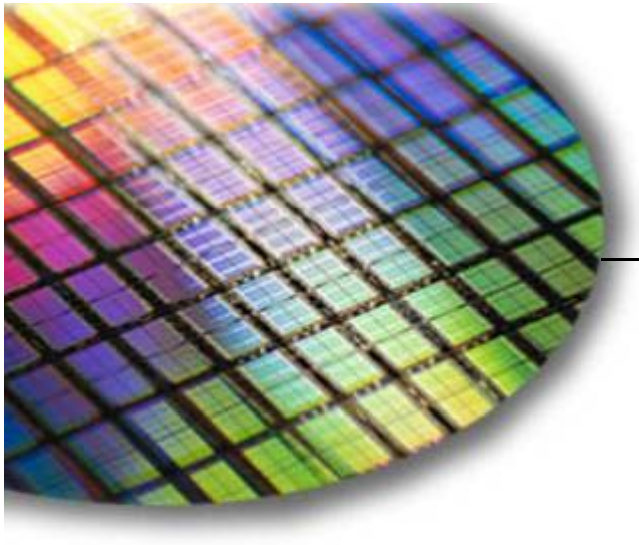
Grounding Mixed Signal ICs: Single PC Board



ANALOG DEVICES

Ground Plane Recommendations

- There is no single grounding method which is guaranteed to work 100% of the time!
- Remove ground plane under op amps to reduce parasitic capacitance
- At least one layer on each PC board MUST be dedicated to ground plane!
- Provide as much ground plane as possible especially under traces that operate at high frequency
- Use thickest metal as feasible (reduces resistance and provides improved thermal transfer)
- Use multiple vias to connect same ground planes together
- Do initial layout with split analog and digital ground planes
- Follow recommendations on device data sheet (read datasheet)
- Keep bypass capacitors and load returns close to reduce distortion
- Connect analog, digital and RF grounds at one point



The World Leader in High Performance Signal Processing Solutions

Packaging and Pinout

ANALOG DEVICES

Op Amp Packaging and Pinout

- **Packaging plays a large role in high-speed applications**

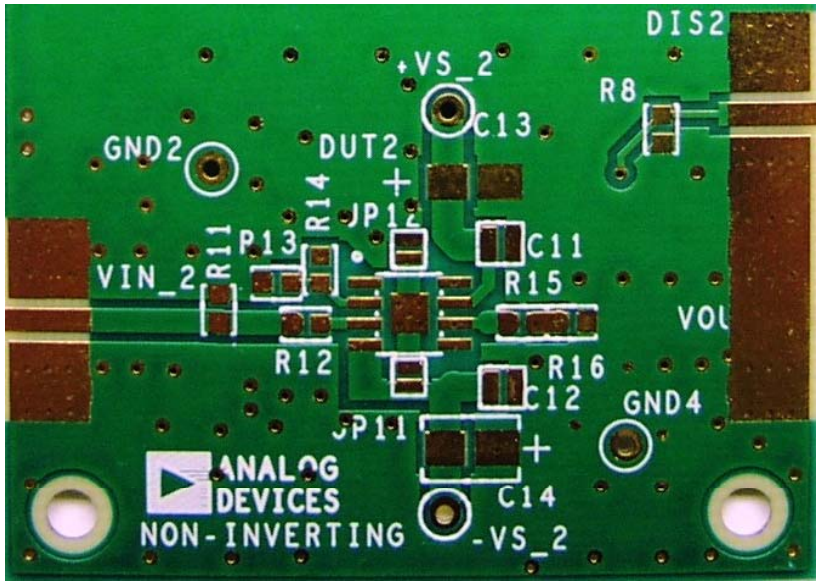
Smaller packages

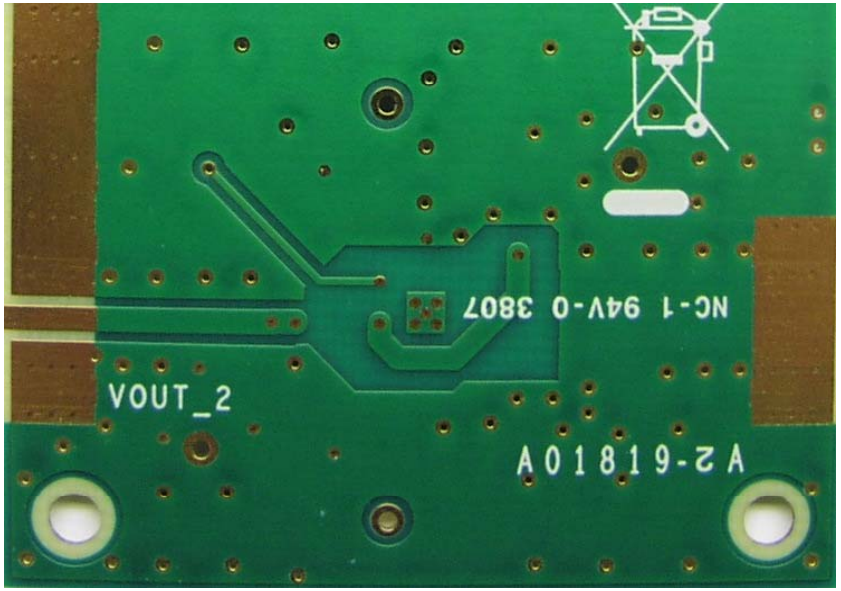
- **Better at higher speeds**
- **Less parasitics**
- **Compact layout**

- **Analog Devices Low Distortion Pinout**
  - **Intuitively makes more sense**
  - **Compact layout**
  - **Streamline signal flow**
  - **Lower distortion**

Op Amp SOIC Packaging

- **Traditional SOIC-8 layout**
- **Feedback routed around or underneath amplifier**





Op Amp SOIC Packaging

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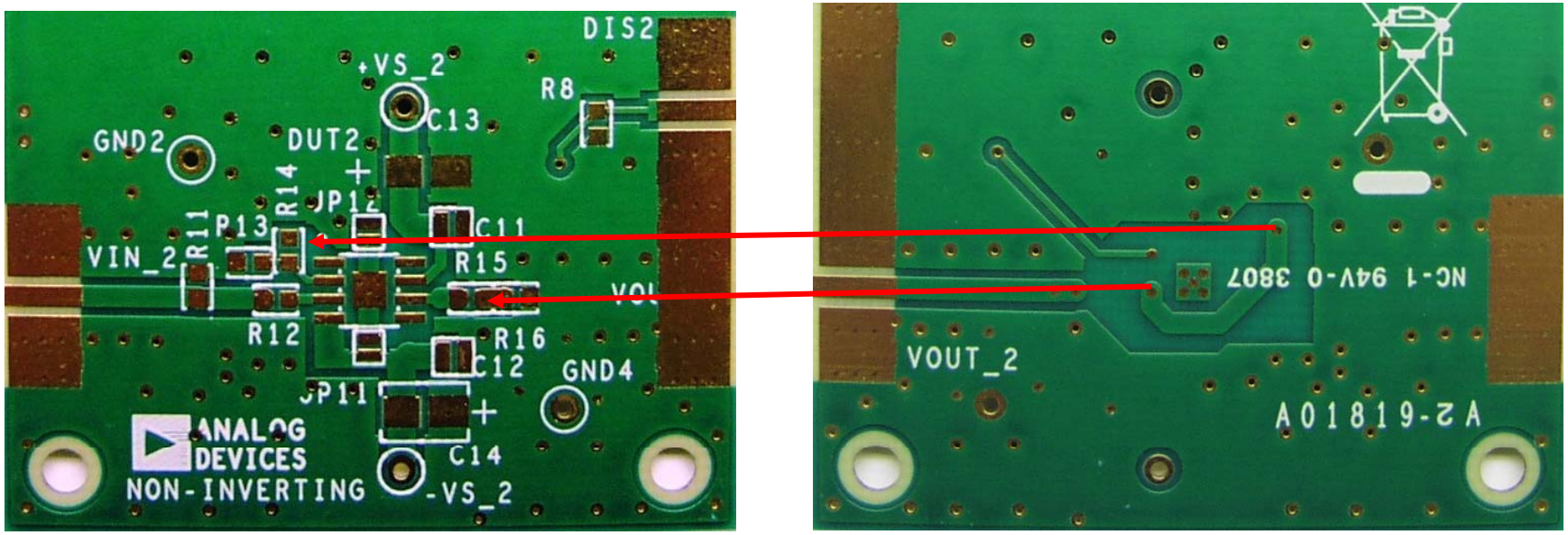
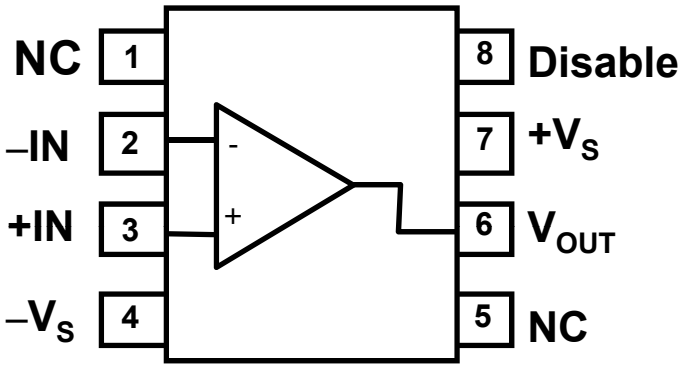


ANALOG DEVICES

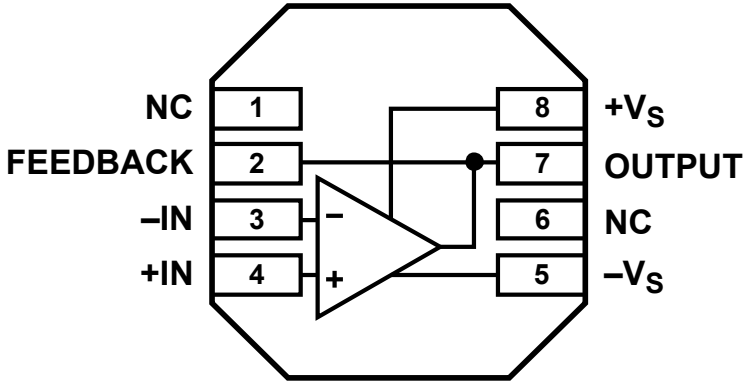
Analog Devices Low Distortion Pinout

- **Pinout enables compact layout**

Original Pin-Out



SOIC



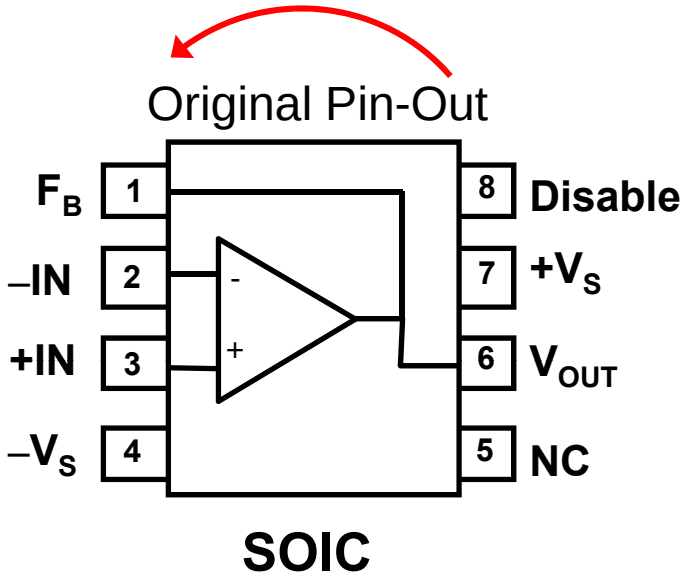
LFCSP

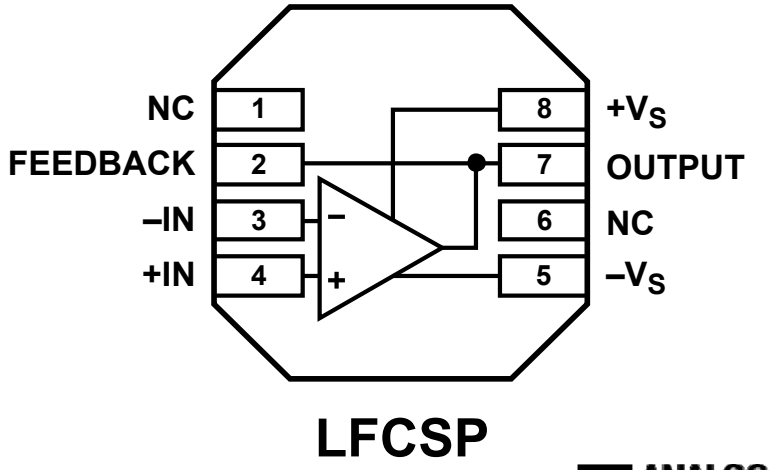
04814-0-001

ANALOG DEVICES

Analog Devices Low Distortion Pinout

- **Pinout enables compact layout**
- **Lower distortion**



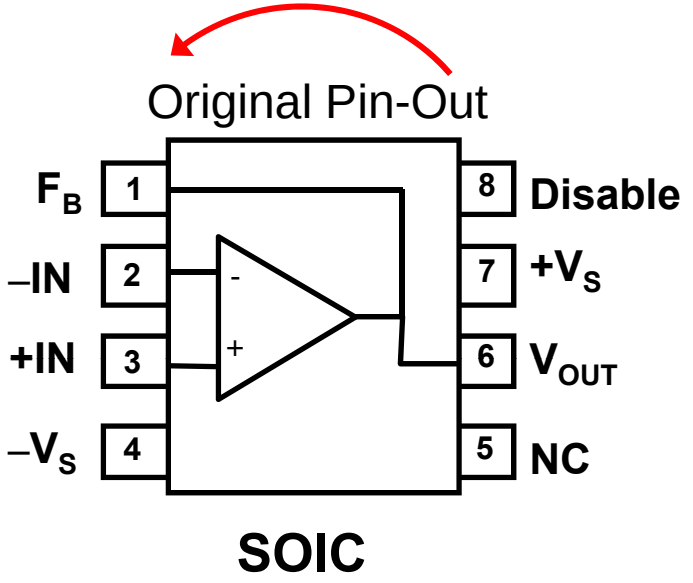


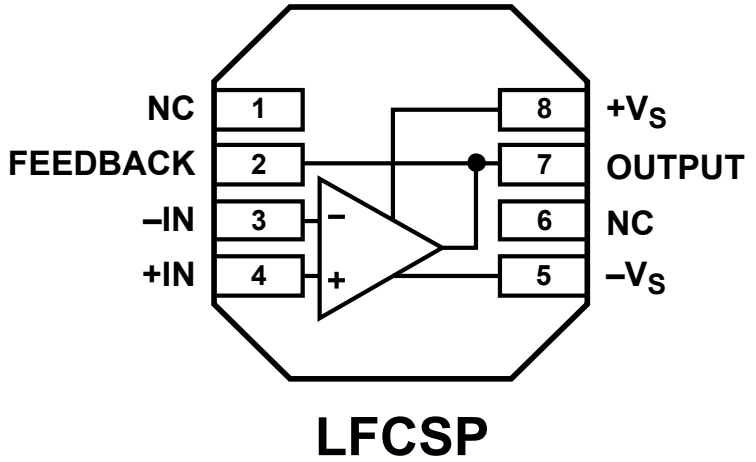
04814-0-001

ANALOG DEVICES

Analog Devices Low Distortion Pinout

- **Pinout enables compact layout**
- **Lower distortion**
- **Improved thermal performance**



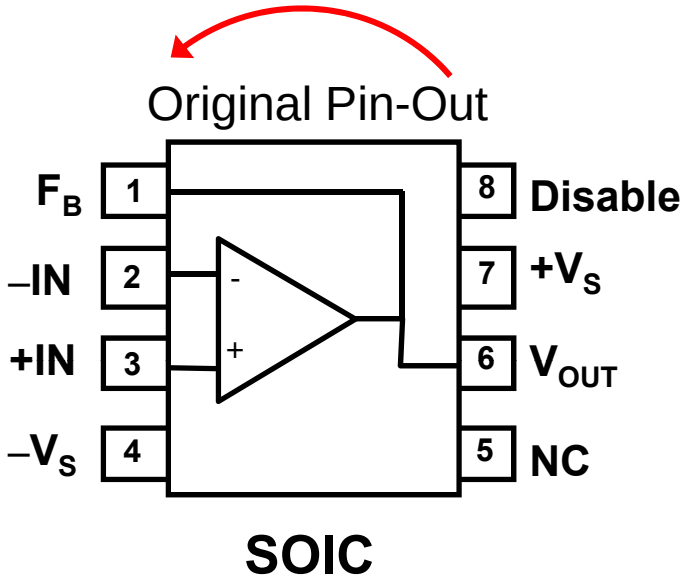


04814-0-001

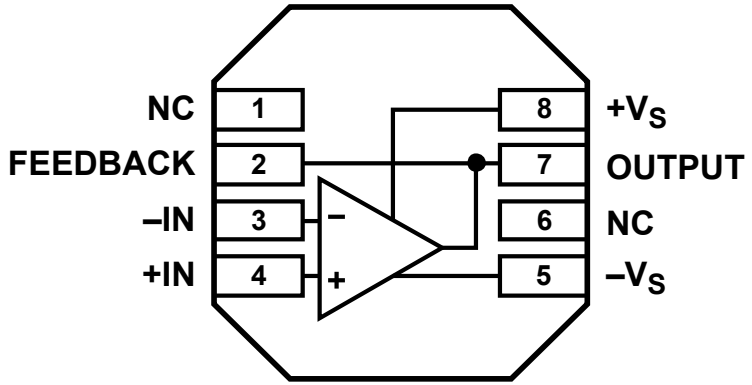
ANALOG DEVICES

Analog Devices Low Distortion Pinout

- **Pinout enables compact layout**
- **Lower distortion**
- **Improved thermal performance**
- **LFCSP**
  - **AD8099, AD8045, AD8000, ADA4899, ADA4857, ADA4817**



SOIC



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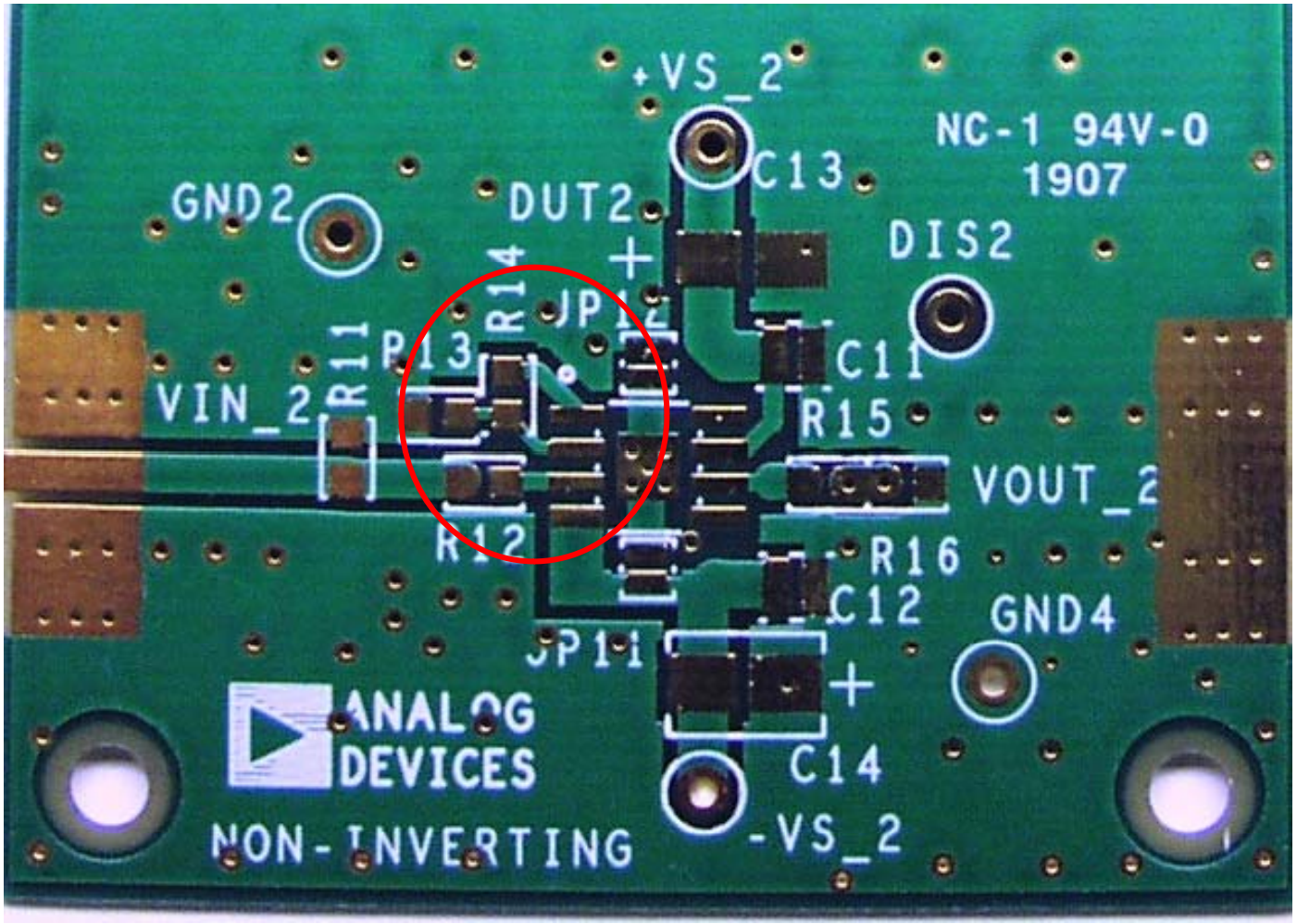
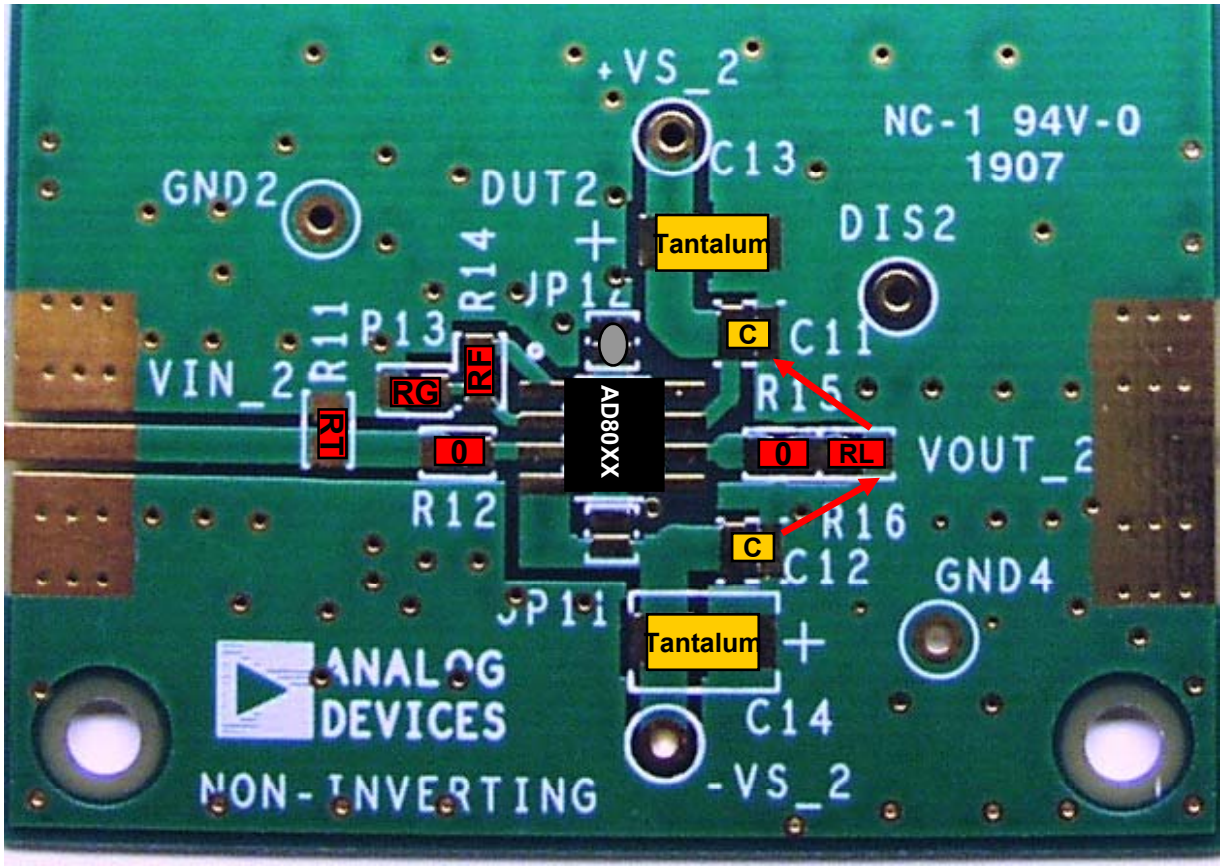
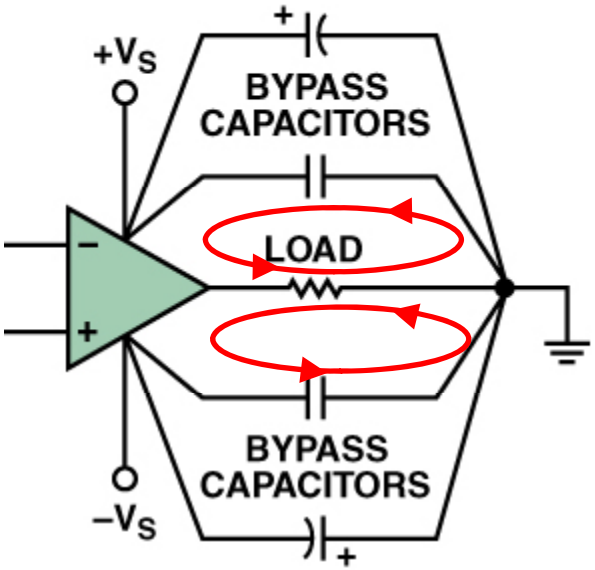
Low distortion pinout enables compact and streamline layout



Low distortion pinout enable compact and streamline layout





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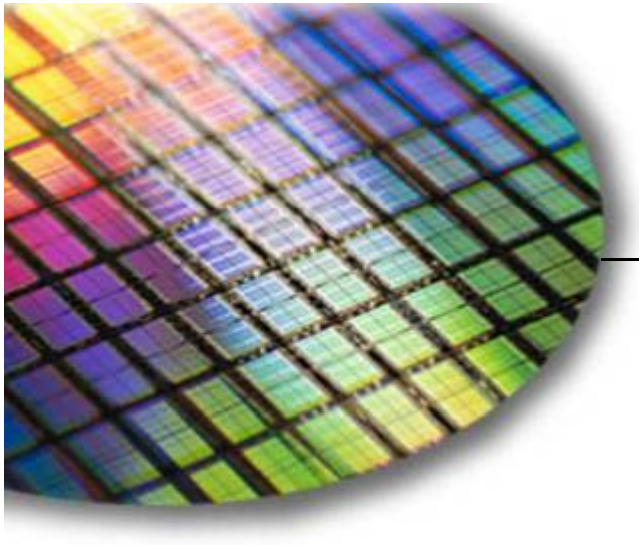

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RF Signal Routing and Shielding

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In This Section

- RF Components from Analog Devices
- PC Board Circuit Material Types and Minimizing Losses
- Microstrip and Stripline Transmission Lines
- Ground Plane Layout Considerations
- Developing a RF Printed Circuit Board
- Using Discrete Components with RF Devices
- Shielding of RF Circuit Boards

RF Components from Analog Devices

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Log Amps / Detectors
Mixers / Multipliers
Modulators / Demodulators
PLL Synthesizers/VCOs
RF / IF Amplifiers
RF / IF Transceivers
RF Switches
RMS Detectors
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Short Range Transceivers

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RF/IF Components

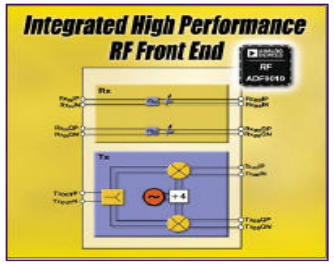
The ADF9010 is a fully integrated RF Tx modulator and Rx analog baseband front end that operates in the frequency range from 840 MHz to 960 MHz. The receive path consists of a fully differential I/Q baseband PGA, low pass filter, and general signal conditioning before connecting to an Rx ADC for baseband conversion. Learn more about the ADF9010.

Product Categories

- DDS Modulators
- Digital Up / Down Converters
- Direct Digital Synthesis (DDS)
- Log Amps / Detectors
- Mixers / Multipliers
- Modulators / Demodulators
- PLL Synthesizers/VCOs
- RF / IF Amplifiers
- RF / IF Transceivers
- RF Switches
- RMS Detectors
- RX / TX Subsystems
- Short Range Transceivers

News | New Products | Design Tools

- Analog Devices Introduces High-Performance Analog Front End for 900 MHz Band RF Applications.
- ADI's Digitally Programmable Variable Gain Amplifier and Driver is First to Drive Low Impedances from a Single Power Supply
- ADI's High-Performance RF Driver Amplifier Reduces Power, Size, and Cost of WiMAX and Wireless Applications



ADF9010

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http://www.analog.com/en/rfif-components/products/index.html

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Analog Devices Components Requiring Matched RF Interfaces

- **AD60x, AD8xxx and ADL533x series of RF/IF and Variable Gain Amplifiers**
- **ADF70xx and 702x series Radio Transmitters and Transceivers**
- **AD4xxx and ADF7xxx series of PLL Synthesizers and VCO's**
- **AD84xx and ADL53xx series of Modulators and Demodulators**
- **AD83xx and ADL539x series of Mixers and Multipliers**
- **AD83xx and ADL5519 series of Log Amps and Detectors**
- **AD836x and ADL550x series of RMS Detectors**
- **ADG9xx series of RF Switches**

PC Board Circuit Material Type and Minimizing Losses

- PC board material selection is usually based on price verses performance
- Select PC board dielectric material to have the lowest loss tangent
- Some types of “FR4” dielectric materials are low loss below 8-10 GHz
- PTFE(Teflon) dielectric material is usually used for the lowest loss at the higher RF and microwave frequency ranges, but at a much higher price
- Be sure that the correct impedance transmission line is used for the interconnection of the RF devices
- Use as wide of a transmission line as possible for the correct impedance, and try to keep it short to reduce “Skin Effect” losses
- Use high “Q”, or low loss passive components for all RF matching, coupling, and bypassing requirements

Microstrip and Stripline Transmission Lines

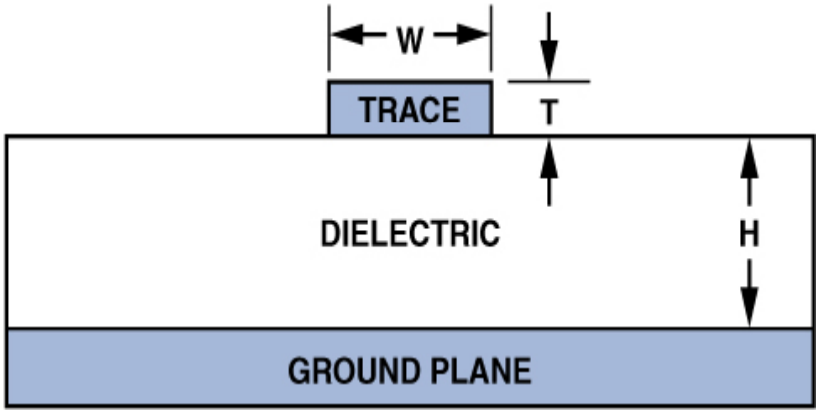
- 50 ohm interfaces are most often used between most “integrated” RF devices
- Interconnects less than 1/20 of a wavelength long can usually be made without a matched transmission line
- Avoid long microstrip lines as they could become “antennas”(microstrip) and radiate RF
- To minimize coupling to the transmission line, DO NOT place other traces or ground plane closer than three times of the dielectric height
- Use proper technique for making bends in microstrip lines
- Locate the microstrip lines on the component side of the board if possible

Microstrip Transmission Lines

Microstrip
Controlled Impedance Line Cross Section

- Advantages:
- Transmission line on outside layer of board
- Easy to attach components to trace
- Components can be placed at different locations along the line to aid in tuning
- Aid in RF testing as you are able to measure levels along the line

- Disadvantages:
- Slightly higher loss
- Not shielded and could radiate RF signal



$$Z_o = \frac{87}{\sqrt{\varepsilon_r} + 1.41} \ln\left[\frac{5.98H}{(0.8W + T)}\right]$$

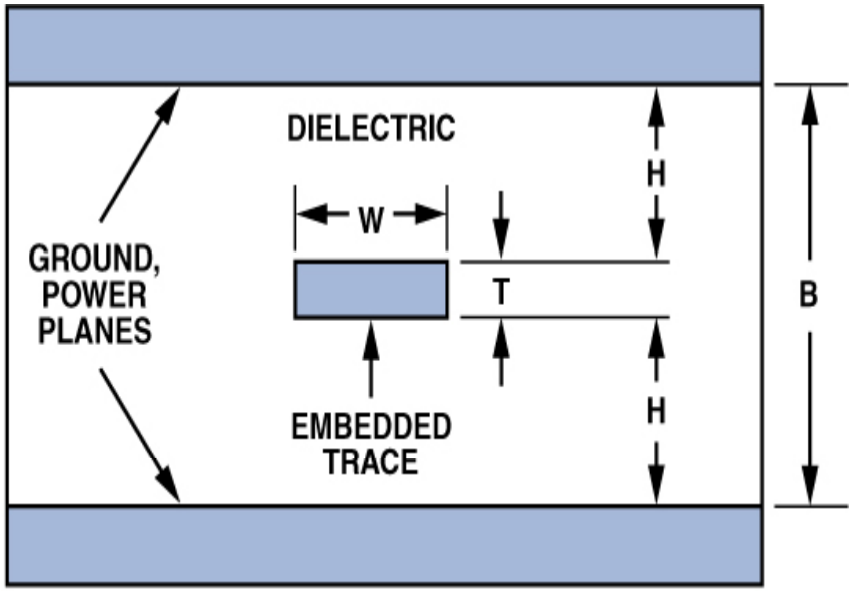
Stripline Transmission Lines

Stripline

Controlled Impedance Line Cross Section

- **Advantages:**
- **Lower loss at higher microwave frequencies**
- **Shielded transmission line, no RF radiation from board**

- **Disavantages:**
- **Requires vias to connect to line**
- **No ability to connect tuning or termination components to line**
- **No access to line to make adjustments or connections to line for RF testing**
- **Higher PCB cost**



$$Z_o(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right]$$

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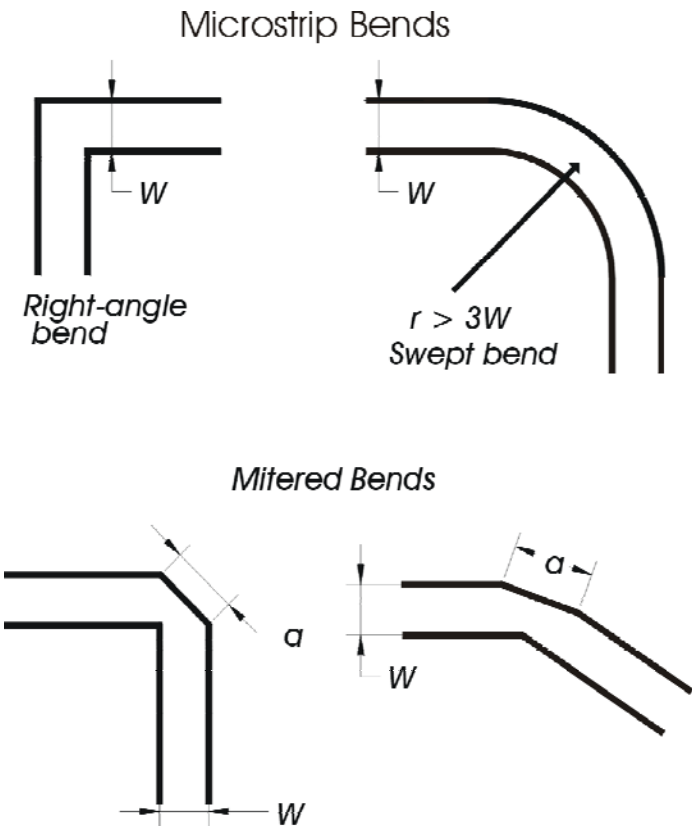
Microstrip and Stripline Transmission Lines

- **Bends in Microstrip and Stripline**
- **In order to preserve a constant impedance around a bend, some general layout rules MUST be followed**
- **DO NOT make a right angle bend as shown**
- **A right angle bend can be made with a "swept" bend, or a "Mitered" bend**
- **Bends in a transmission line that are less than 90 degrees can also be mitered as shown**



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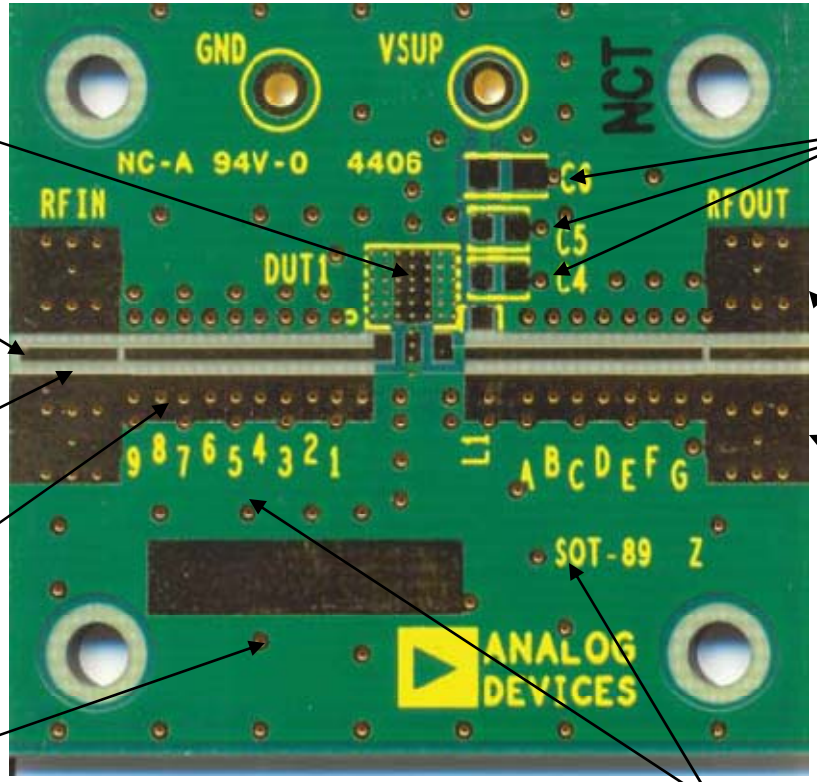
Ground Plane Layout Considerations

- Do NOT have breaks or voids in the RF ground plane under, or over RF transmission lines
- Ground plane Vias around the RF circuits should be spaced closer than 1/20 of a wavelength as a minimum, or closer if possible at the higher frequencies
- Use as large size vias as practical to minimize inductance
- "Stitch" the top and bottom ground planes together with as many vias as possible
- Signal and bias lines can be placed below RF ground plane layer followed by another "power" ground plane layer for the DC and digital returns
- Under components that require heat sinking, have solid ground plane with many closely spaced vias to transfer heat to all ground plane layers

Ground Plane Layout Considerations



Closely spaced vias under components requiring heat sinking

50 ohm microstrip transmission line

Proper spacing of ground plane away from transmission line (gap= 3 times dielectric height)

Closely spaced Ground plane vias along transmission line

"Stitch" ground planes together with multiple vias

Vias placed in ground plane at each end of the DC bias bypass components

Proper layout pattern for connecting edge mounted RF connector to PC board

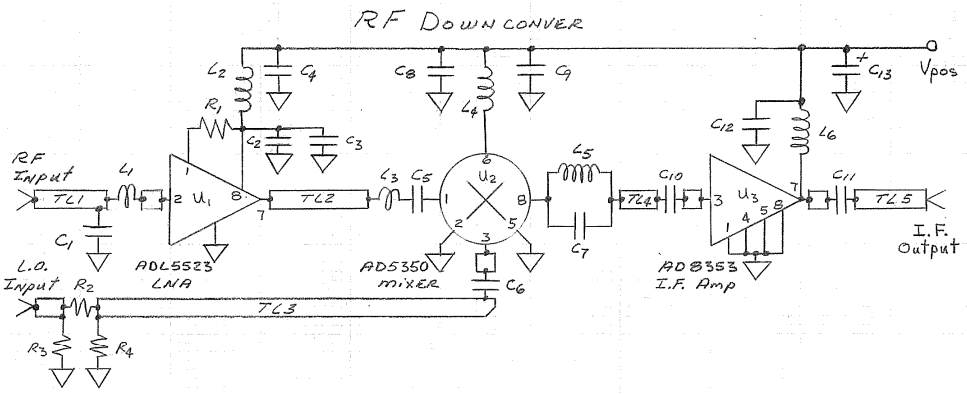
Maximum amount of ground plane on top and bottom sides of PC board

Developing a RF Printed Circuit Board

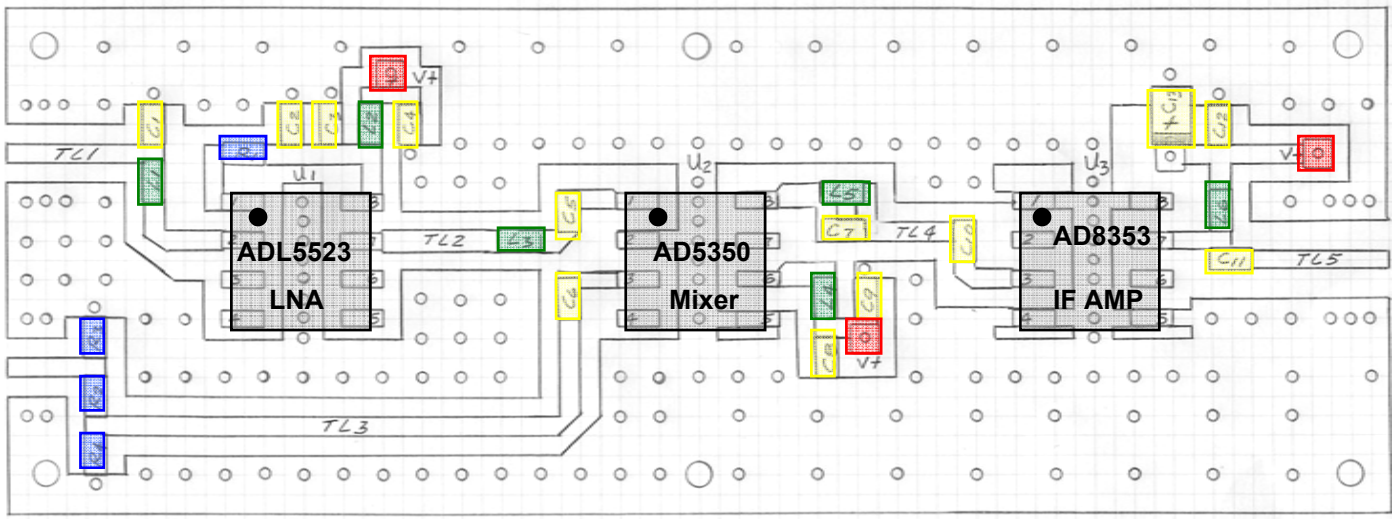
- Draw Schematic of circuit to be placed on the PC board
- Have data sheets on components to indicate pkg size, pinouts, etc
- Determine location and orientation of active devices to optimize RF interfaces
- Place RF matching/terminating components around the device to provide the shortest possible connections
- Use as small of mounting pad as possible with discrete RF components to keep stray capacitance to a minimum
- Observe proper orientation of discrete components if placed next to each other to avoid coupling effects
- Separate inductors from each other in the layout, or place perpendicular to each other to prevent coupling of their magnetic fields
- Make sure that components that are connected to the ground plane have a via(s) as close to the end of the component as possible
- Use wide power traces if possible to lower DC losses and provide higher stray capacitance to ground(will also act as a RF bypass cap)

Designing a RF Printed Circuit Board

- Draw Schematic of circuit



- Draw layout of components to optimize parts placement and interconnections



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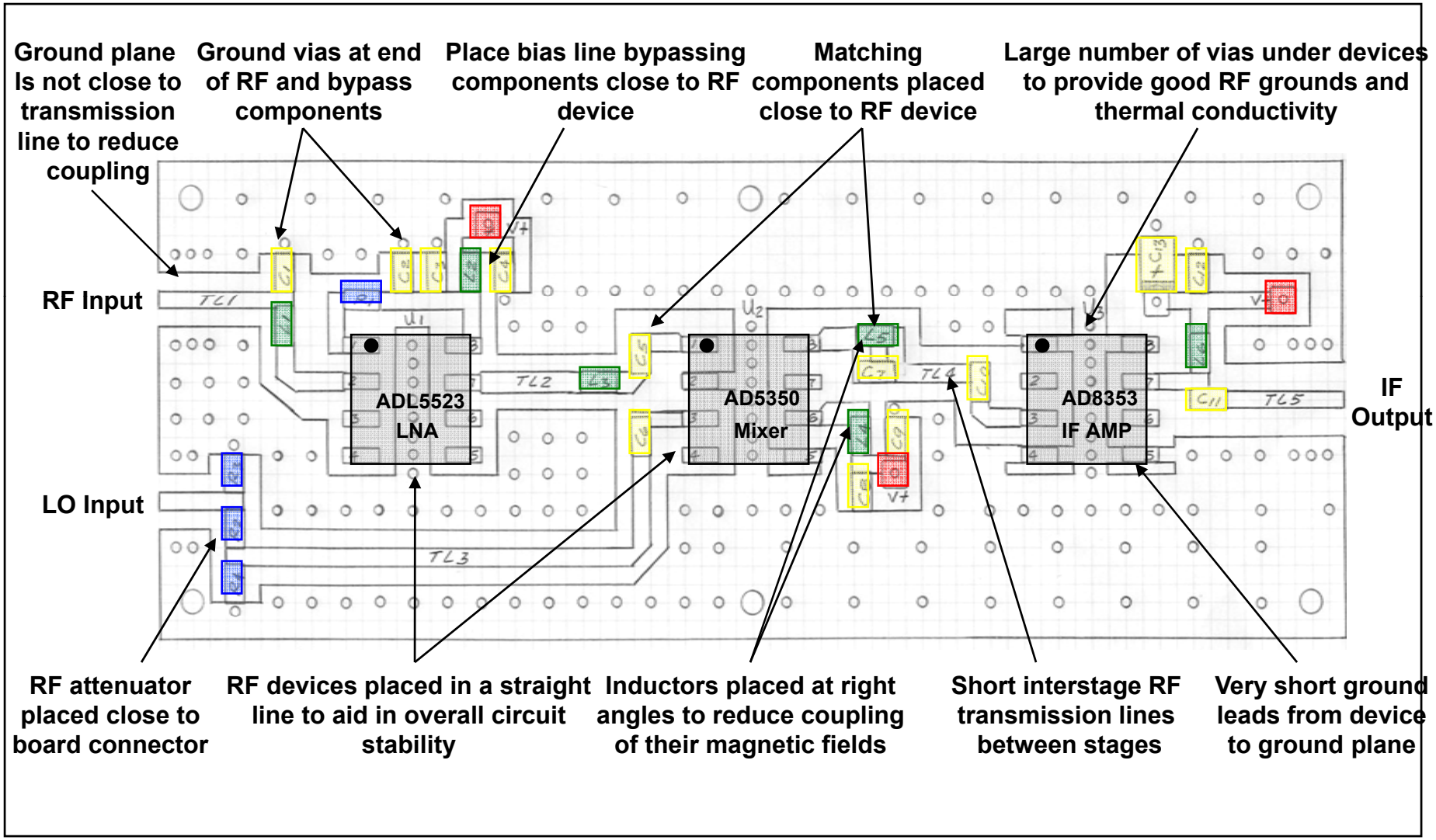
Designing a RF Printed Circuit Board



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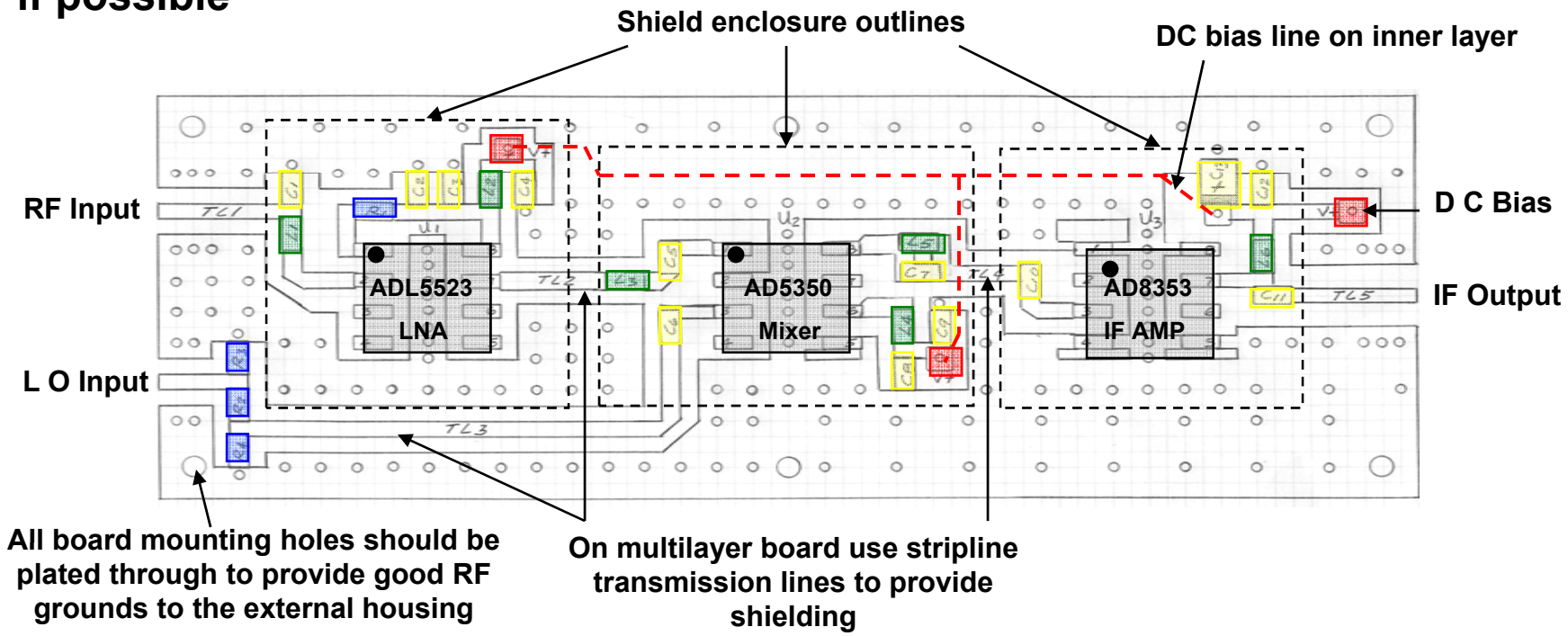
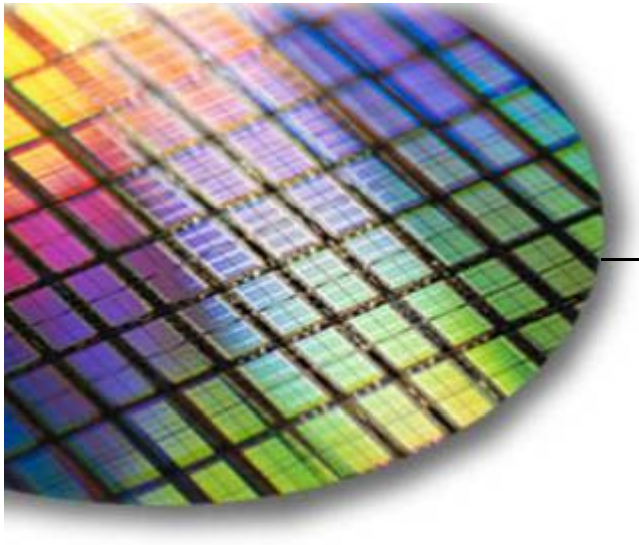
Shielding on RF Circuit Boards

- On multilayer circuit boards, use Stripline transmission lines if possible
- Route DC bias and signal traces on inner layers between the ground planes
- If required, place shielded enclosures around the RF stages on the board
- Be careful as to the physical size of the shielded enclosures, as it could become a resonate “cavity” at the higher frequencies
- Traces going to or from shielded sections should be routed on inner layers if possible





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Checking the Layout

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Checking the Layout

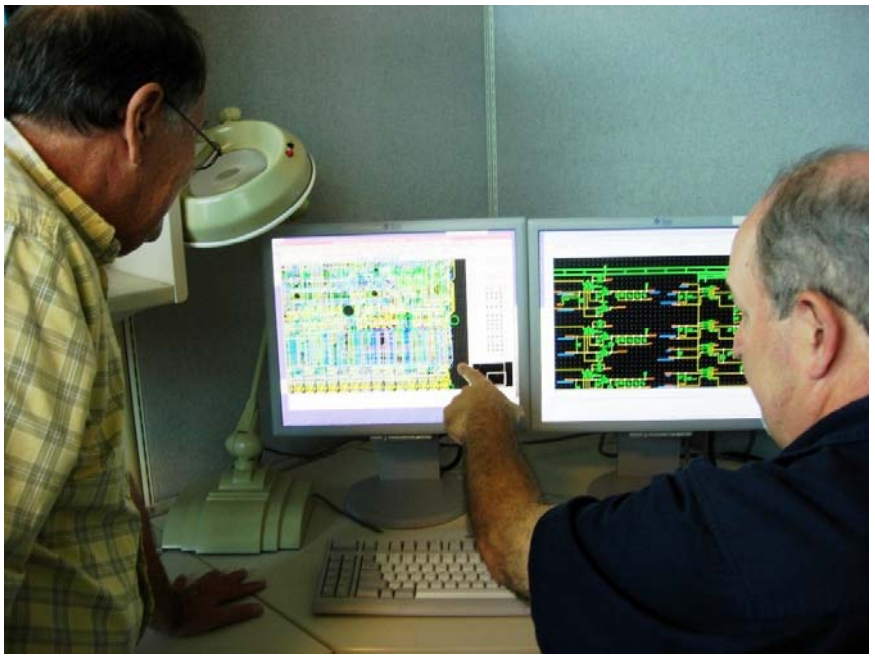
- **Design review**
- **Colleague review**

Checking the Layout

- Design review
- Colleague
- Colored pencils
  - Old School
  - Helps trace signal path on schematic and PCB

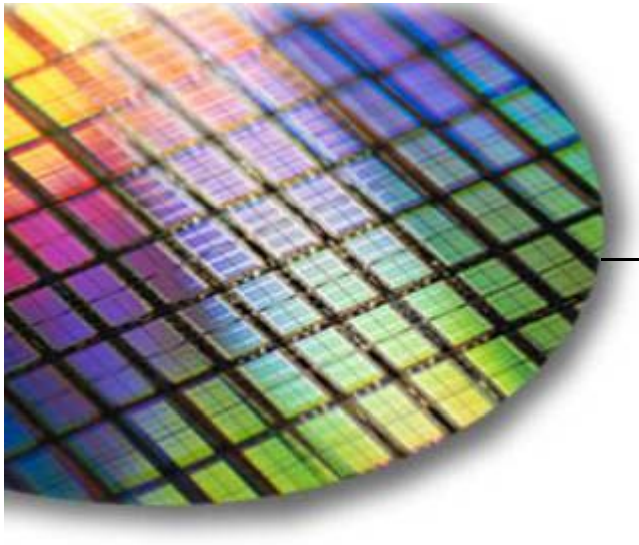
Checking the Layout

- Design review
- Colleague
- Colored pencils
  - Old School
  - Helps trace signal path on schematic and PCB
- Sit with the designer when board corrections are made
  - Trust no one
  - A change in one area of the board could inadvertently change another part of the board



Next Steps

- Order Boards
- Build and test
- Evaluate performance
- Iterate and try again if required
- Successful High Speed/RF PCB design is a combination of education and experience



Summary

Summary

- High speed PCB design requires deliberate thought and attention to detail!
- Load the schematic with as much information as possible
- Where you put individual components on the board is just as important as to where you put entire circuits
- Take the lead when laying out your board, don't leave anything to chance
- Use multiple capacitors for power supply bypassing
- Parasitics must be considered and dealt with
- Ground and Power planes play a key role in reducing noise and parasitics
- New packaging and pinout options allow for improved performance and more compact layouts
- There are many options for signal distribution, make sure you choose the right one for your application
- Check the layout and check it again
- Successful High Speed PCB design is a combination of education and experience and sometimes a little luck!

Summary

- Work directly with PC board designer as they most likely will not understand proper RF layout techniques
- Provide designer with a drawing of the location of the critical high frequency components and transmission lines
- Instruct the board designer that transmission line widths and lengths are very critical and must be exactly as calculated
- Place the components to minimize the length of RF interconnections
- Generally try to place components in a “straight line” to avoid feedback loops and instabilities
- Place circuit blocks such as oscillators, mixers, amplifiers in separate sections on the board if possible
- Do NOT mix digital, low level analog, or bias traces with RF interconnects to avoid unwanted coupling
- Locate the components operating at the highest frequencies close to board interconnects
- With the PC board designer, check, and recheck the layout before sending out for fabrication

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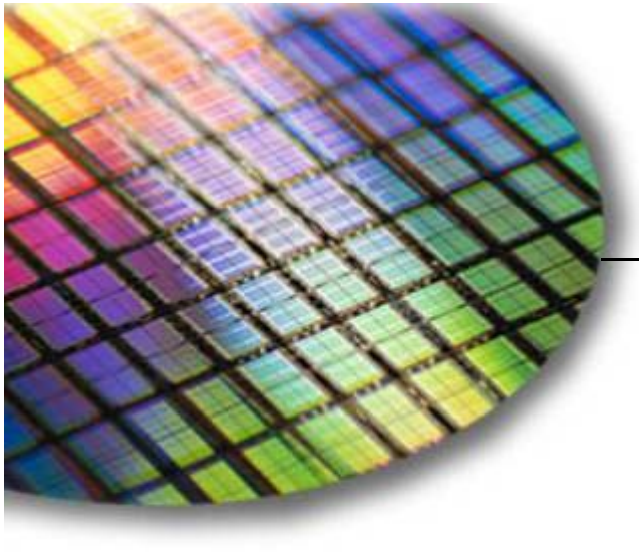

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