OEM Reader Module – LF read-only

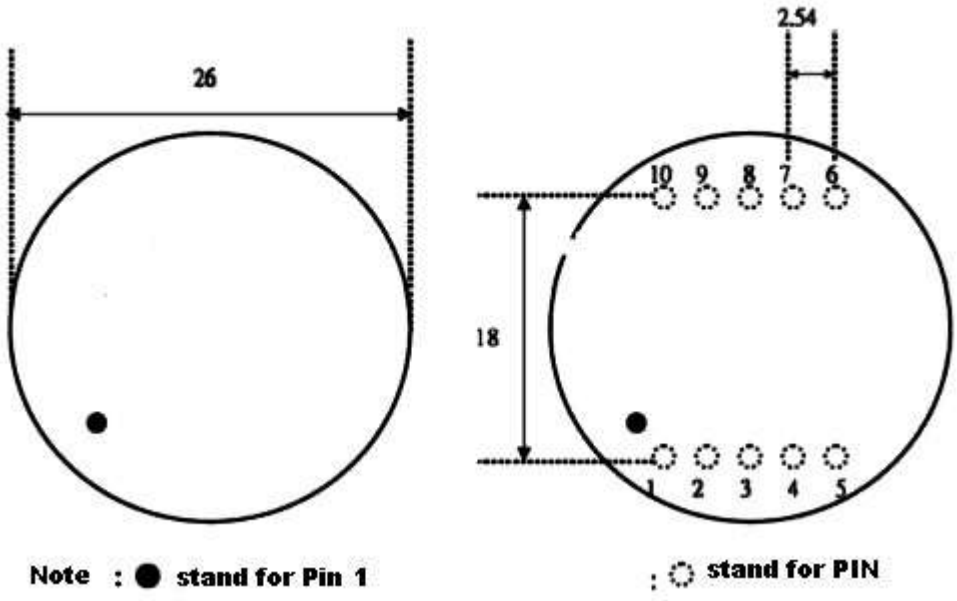
This iDTRONIC reader module has been designed for build of simple access control readers and for applications in machines and production equipment. The development of this product has been focussed on small size and convenient price

The module is specially designed for read EM card. The output interface can be Wiegand 26 or serial format.

Product specification:

Dimensions:	26 mm (circular diameter) × 8.5 mm (thickness)
Interfaces:	Serial (TTL comp.) or Wiegand 26 bits
Reading distance:	up to 10 cm (depending on tag size)
Decoding time:	Less then 100 ms decoding time
Power supply:	5 VDC (±5 %)
Current consumption:	40 mA @ 5 V nominal
I/O output current:	25 mA sink/source
Operating temperature:	-40 °C to +85 °C
Storage Humidity:	5–95 % RH
Possible transponders:	EM 4100
Order number:	R-OEM-LF-RO

Trim Size Sketch:



The rectangular pins have a width of 0.65 mm.
In most PCBs a round hole of ø 0.8 mm will be sufficient.

The pins protrude app. 4.2 mm long.

A.) Pinout and Electrical Characteristics

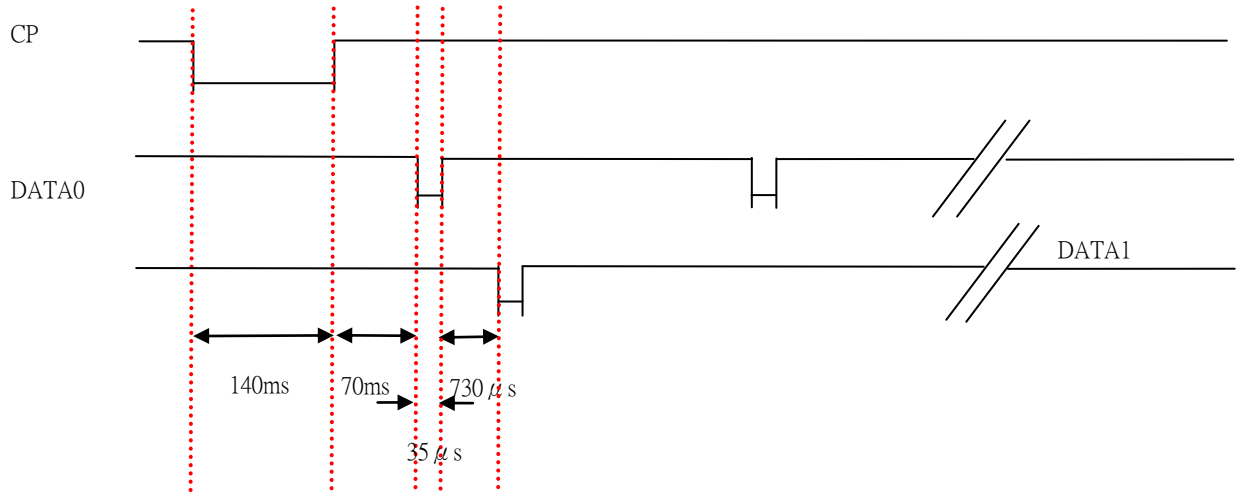
PIN	NAME	I/O	SYMBLE	MIN	TYP	MAN	DESCRIPTION
1	**CP**	**O**	**Vo-H Vo-L**	**Vcc-0.2V -**	**Vcc GND**	**Vcc+0.2V Vss+0.2V**	**Low Pulse 140ms**
2	**CP**	**O**	**Vo-H Vo-L**	**Vcc-0.2V -**	**Vcc GND**	**Vcc+0.2V Vss+0.2V**	**Low Pulse 140ms**
3	**DATA1**	**O**	**Vo-H Vo-L**	**Vcc-0.2V -**	**Vcc GND**	**Vcc+0.2V Vss+0.2V**	**Digital data output**
4	**DATA0**	**O**	**Vo-H Vo-L**	**Vcc-0.2V -**	**Vcc GND**	**Vcc+0.2V Vss+0.2V**	**Digital data output**
5	**Reserved**	**I**					**Low active, unused**
6	**ASCII/ WIEGAND**	**I**					**HI: ASCII Default: Wiegand26**
7	**GLED**	**O**	**Vo-H Vo-L**	**Vcc-0.2V -**	**Vcc GND**	**Vcc+0.2V Vss+0.2V**	**High active**
8	**RLED**	**O**	**Vo-H Vo-L**	**Vcc-0.2V -**	**Vcc GND**	**Vcc+0.2V Vss+0.2V**	**Low active**
9	**VCC**		**Vcc**	**3.5V-**	**5V**	**5.25V**	**VCC**
10	**GND**						**Ground**

Remark:
If Wiegand output is selected by PIN 6, connect only PIN 3 (DATA1), PIN 4 (DATA0), PIN 9 (Vcc), PIN 10 (GND). It is not needed to connect PIN 6, when PIN 6 connecting with High level, the output will be as ASCII, while Low/open/default selects Wiegand26 protocol.

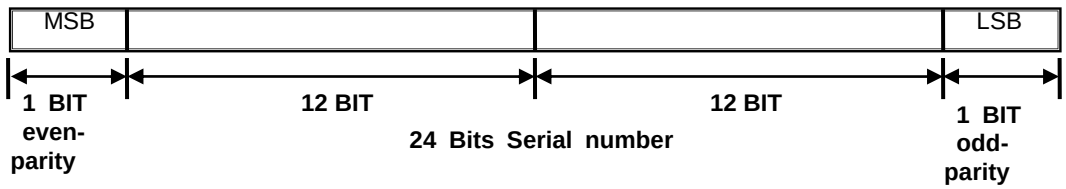
B.) Wiegand Code:

When card comes in, CP transmit about 140 ms LOW PULSE.
When card comes in, After CP transmit signal about 70 ms, then start to transmit D0 & D1 signal.
D0 & D1 signal, BIT & BIT about 730 µs(HI time).
D0 & D1 signal BIT LOW PULSE about 35 µs.

1.Scheduling sketch map



2.Data output format



- **MSB send first**
- **MSB 12Bits use even-Parity，LSB 12 Bit use odd-parity。**

C.) Serial Interface (TTL compatible):

1. Data output format

   a. **9600bps, N, 8, 1**

   b. **PIN5: TX non-invert output**

   c. **PIN6: TX invert output**

   d. **CHECKSUM: Cards of 10 bytes DATA, all use XOR operation**

02	10 ASCII Data Characters	Checksum	03
STX	UID	CHK	ETX

Example

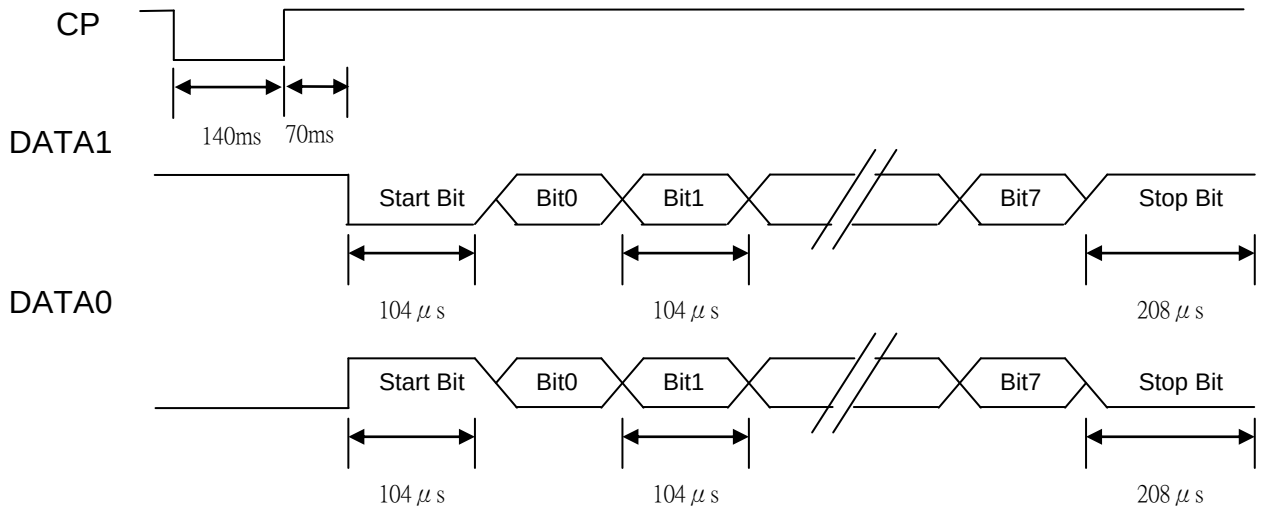
Card number: **62E3086CED (hex value)**

Checksum: (62H) XOR (E3H) XOR (08H) XOR (6CH) XOR (EDH) = 08H

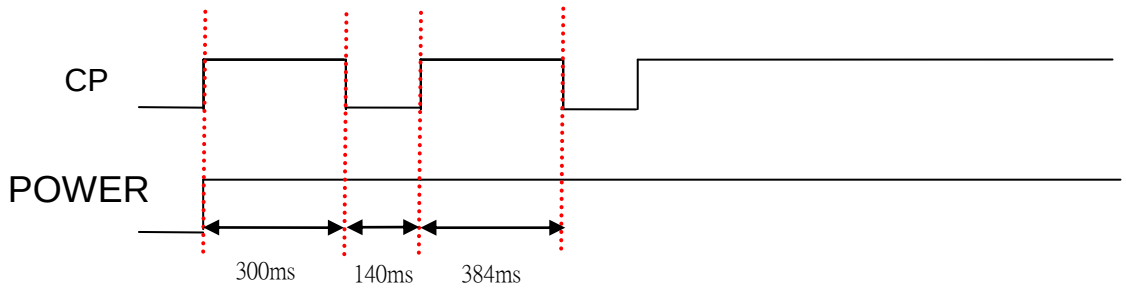
Values in telegram:

36H (ASCII '6'), 32H (ASCII '2'), 45H (ASCII 'E'), 33H (ASCII '3'), 30H (ASCII '0'), 38H (ASCII '8'), 36H (ASCII '6'), 43H (ASCII 'C'), 45H (ASCII 'E'), 44H (ASCII 'D'), 30H (ASCII '0'), 38H (ASCII '8')

2. Scheduling sketch map

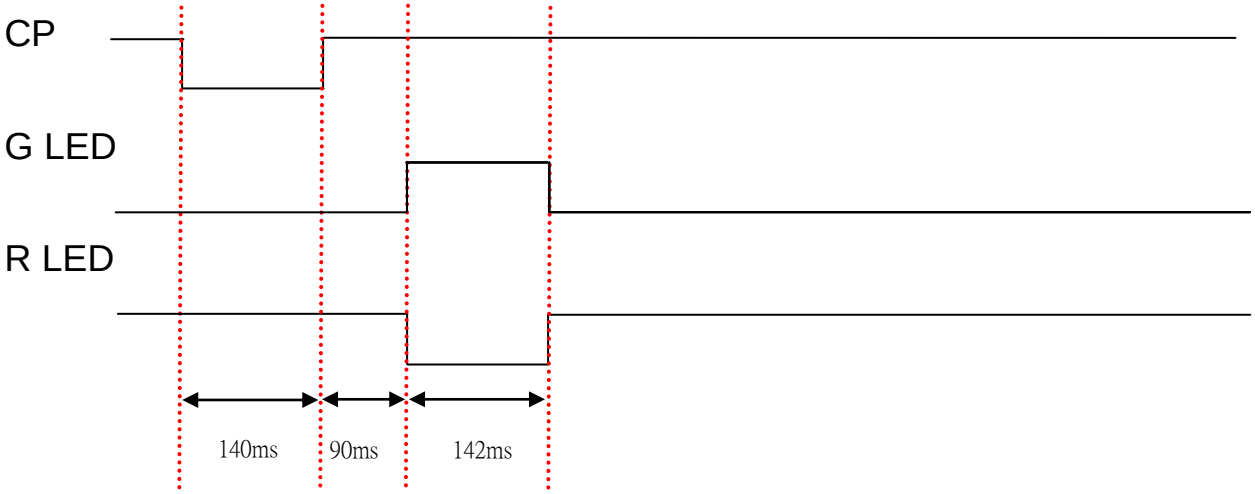


D.) Startup:



E.) LED:

1. Data output format:
   a. **When card comes in, after CP transmit signal for about 90 ms, then start to transmit G LED signal (normal as LOW) HI PULS around142 ms**
   b. **When card comes in, after CP transmit signal for about 90 ms, then start to transmit R LED signal (normal as HI) LOW PULSE around142 ms**
2. Scheduling sketch map



F.) Reference application circuit diagram: