

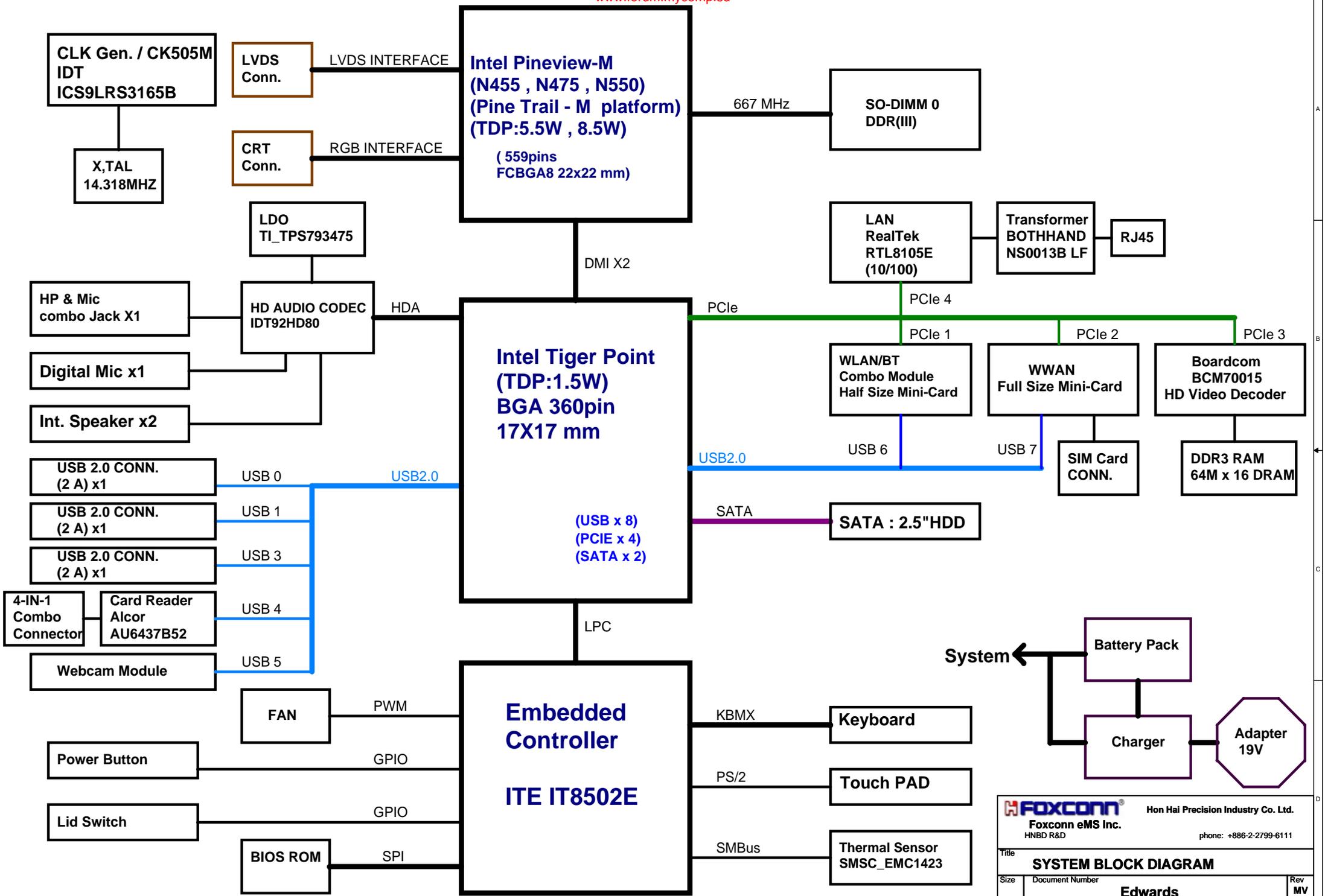
Edwards1.1 and Nano1.0 UMA MV Schematic

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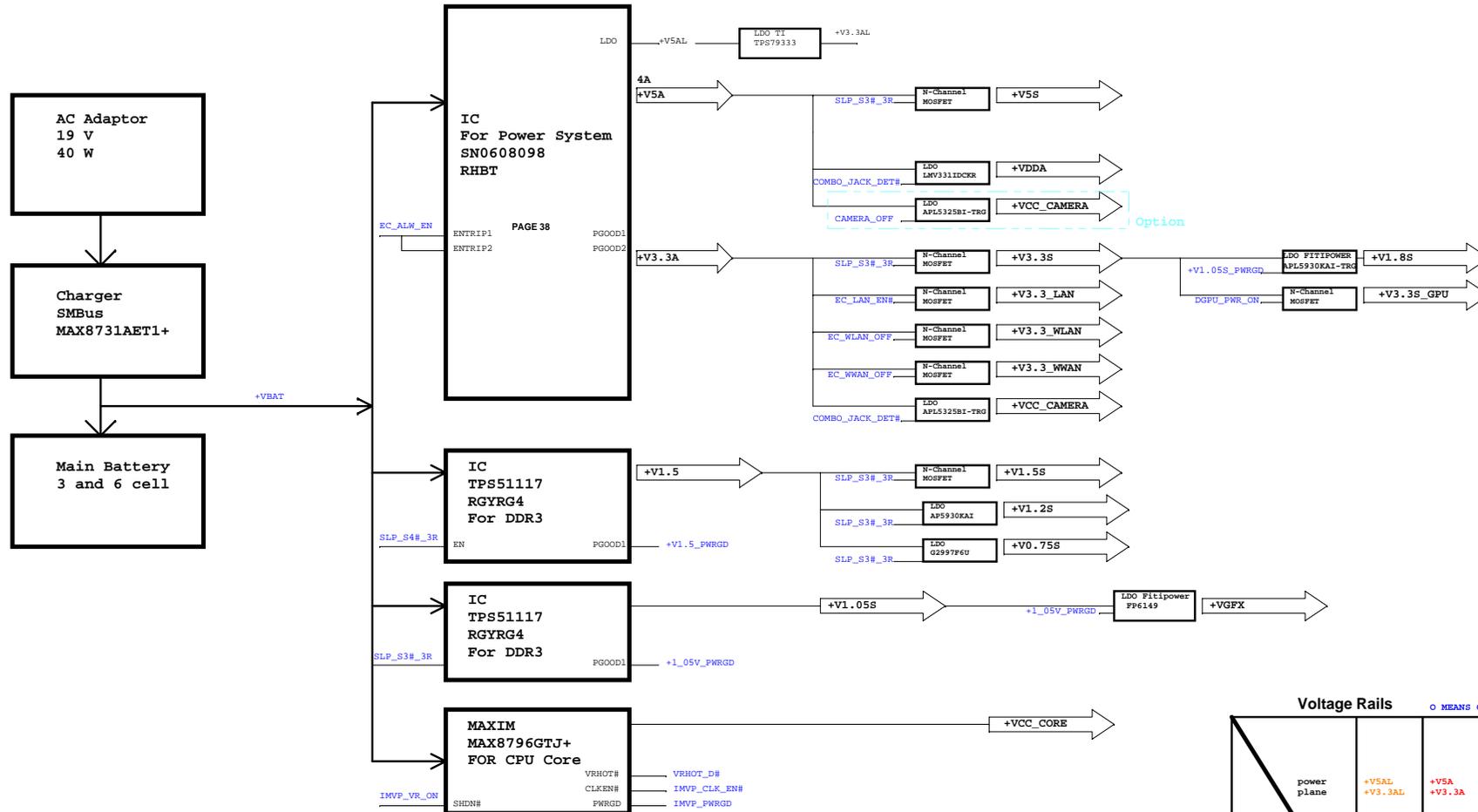
MB

P02 : SYSTEM BLOCK DIAGRAM	P24 : LAN (RTL8105E)
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P19 : TIGERPOINT(GND)5/5	
P20 : LVDS & Webcam	
P21 : WLAN & WWAN	
P22 : EC+KBC (IT8502E)	
P23 : CODEC/COMBO JACK/SPEAKER	

P. Leader	Check by	Design by
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Title		
COVER SHEET		
Size	Document Number	Rev
	Edwards	MV
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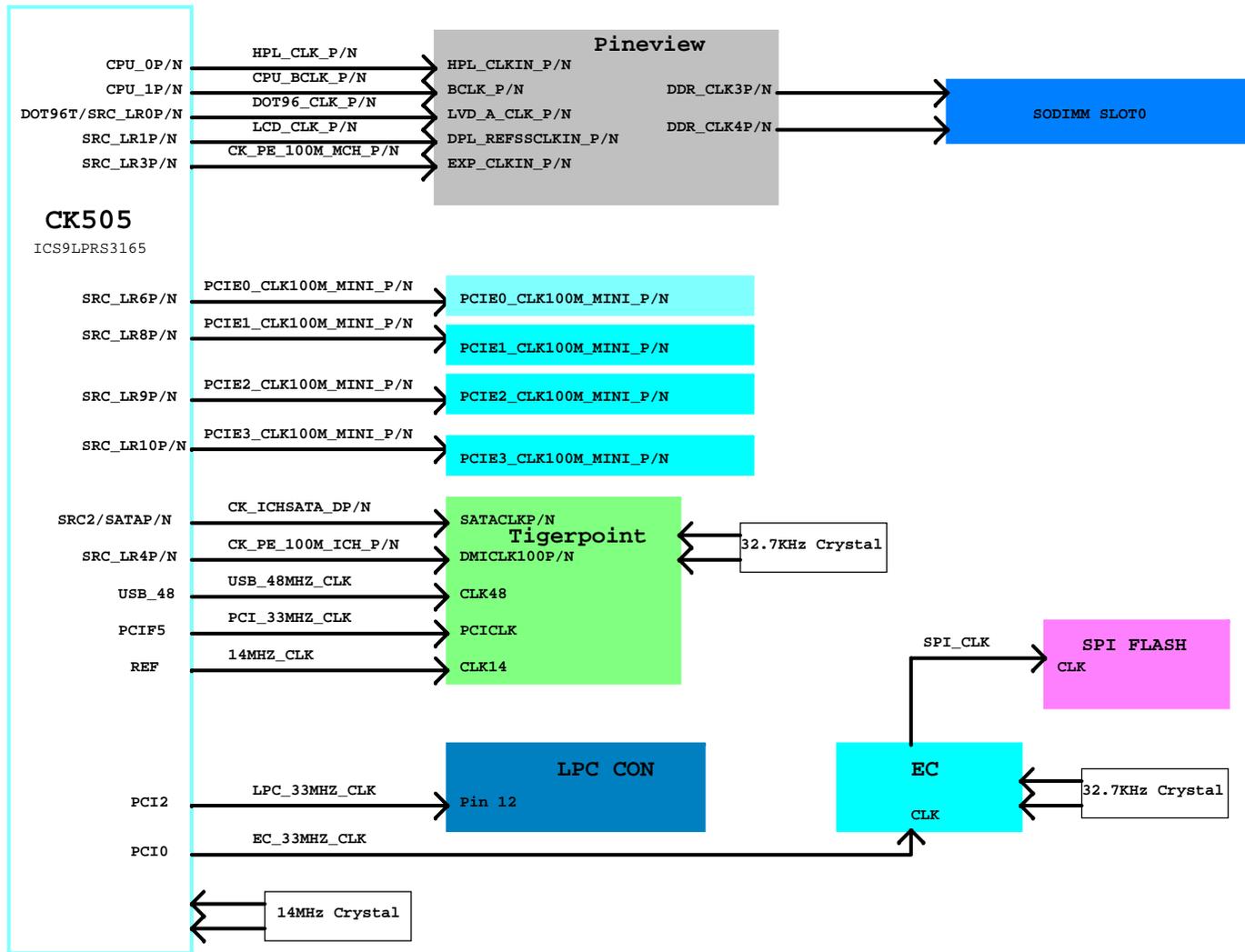
Edwards Power Block Diagram



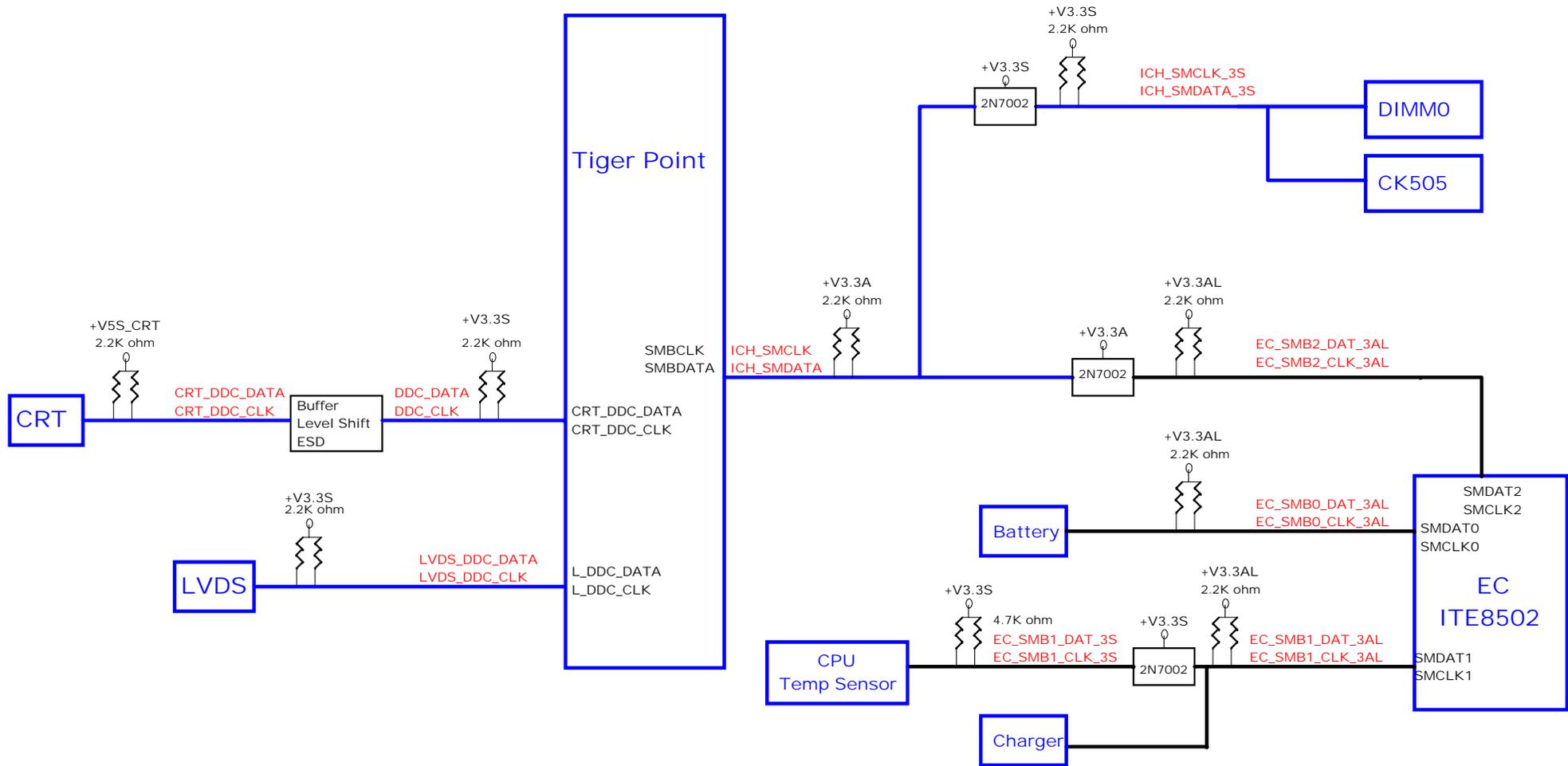
Voltage Rails O MEANS ON X MEANS OFF

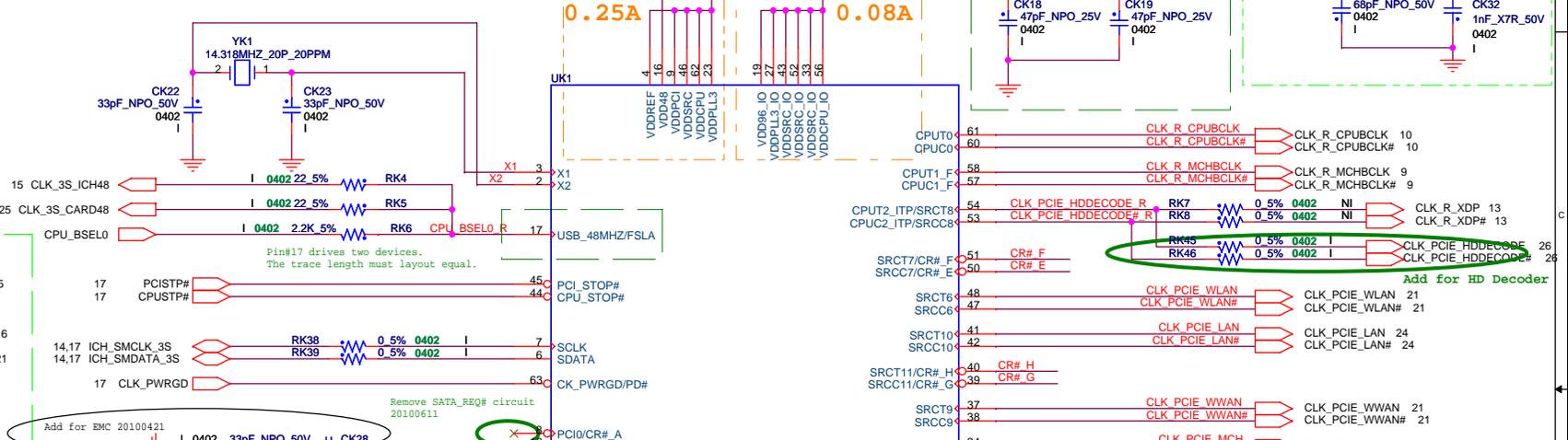
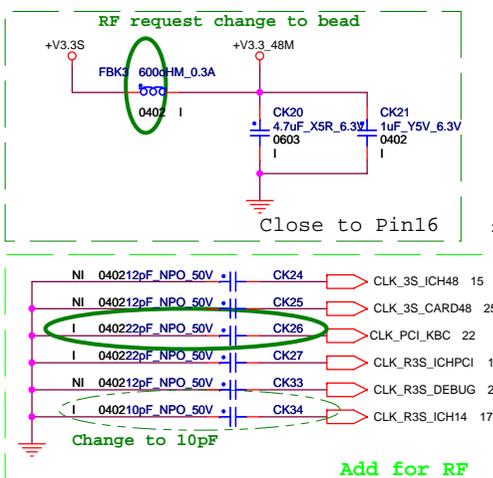
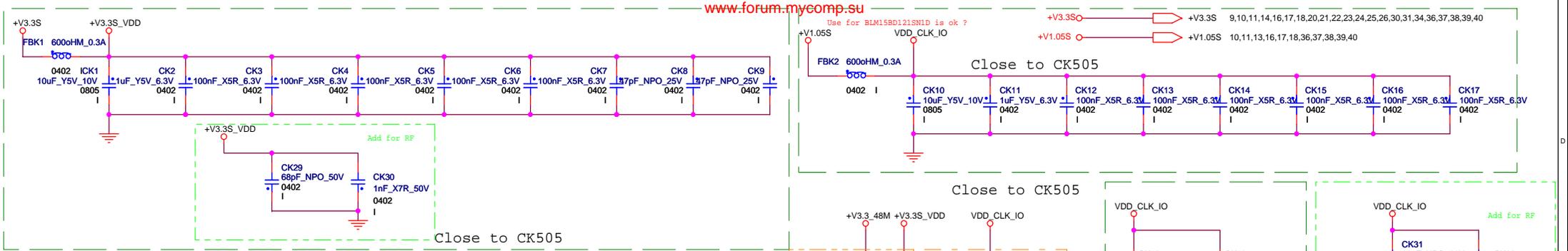
power plane \ State	+V5A +V3.3A	+V5A +V3.3A	+V1.5	+V5S +V3.3S +V1.8S +V1.5S +V1.05S +V0.75S +VGFYX +VCC_CORE +V1.2S +V1.5S_HD
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist (G3)	X	X	X	X

S3 : STR
S4 : STD
S5 : SOFT OFF
G3 : ME OFF

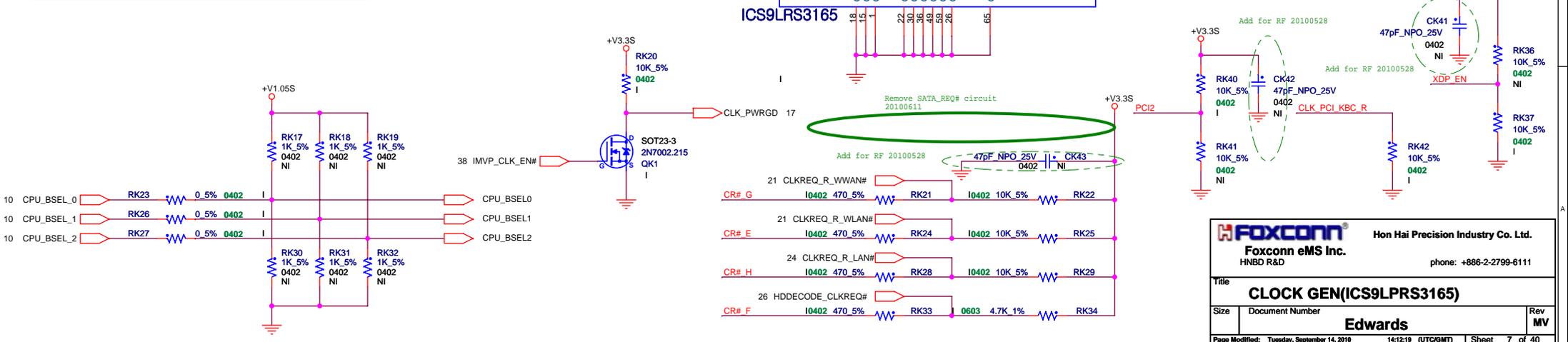


SMBUS&I2C MAP





SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

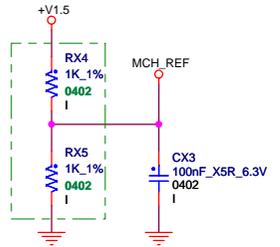
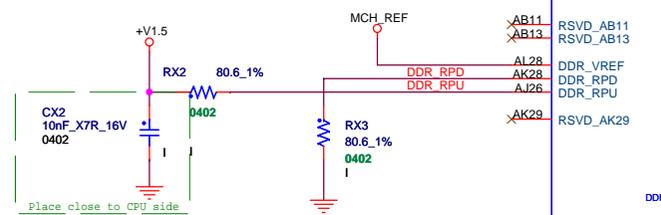
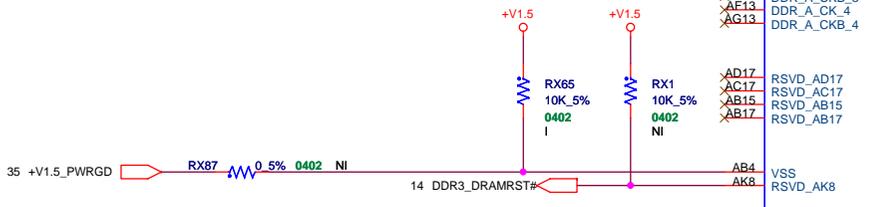
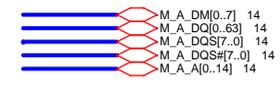
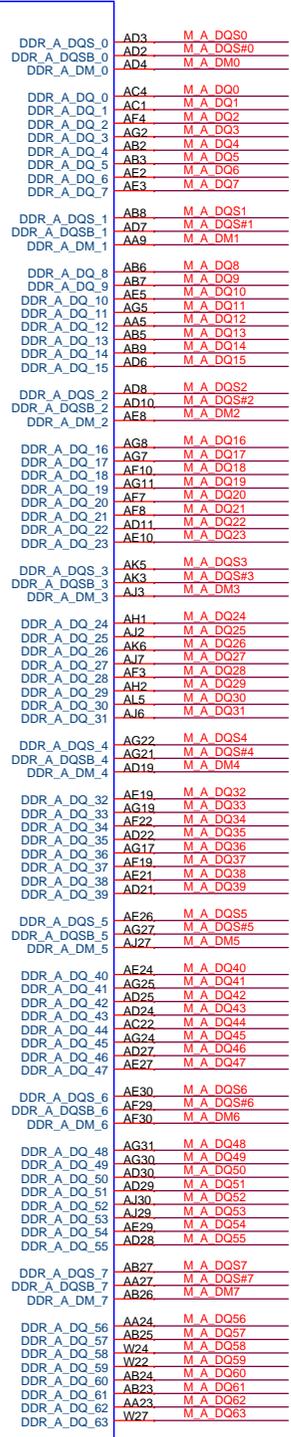
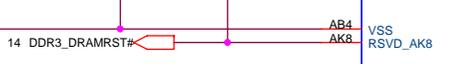
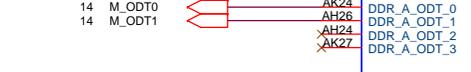
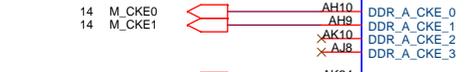
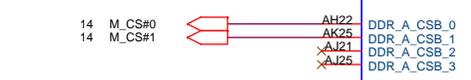
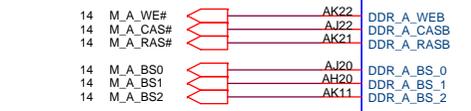
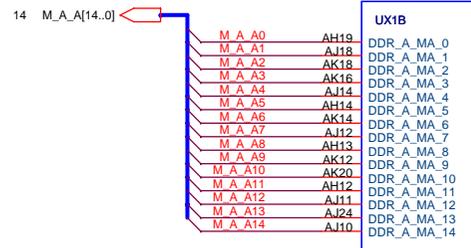


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Title: **CLOCK GEN(ICS9LPRS3165)**

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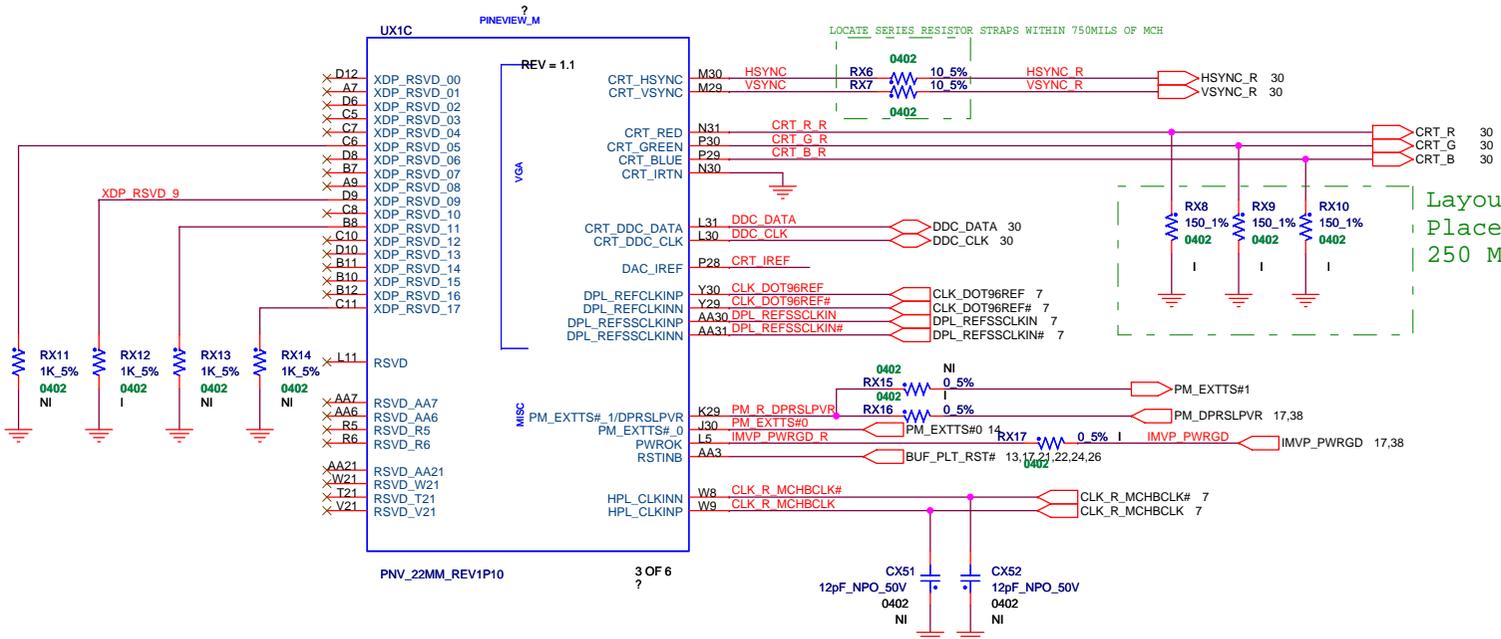
Layout Notes :
Place RX3 and RX4 close to CPU pins on M_REF

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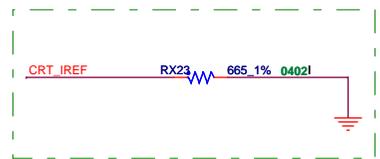
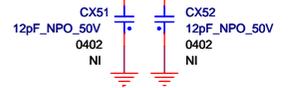
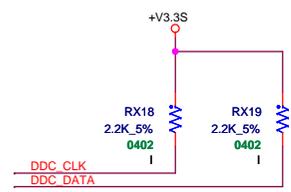
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Size: Document Number: **Edwards** Rev: **MV**

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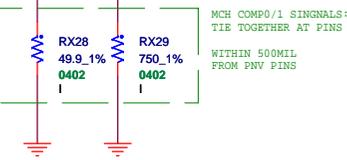
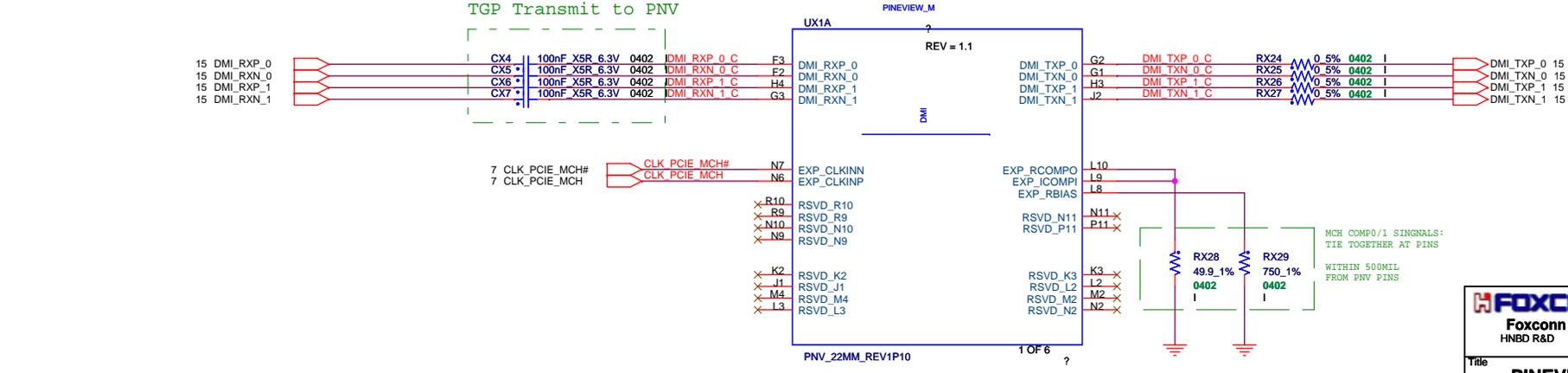


Layout Notes :
Place RX7 , RX8 and RX9 close to CPU
250 MIL TO BALL



Layout Notes :
Place RES close to CPU
500 MIL TO BALL

Layout Notes :
AC Couple
TGP Transmit to PNV

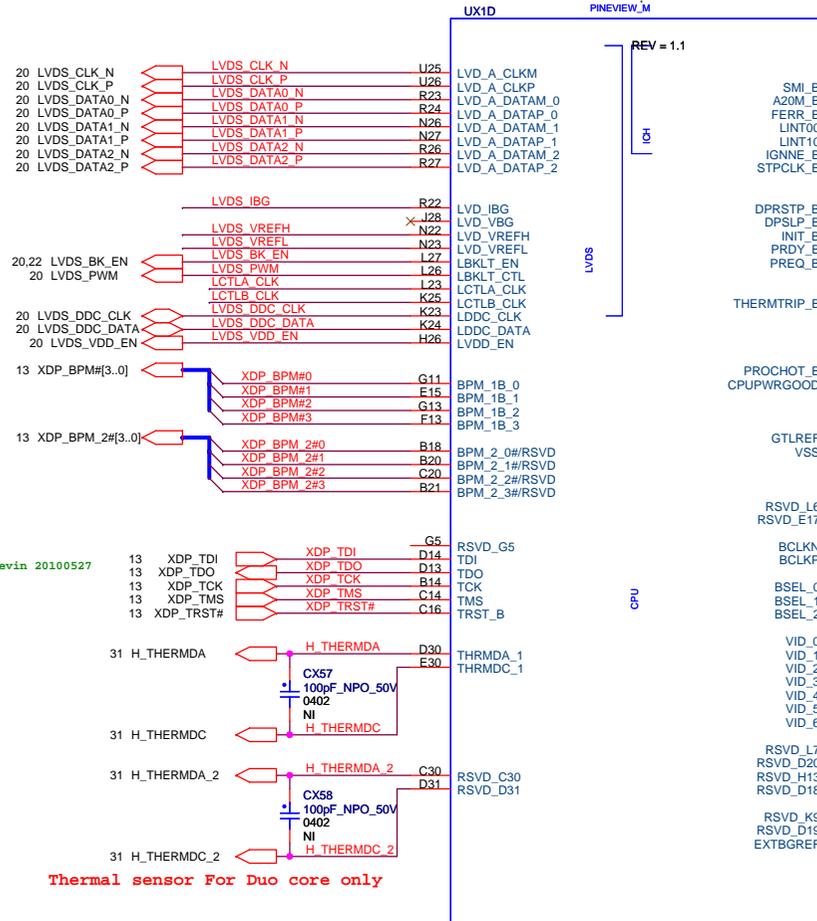


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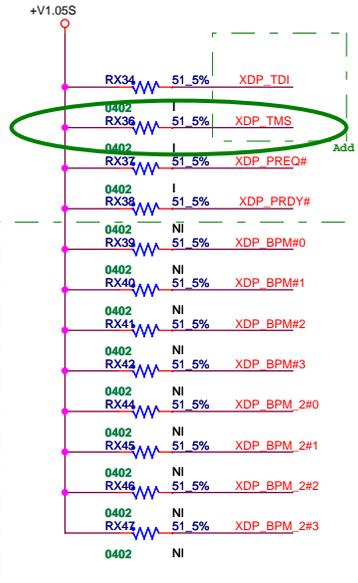
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Layout Notes :
Place TDI/TMS Termination Near CPU

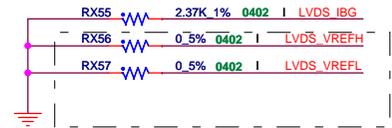
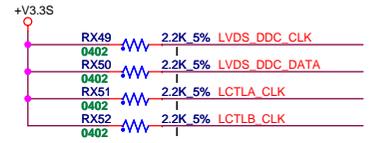
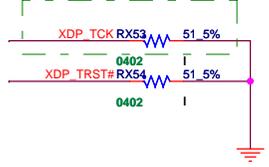


Add by Kevin 20100527

Thermal sensor For Duo core only

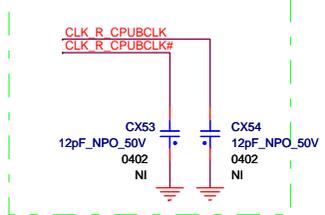
Layout Notes :
PlaceBPM Termination Near CPU

Layout Notes :
Place TCK Termination Near CPU

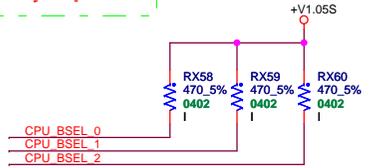


Layout Notes :
PlaceResistors CClose to CPU

Add for RF



Layout Notes :
EXTBGREF MAX TRACE LENGTH OF 500 MIL
AND 5 MIL SPACING within 0.5" of CPU



Layout Notes :
Place Near GTLREF'S Pins
CPU GTLREF Need to be at
2/3 of VCCP 1.05s

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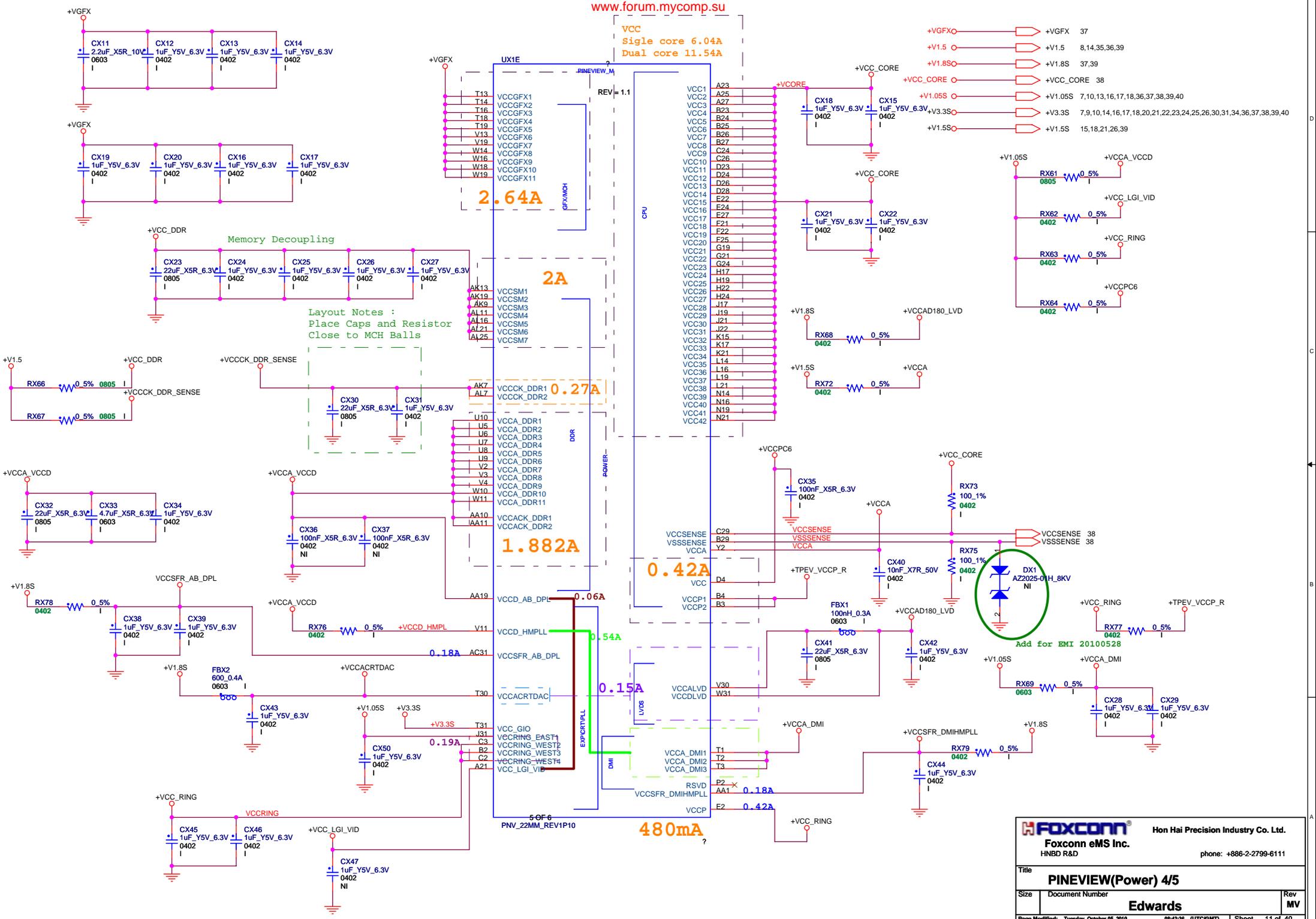
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Size: Document Number: **Edwards** Rev: **MV**

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vcc
Single core 6.04A
Dual core 11.54A

- +VGFXX 37
- +V1.5 8,14,35,36,39
- +V1.8SO 37,39
- +VCC_CORE 38
- +V1.05S 7,10,13,16,17,18,36,37,38,39,40
- +V3.3S 7,9,10,14,16,17,18,20,21,22,23,24,25,26,30,31,34,36,37,38,39,40
- +V1.5S 15,18,21,26,39

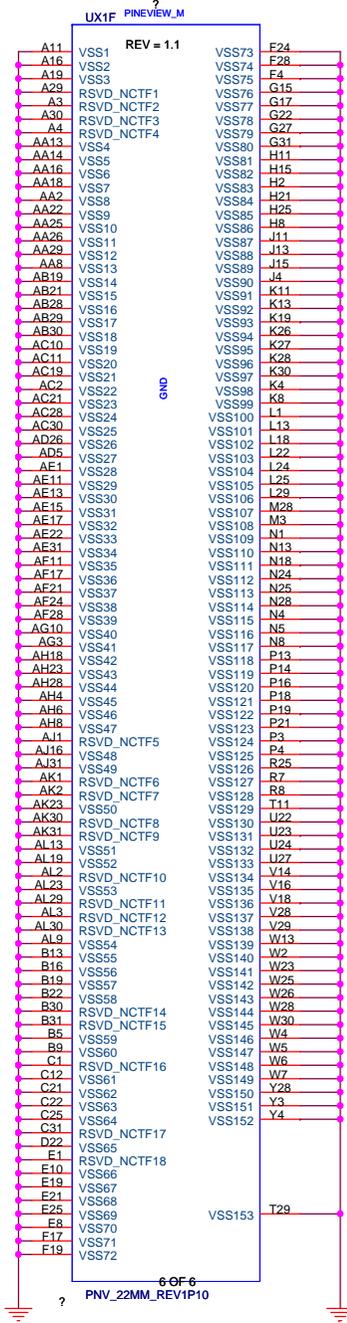


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Title: **PINEVIEW(Power) 4/5**

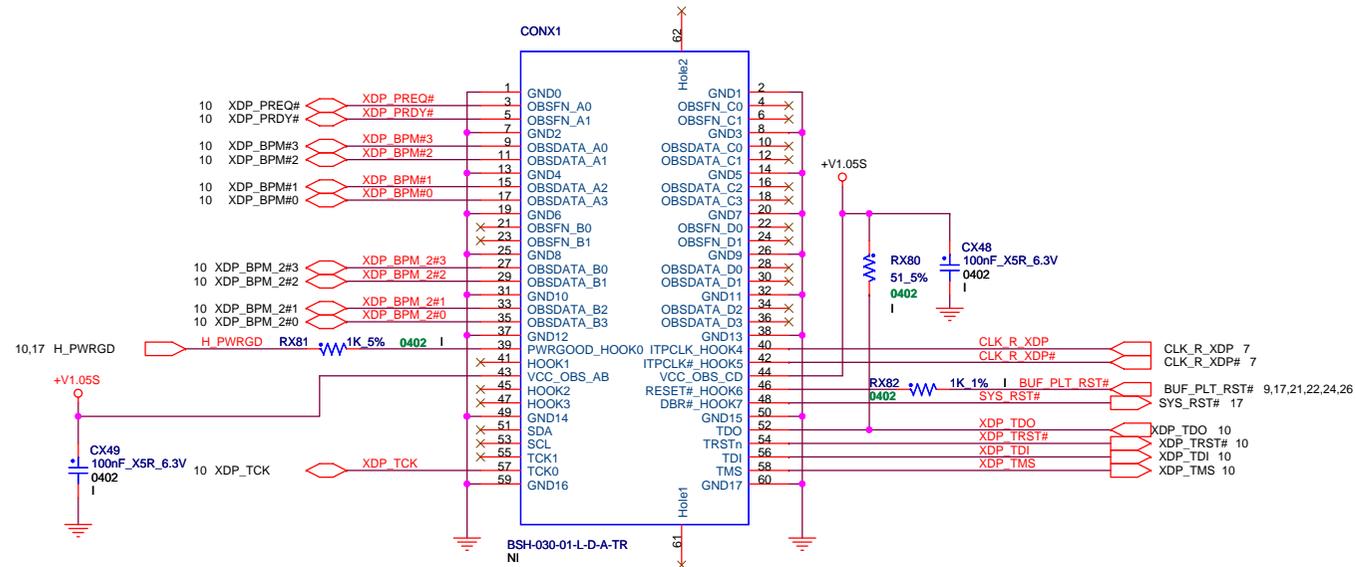
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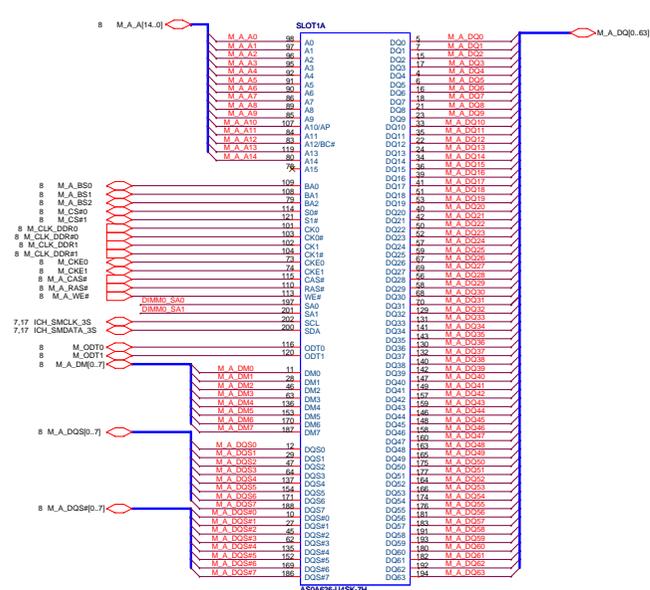


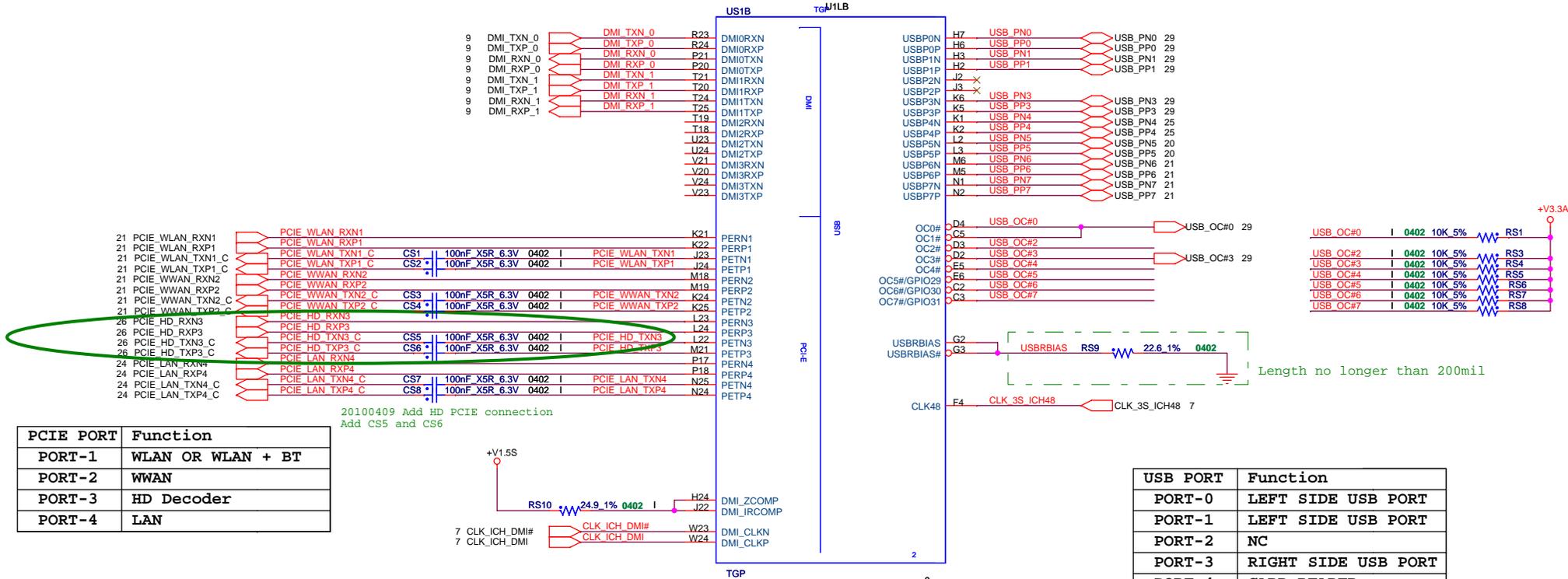
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Title			
PINEVIEW(GND) 5/5			
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+V1.05S +V1.05S 7,10,11,16,17,18,36,37,38,39,40



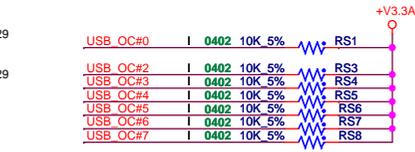
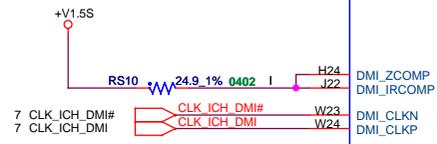
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XDP			
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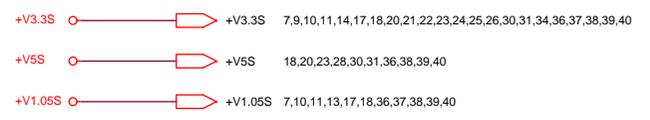
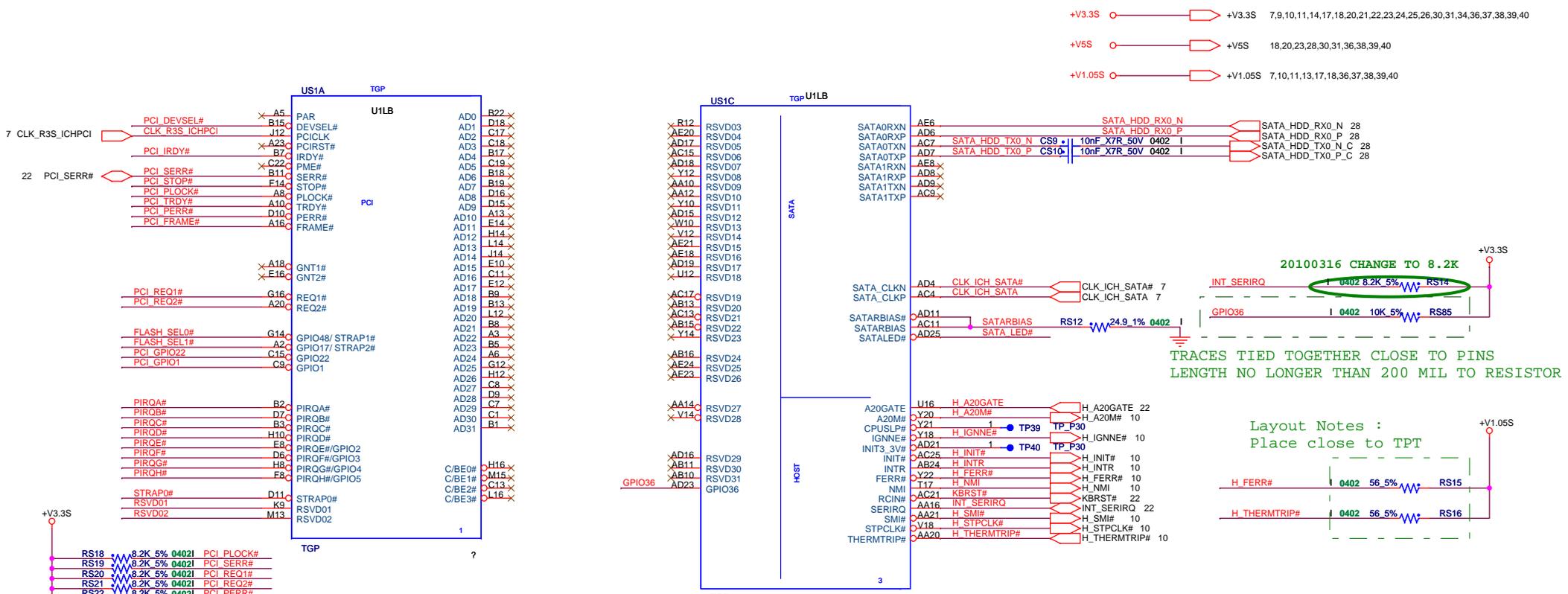
20100409 Add HD PCIE connection
Add CS5 and CS6

PCIE PORT	Function
PORT-1	WLAN OR WLAN + BT
PORT-2	WWAN
PORT-3	HD Decoder
PORT-4	LAN

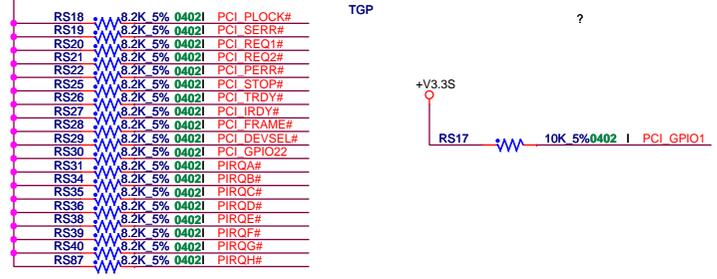
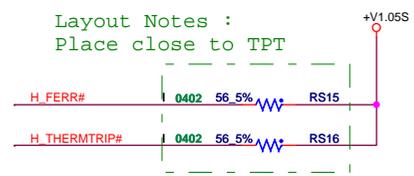


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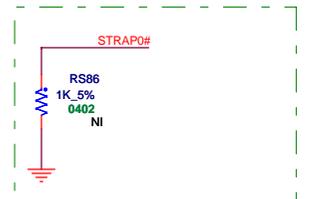
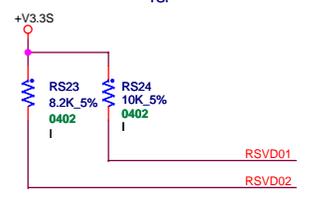
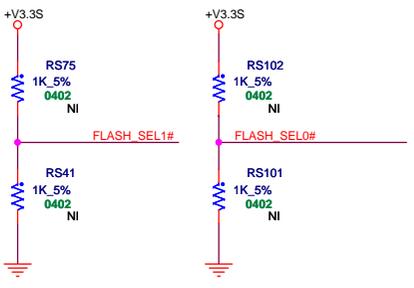
USB PORT	Function
PORT-0	LEFT SIDE USB PORT
PORT-1	LEFT SIDE USB PORT
PORT-2	NC
PORT-3	RIGHT SIDE USB PORT
PORT-4	CARD READER
PORT-5	CAMERA
PORT-6	WLAN OR WLAN + BT
PORT-7	WWAN



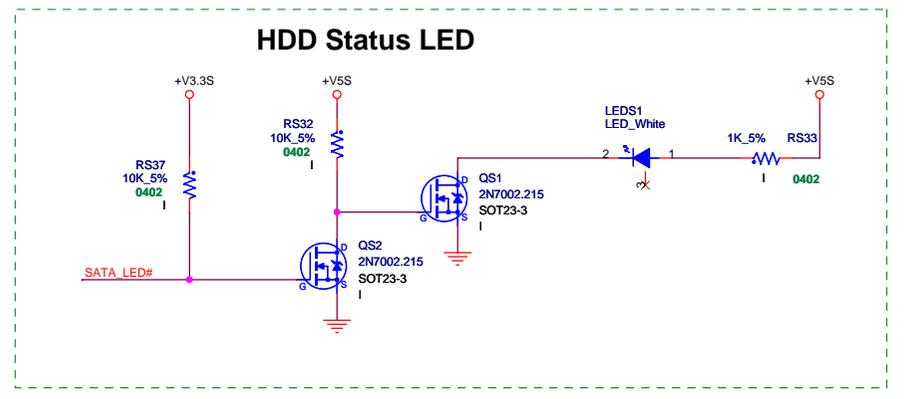
20100316 CHANGE TO 8.2K
 INT SERIRQ I 0402 8.2K 5% RS14
 GPIO36 I 0402 10K 5% RS85
 TRACES TIED TOGETHER CLOSE TO PINS
 LENGTH NO LONGER THAN 200 MIL TO RESISTOR



	STRAP	FLASH_SEL1	FLASH_SEL0
LPC	11	HIGH	HIGH
PCI	10	HIGH	LOW
SPI	01	LOW	HIGH



STRAP0#: Top-Block Swap Override.
 If the signal is sampled low, this indicates that the system is strapped to the "top-block swap" mode (Tiger Point inverts A16 for all cycles targeting FWH BIOS space)

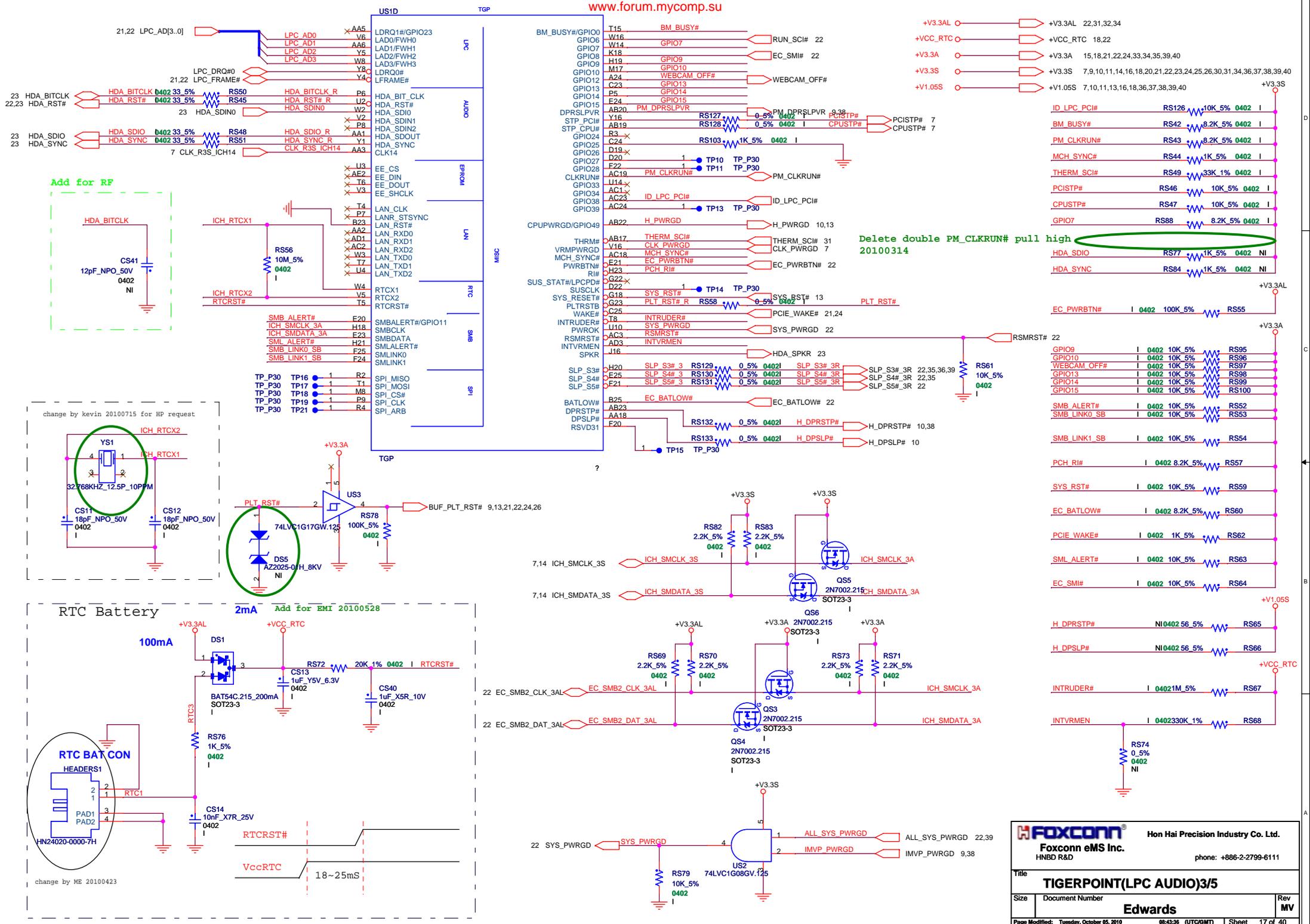


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Title: **TIGERPOINT(SATA and PCI)2/5**

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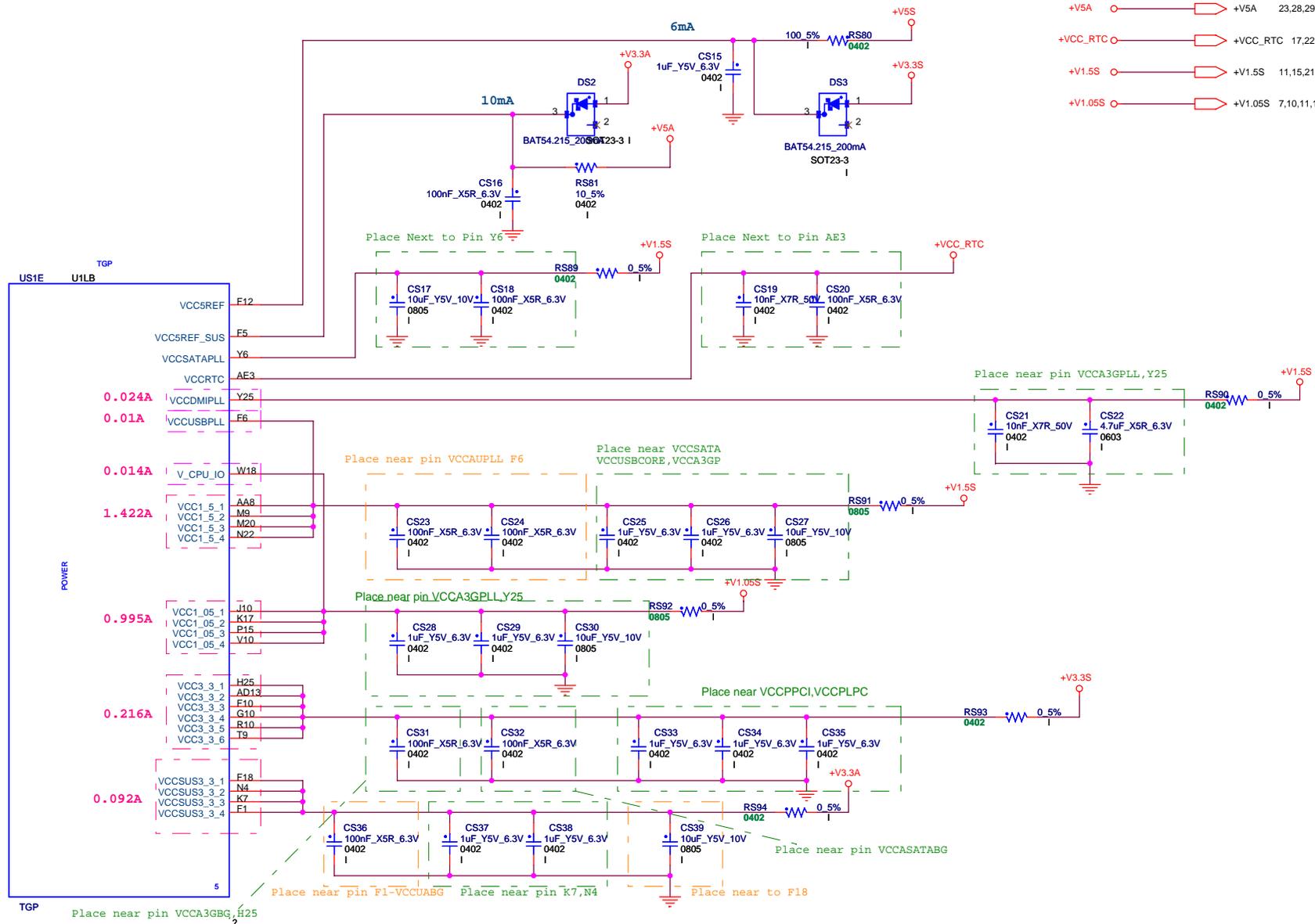
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Foxconn eMS Inc. HNB D R&D
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Title: **TIGERPOINT(LPC AUDIO)3/5**

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- +V5S  +V5S 16,20,23,28,30,31,36,38,39,40
- +V3.3S  +V3.3S 7,9,10,11,14,16,17,20,21,22,23,24,25,26,30,31,34,36,37,38,39,40
- +V3.3A  +V3.3A 15,17,21,22,24,33,34,35,39,40
- +V5A  +V5A 23,28,29,31,34,35,36,37,38,39
- +VCC_RTC  +VCC_RTC 17,22
- +V1.5S  +V1.5S 11,15,21,26,39
- +V1.05S  +V1.05S 7,10,11,13,16,17,36,37,38,39,40

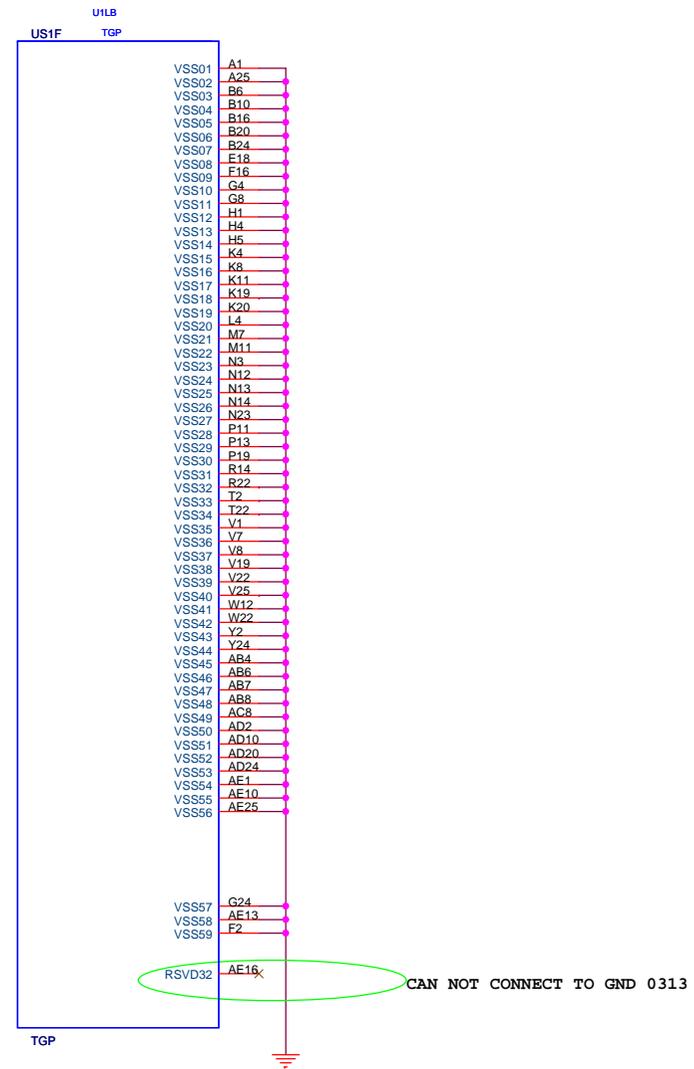


US1E U1LB

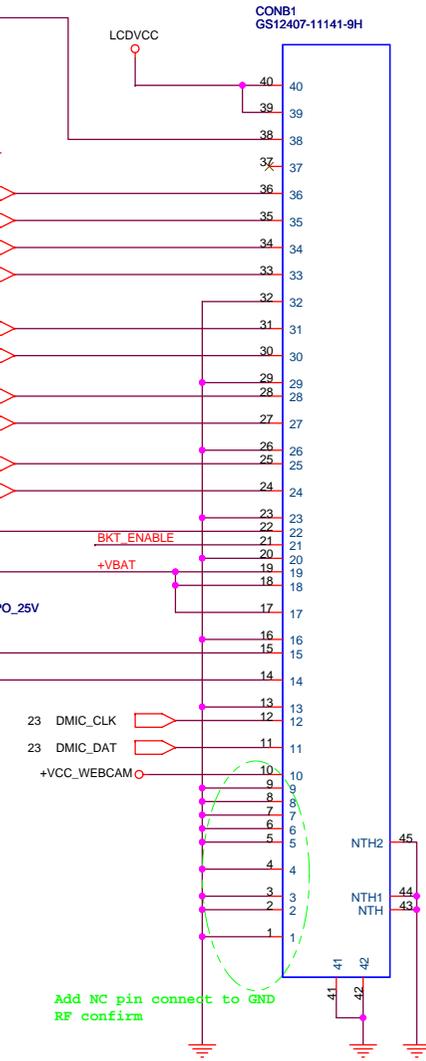
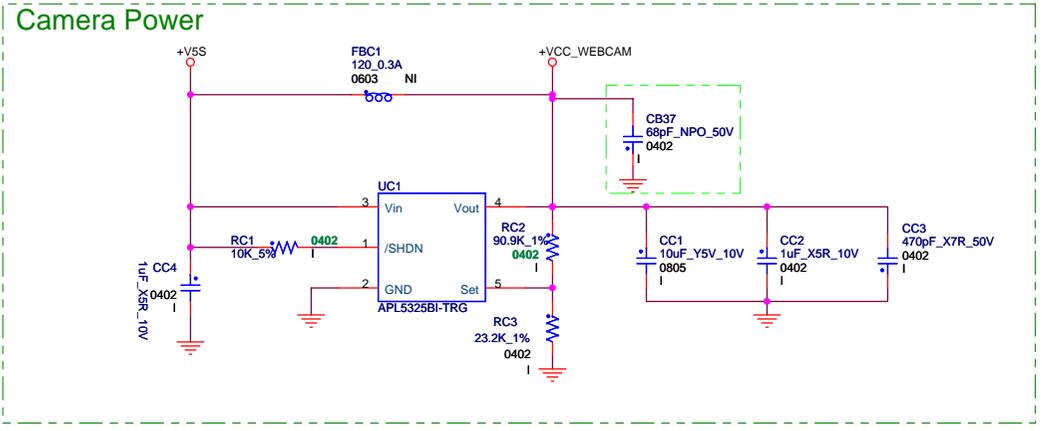
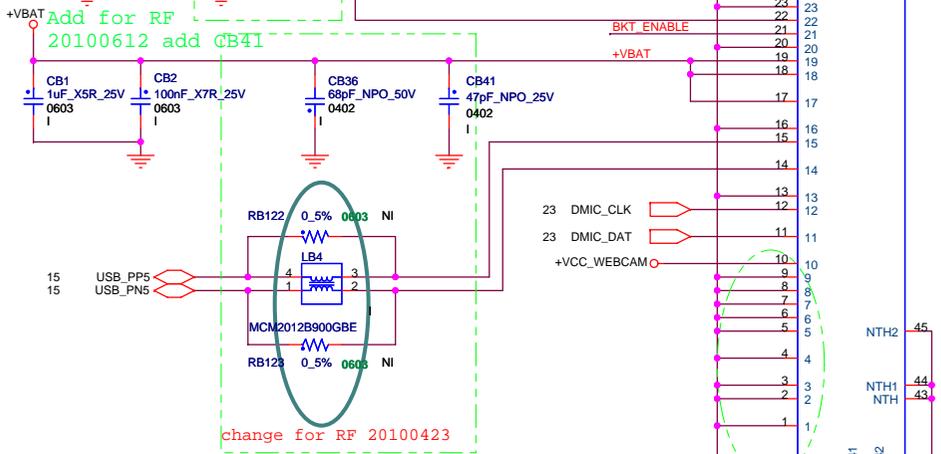
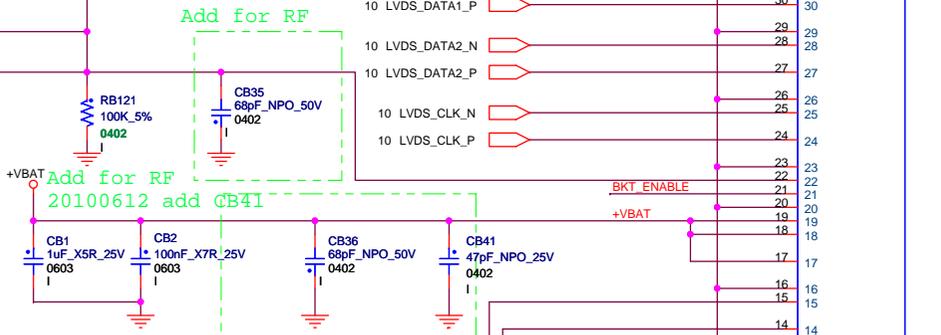
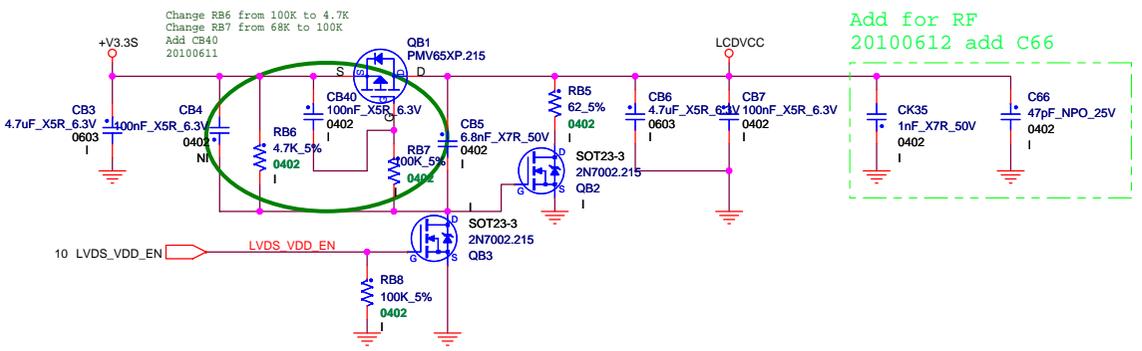
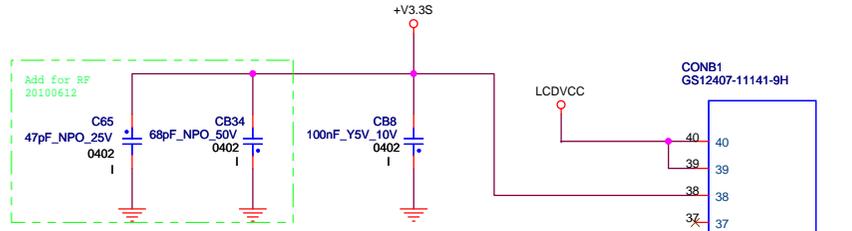
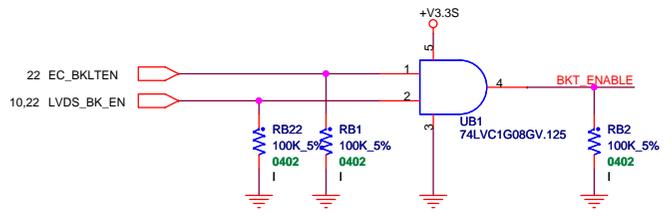
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VCC5REF_SUS	F5
VCCSATAPLL	Y6
VCCRTC	AE3
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0.01A VCCUSBPLL	F6
0.014A V_CPU_IO	W18
1.422A VCC1_5_1	AA8
VCC1_5_2	M9
VCC1_5_3	M20
VCC1_5_4	N22
0.995A VCC1_05_1	J10
VCC1_05_2	K12
VCC1_05_3	P15
VCC1_05_4	V10
0.216A VCC3_3_1	H25
VCC3_3_2	AD13
VCC3_3_3	F10
VCC3_3_4	G10
VCC3_3_5	R10
VCC3_3_6	T9
0.092A VCCSUS3_3_1	F18
VCCSUS3_3_2	N4
VCCSUS3_3_3	K7
VCCSUS3_3_4	F1

TGP Place near pin VCCA3GBG, H25

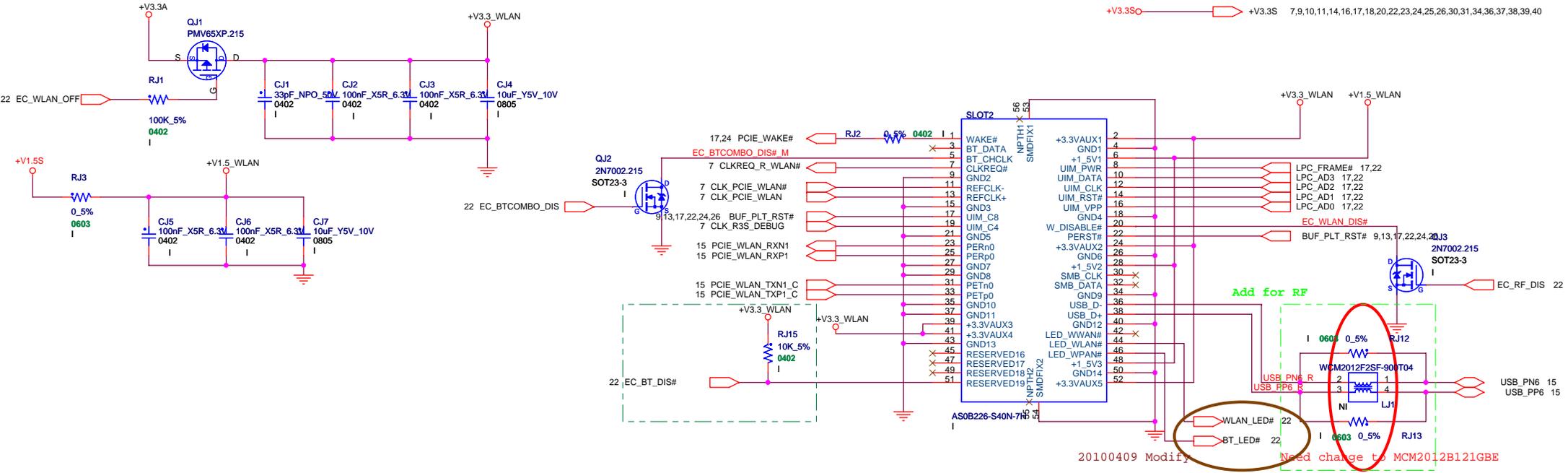
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBND R&D	
		phone: +886-2-2799-6111	
Title: TIGERPOINT(POWER)4/5			
Size	Document Number	Rev	
	Edwards	MV	
Page Modified: Tuesday, October 05, 2010 08:43:36 (UTC/GMT) Sheet 18 of 40			



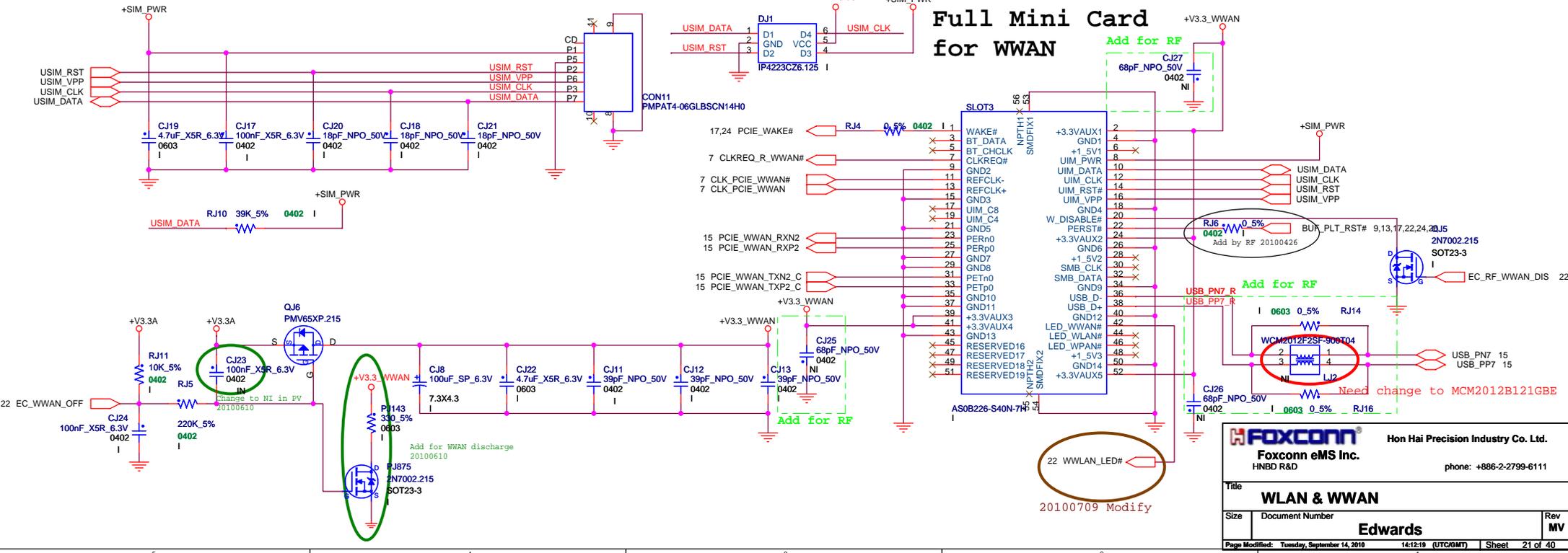
- +VBAT 33,34,35,36,38,40
- +V3.3S 7,9,10,11,14,16,17,18,21,22,23,24,25,26,30,31,34,36,37,38,39,40
- +V5S 16,18,23,28,30,31,36,38,39,40



Half Mini Card for WLAN



Full Mini Card for WWAN



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 HNBd R&D
 Hon Hai Precision Industry Co. Ltd.
 phone: +886-2-2799-6111

Title: **WLAN & WWAN**

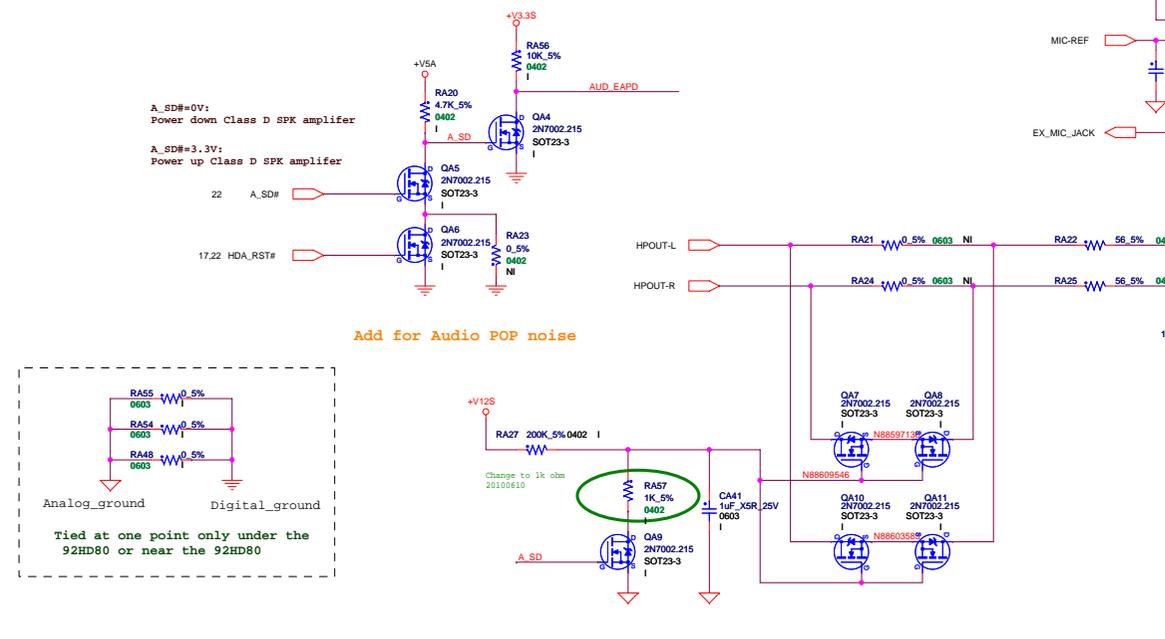
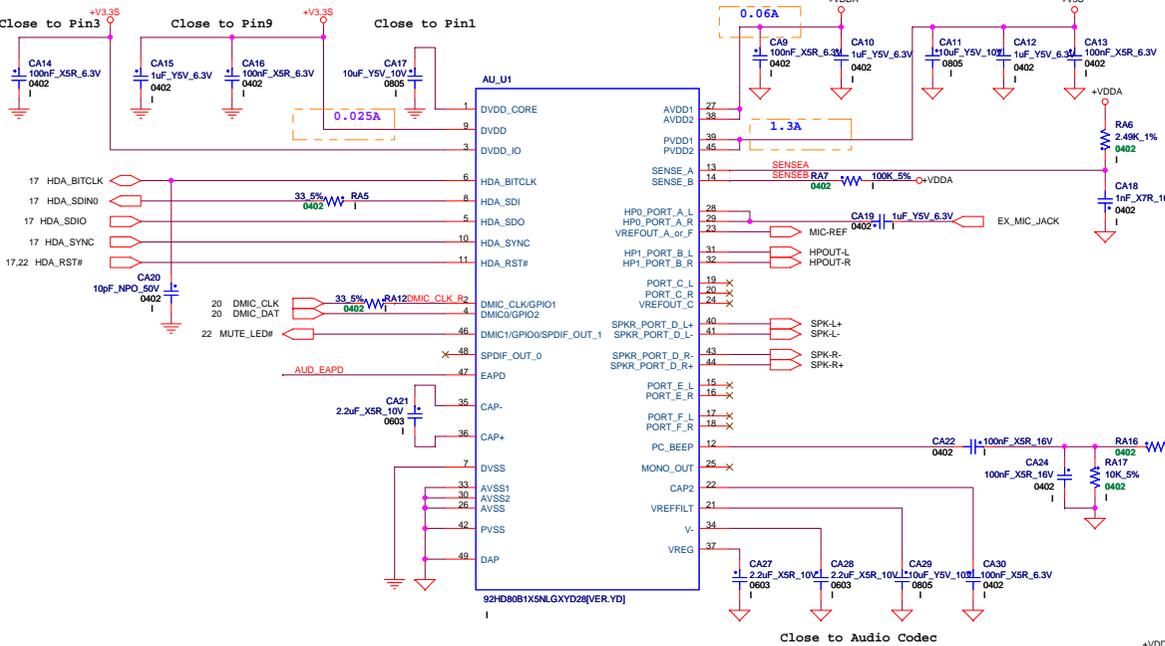
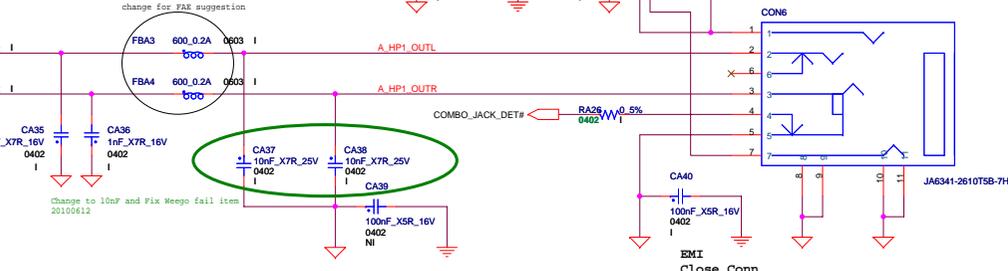
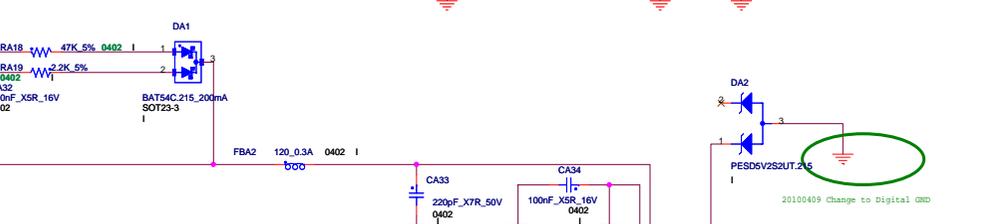
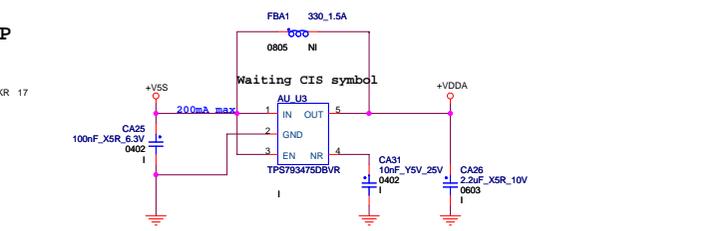
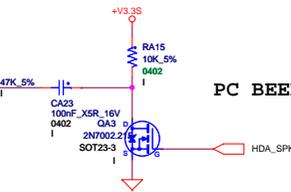
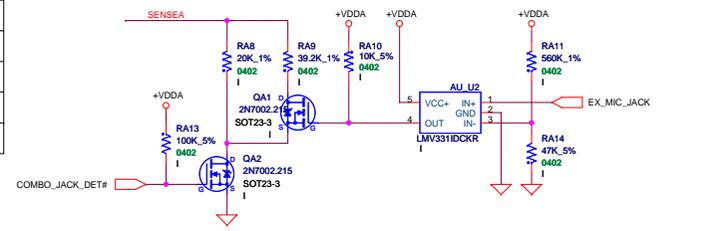
Size: Document Number: **Edwards** Rev: **MV**

Page Modified: Tuesday, September 14, 2010 14:12:19 (UTC/GMT) Sheet 21 of 40

- +V3.3S +V3.3S 7,9,10,11,14,16,17,18,20,21,22,24,25,26,30,31,34,36,37,38,39,40
- +V12S +V12S 39
- +V5S +V5S 16,18,20,28,30,31,36,38,39,40
- +V5A +V5A 18,28,29,31,34,35,36,37,38,39



PORT	Discription	Sense
A	Microphone	SENSE_A
B	Headphone	SENSE_A
C	NO USE	
D	SPKR	
E	NO USE	
F	NO USE	



Analog_ground
Tied at one point only under the 92HD80 or near the 92HD80

Add for Audio POP noise

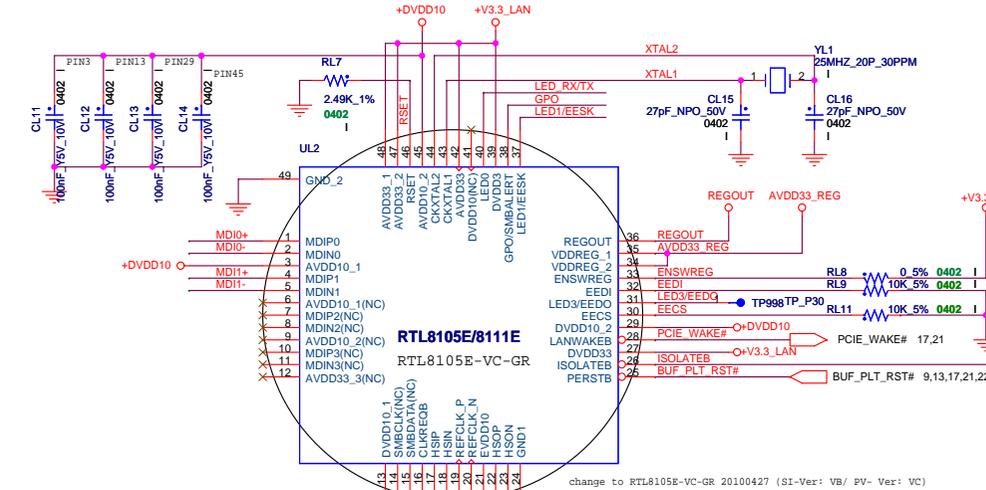
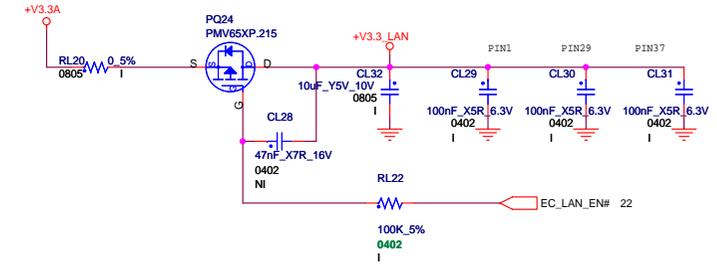
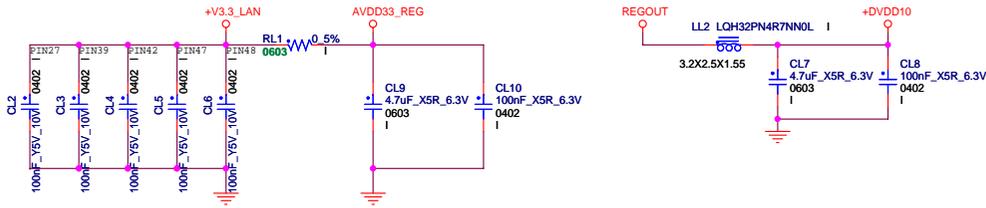
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T80
CODEC/JACK/SPEAKER/MIC

Size Document Number **Edwards** Rev **MV**

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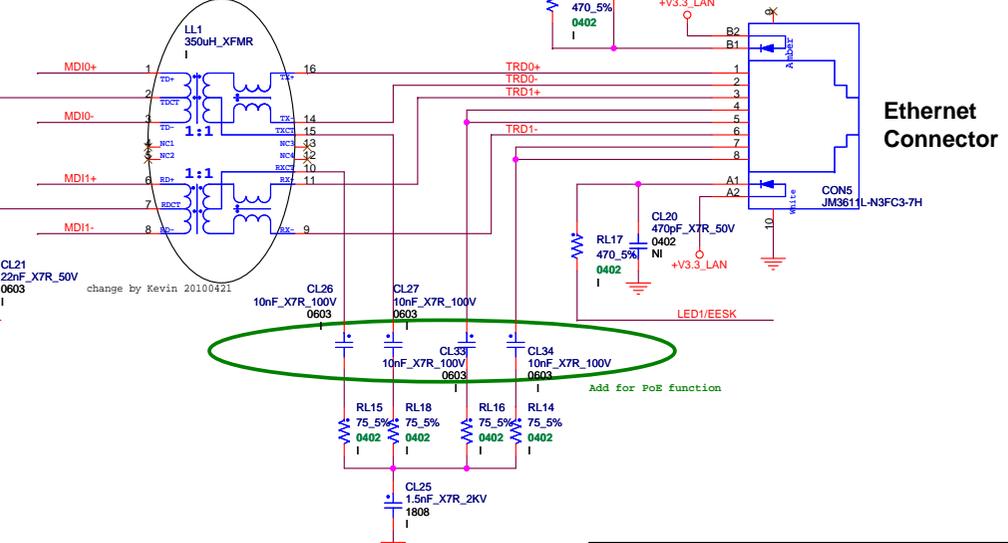
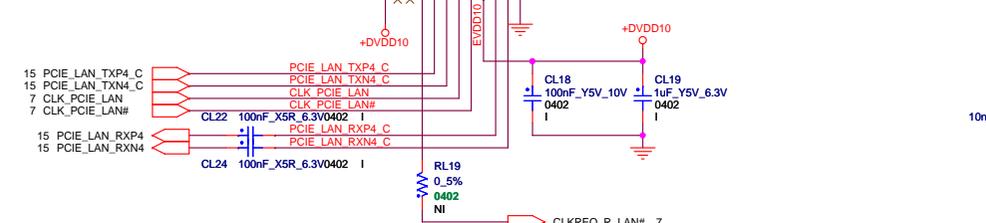
- (1) 4.7uH
- (2) IDC >= 600mA
(if spec has IDC1 and IDC2, the smaller value of IDC should >= 600mA.)
- (3) Tolerance <=20%
- (4) RDC(or DCR) <= 0.8ohms @1Mhz. (Usually its not 1Mhz...anyway, we check the value <=0.8 at any freq.)
- (5) Measure Efficiency >= 75% @ GbE link speed. (Important, u can use demo board to confirm.)



10K ohm close to Host side
GPO RL6 1K 5% 0402
When using EEPROM(93C46A)

White LED for connectivity and
Amber LED for activity located

GND_TR-->GND
for EMI issue

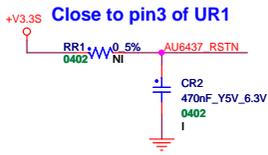


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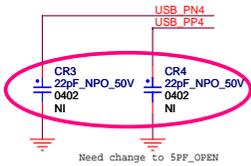
Title: **LAN (RTL8105EL)**

Size	Document Number	Rev
Custom	Edwards	MV

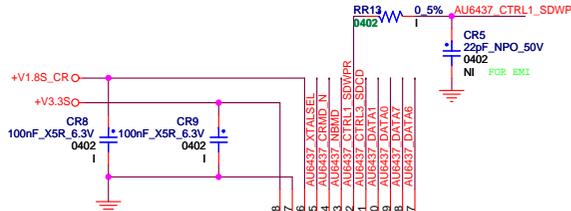
Page Modified: Tuesday, October 05, 2010 08:43:36 (UTC/GMT) Sheet 24 of 40



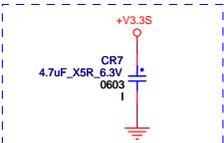
CR3,CR4 Close to CR_U1



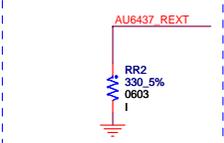
CR_C12 Close to CN3



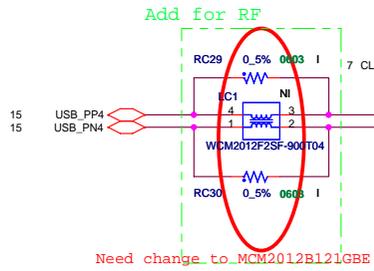
+V3.3S [Symbol] +V3.3S 7,9,10,11,14,16,17,18,20,21,22,23,24,26,30,31,34,36,37,38,39,40



The capacitor CR7 must close between VDD33P (Pin 5) and VS33P (Pin 8) without via.



The capacitor CR10 must close between VDD (Pin 11 & Pin 12) and VS33P (Pin 8) without via. If not, it will cause worse jitter at USB signal.



The capacitor CR11 & CR12 must be close to pin15 & 17

+V3.3S: 30 mils

AU6437_XTALSEL RR5 0.5% 0402 NI

Clock input selection
'1' for 48MHz input [Default]
'0' for 12MHz input

AU6437_SDWPEN RR6 0.5% 0402 NI

SD write protect
'1':decided by SDWP[Default]
'0':letting SD always write-able

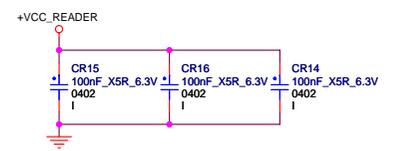
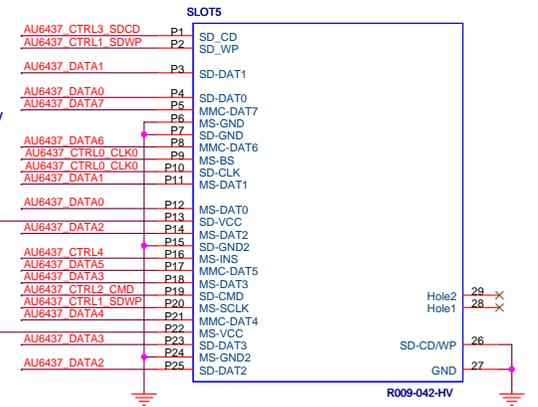
AU6437_GPI2 RR9 0.5% 0402 NI

XD CIS check
'1' for check [Default]
'0' for not check

AU6437_NBMD RR10 0.5% 0402 NI

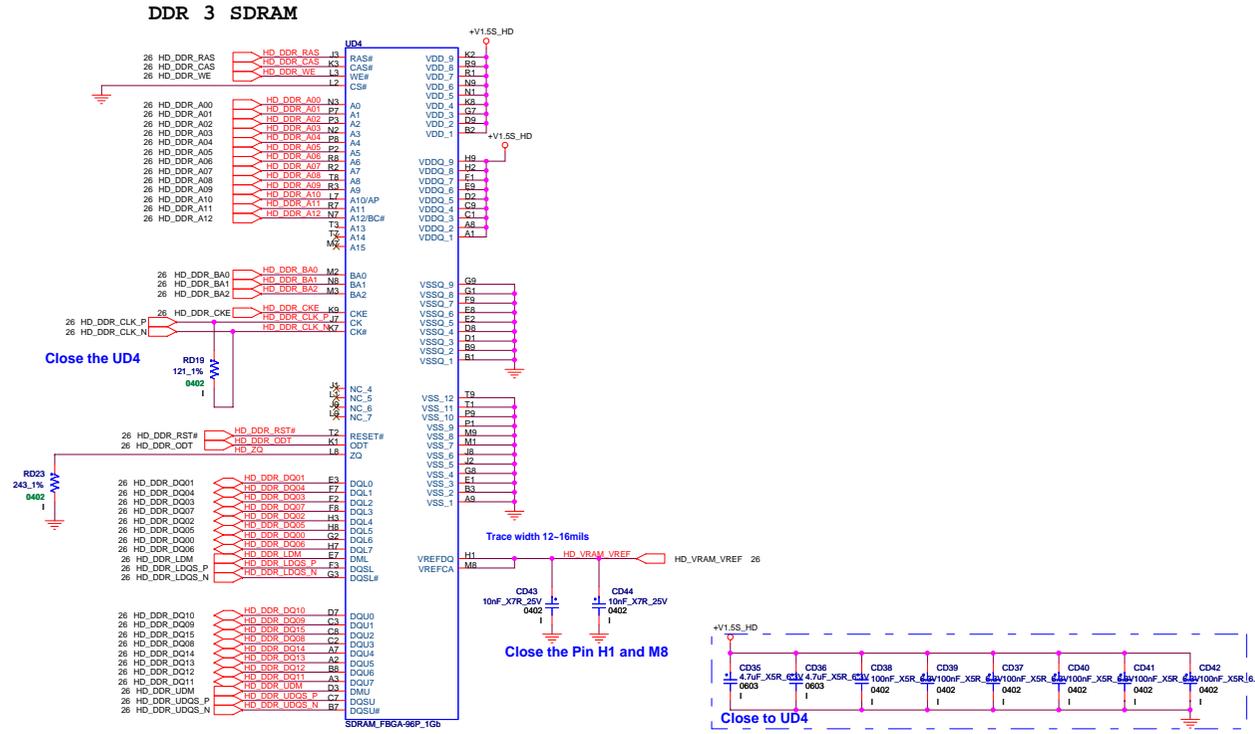
Power saving mode
'1' for enable [Default]
'0' for disable

TP_P30TP980	1	AU6437_GPON7
TP_P30TP981	1	AU6437_XTAL IN
TP_P30TP982	1	AU6437_XTAL OUT
TP_P30TP983	1	AU6437_CTRL4
TP_P30TP984	1	AU6437_XDCDN
TP_P30TP985	1	AU6437_SDWPEN
TP_P30TP988	1	AU6437_DATA4
TP_P30TP994	1	AU6437_DATA6
TP_P30TP995	1	AU6437_DATA7
TP_P30TP996	1	124C04_EEPCLK
TP_P30TP997	1	124C04_EEPPDATA

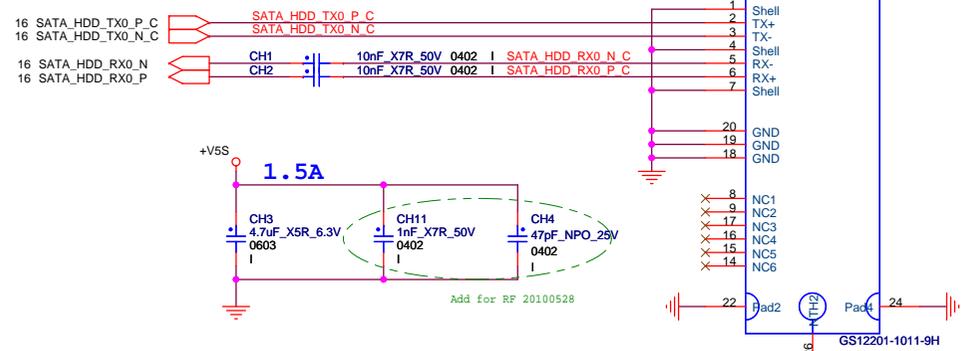


FOXCONN		Hon Hai Precision Industry Co. Ltd.	
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HNBD R&D			
Title			
Card Reader			
Size	Document Number	Rev	MV
Custom	Edwards		
Page Modified: Tuesday, October 05, 2010		88:43:38 (UTC/GMT) Sheet 25 of 40	

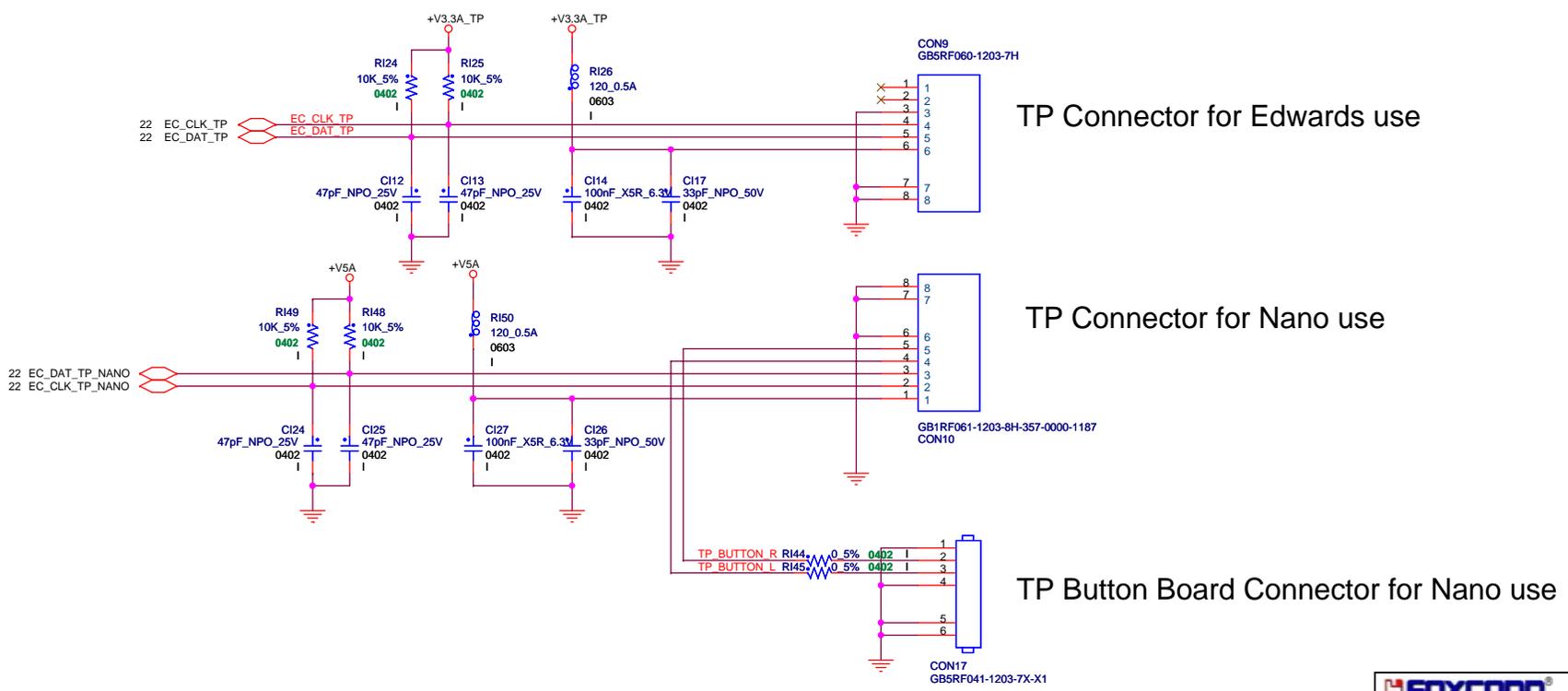
+V1.5S_HD 26



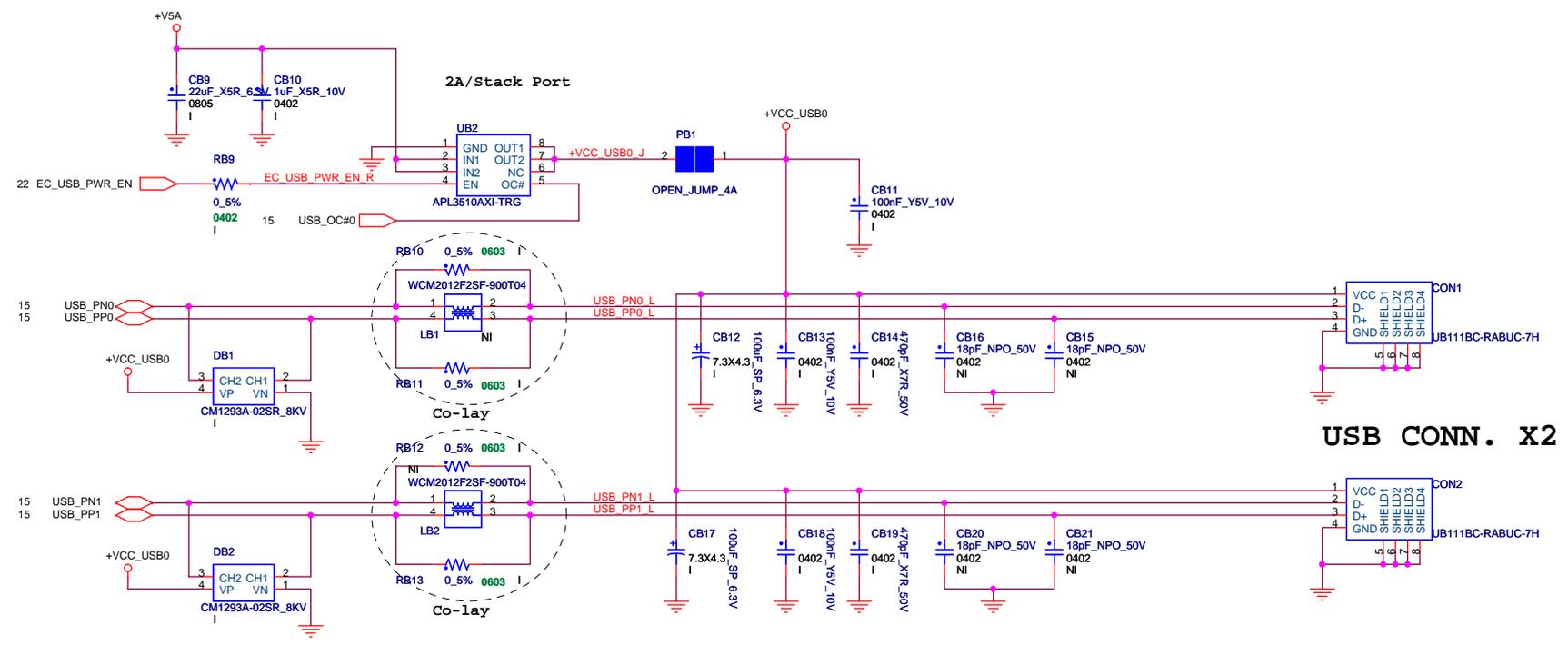
SATA HDD CONN



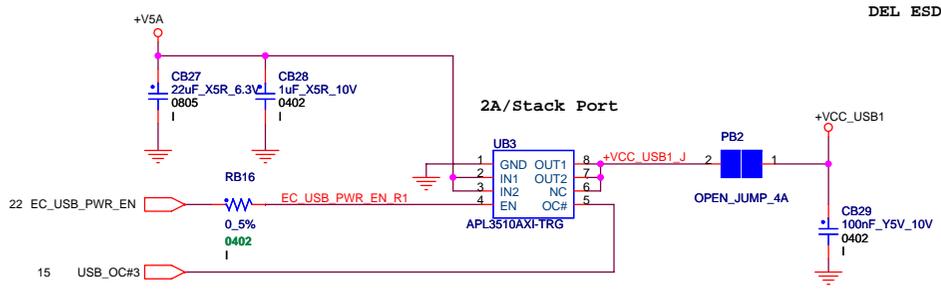
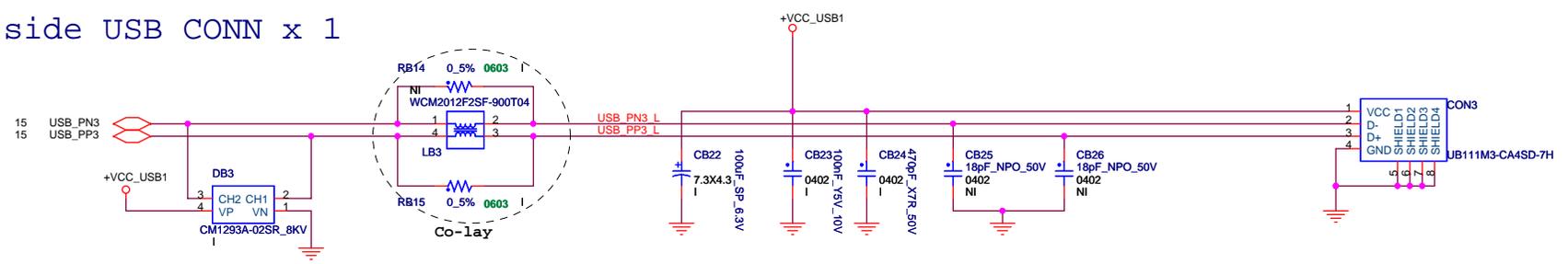
+V5S ○ → +V5S 16,18,20,23,30,31,36,38,39,40



Right side USB CONN x2



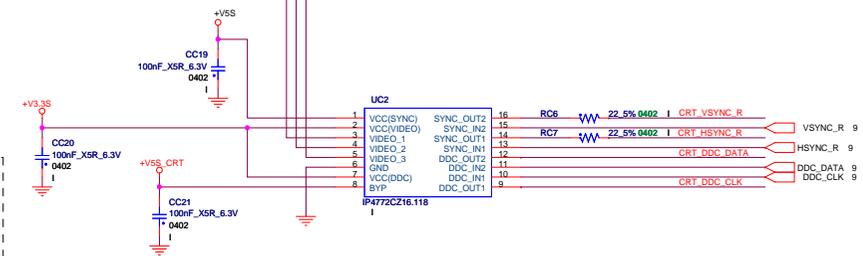
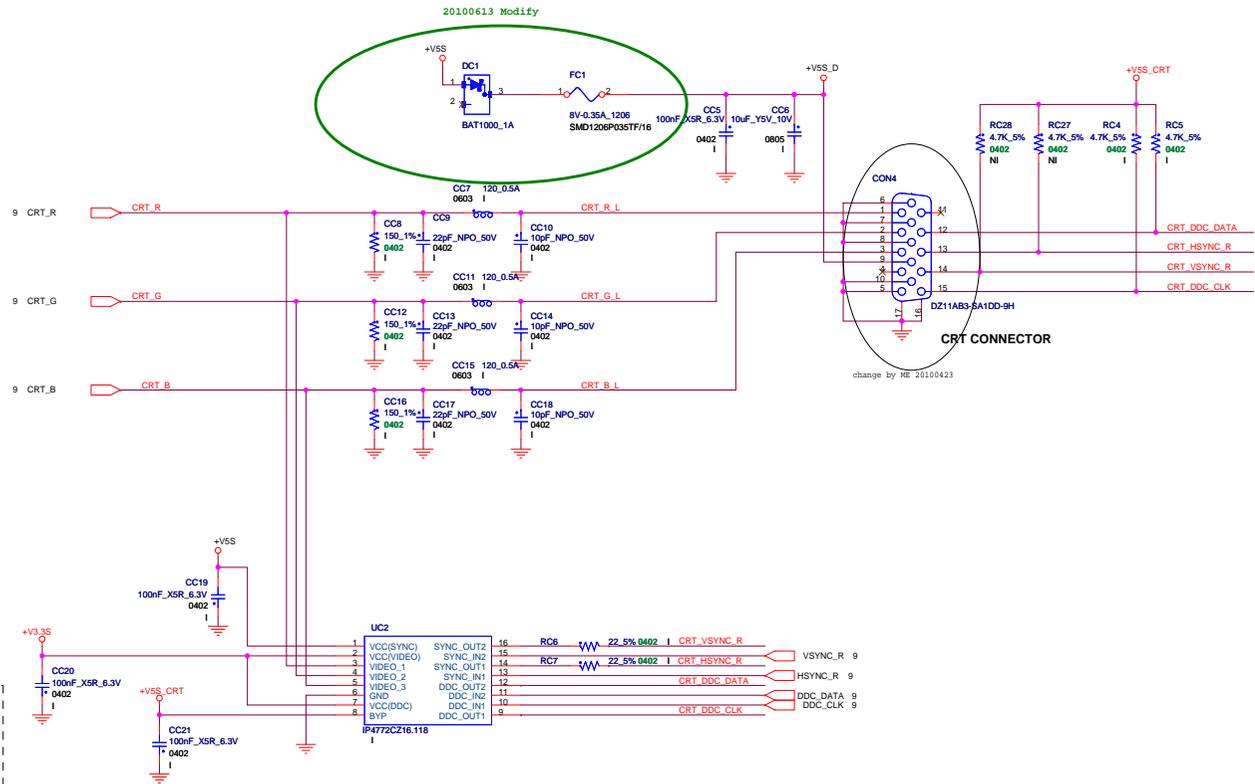
Left side USB CONN x 1



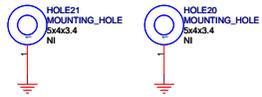
DEL ESD SOLUTION 0312

		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNB D R&D	
		phone: +886-2-2799-6111	
Title: USB PORT X 3			
Size: A3	Document Number: Edwards	Rev: MV	
Page Modified: Tuesday, September 14, 2010		14:12:19 (UTC/GMT) Sheet 29 of 40	

+V3.3SO → +V3.3S 7,9,10,11,14,16,17,18,20,21,22,23,24,25,26,31,34,36,37,38,39,40
 +VSS → +VSS 16,18,20,23,28,31,36,38,39,40



CPU Hole



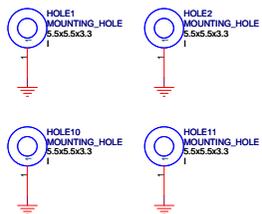
EMI SPRING



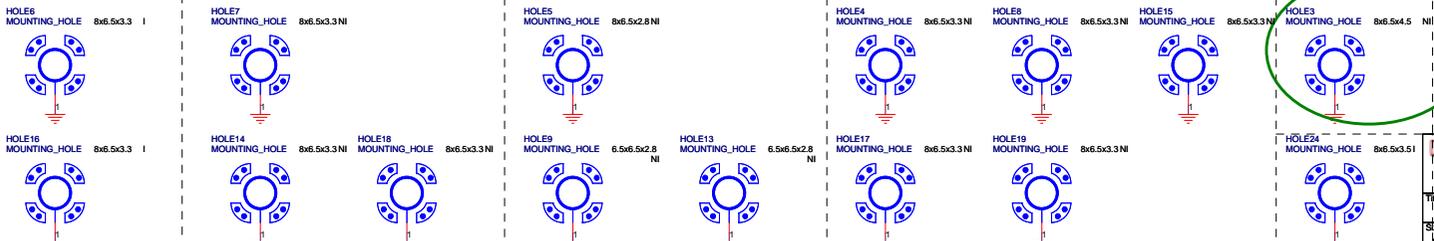
add for RF 20100423

Top x Bottom x Hole(mm) change screw pad by kevin 20100421

Mini Card Hole



FAN Hole



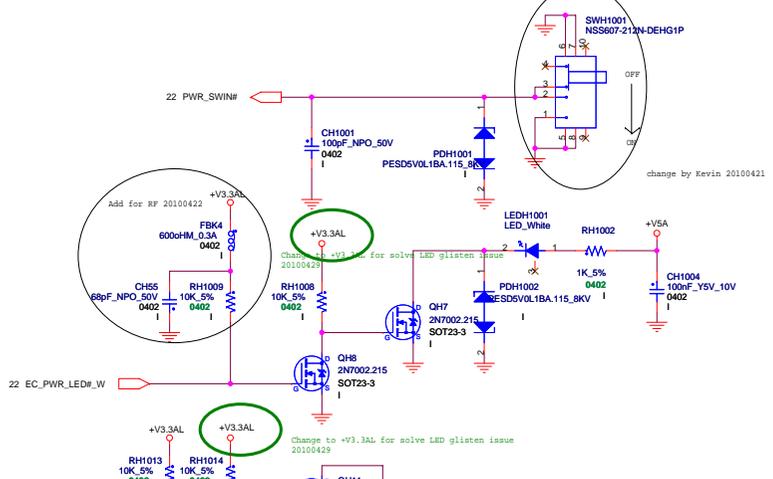
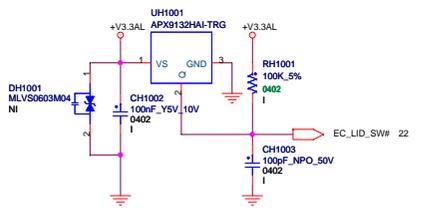
20100530 change for ME

		Hon Hai Precision Industry Co. Ltd. HNB0 R&D phone: +886-2-2799-6111	
CRT			
Type	Document Number	Rev	MV
Size	Custom	Edwards	
Page Modified: Tuesday, September 14, 2010 14:18:19 (UTC+08:00) Sheet 30 of 40			

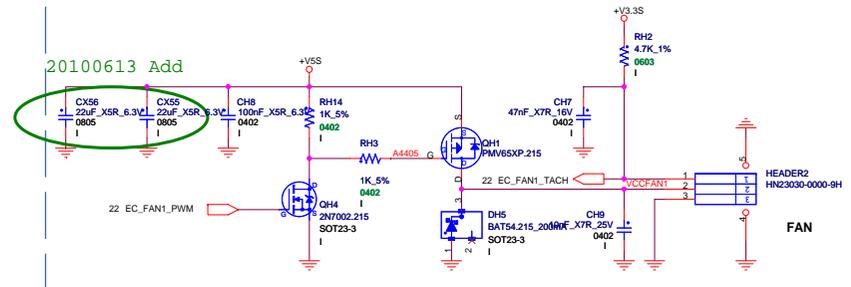
Power Switch and Power LED

- +V3.3A → +V3.3AL 17,22,32,34
- +V5A → +V5A 18,23,28,29,34,35,36,37,38,39
- +V3.3S → +V3.3S 7,9,10,11,14,16,17,18,20,21,22,23,24,25,26,30,34,36,37,38,39,40
- +V5S → +V5S 16,18,20,23,28,30,36,38,39,40

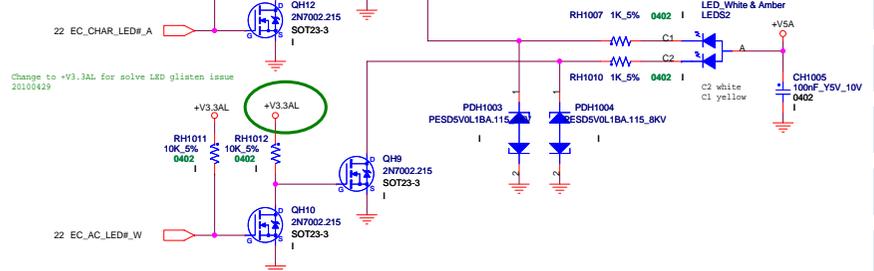
LID Switch



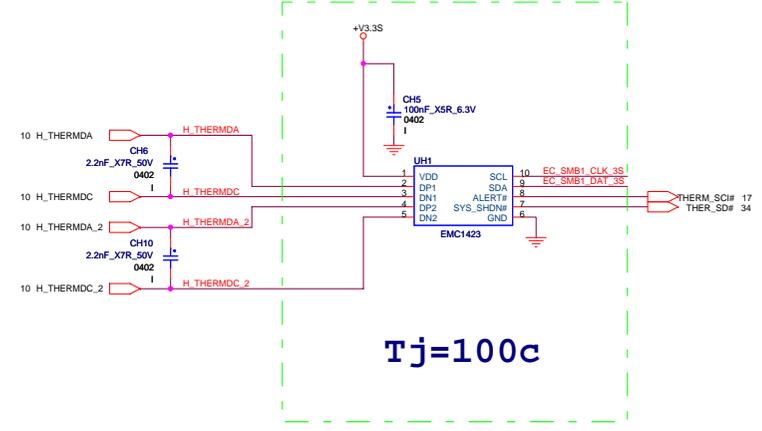
FAN CONNECTOR



AC Plug LED

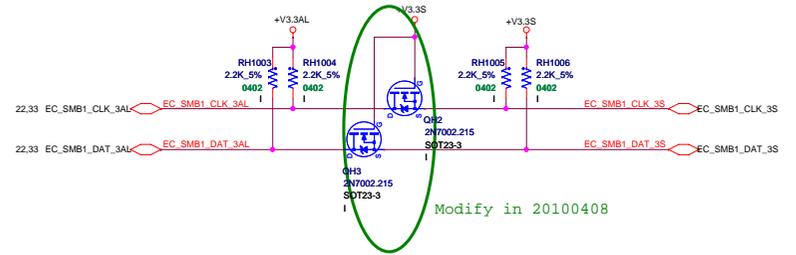


Add for Dual Core use



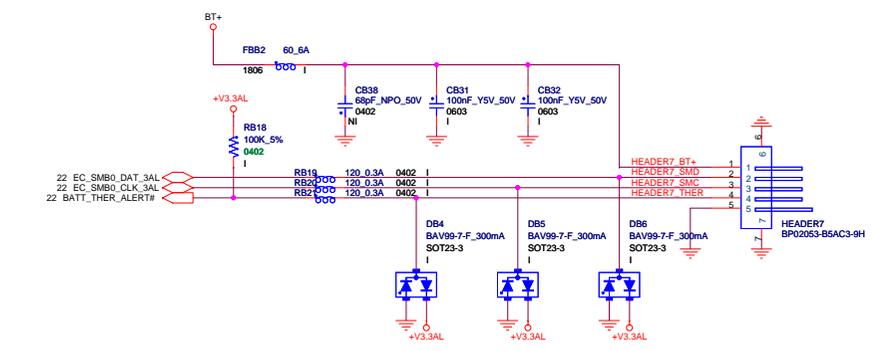
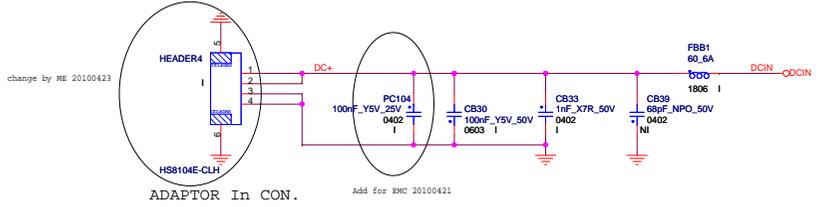
Tj=100c

THERMAL SENSOR

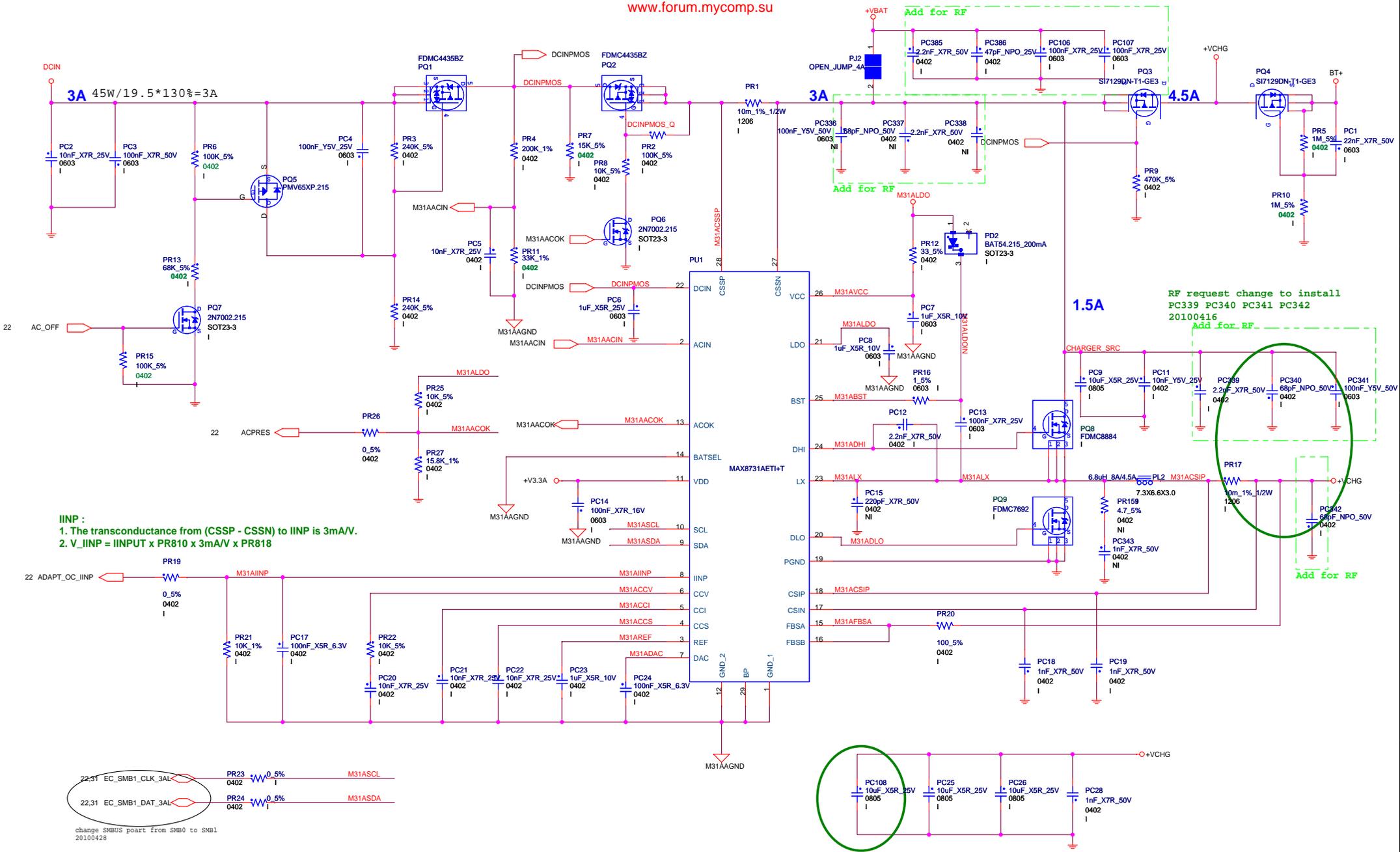


Modify in 20100408

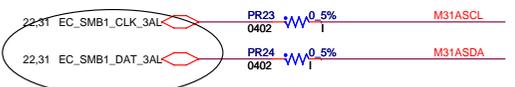
DC JACK Wire to Board Connector



BATTERY CONNECTOR



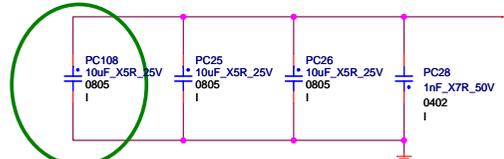
IINP :
 1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
 2. $V_{IINP} = IINP_{INPUT} \times PR810 \times 3mA/V \times PR818$



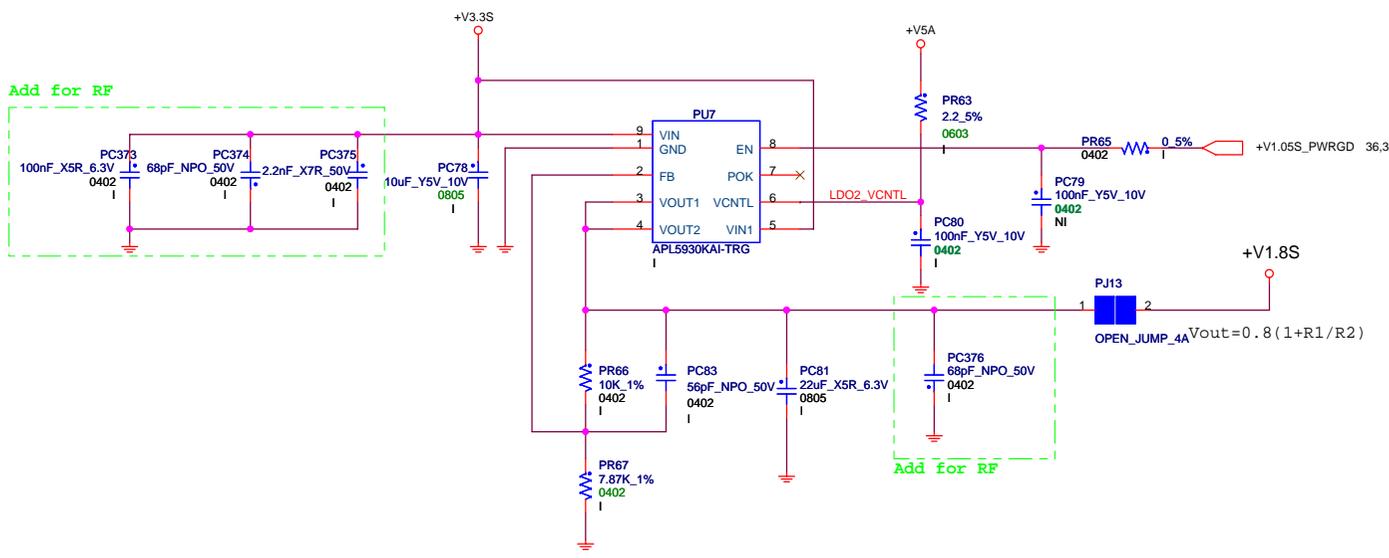
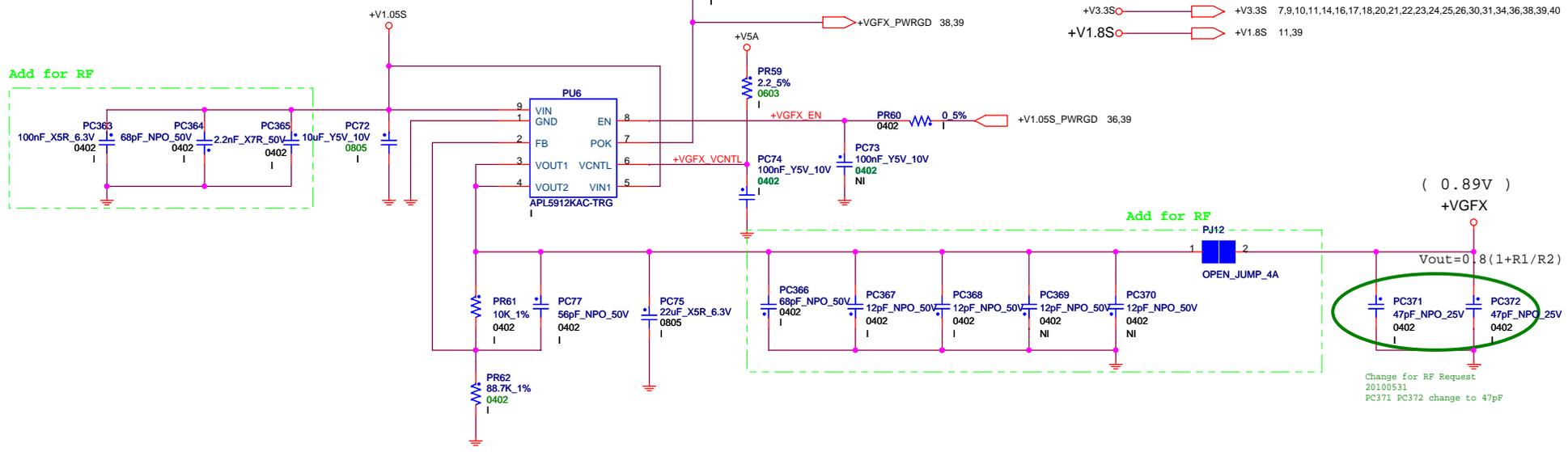
change SMBUS poart from SMB0 to SMB1
 20100428



Change for Acoustic by Kevin
 20100710



		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D	
Title PWR_Charger MAX8731AETI		phone: +886-2-2798-6111	
Size	Document Number	Rev	
Custom	Edwards	MV	
Page Modified: Tuesday, September 14, 2010 14:12:19 (UTC/GMT)		Sheet	33 of 40

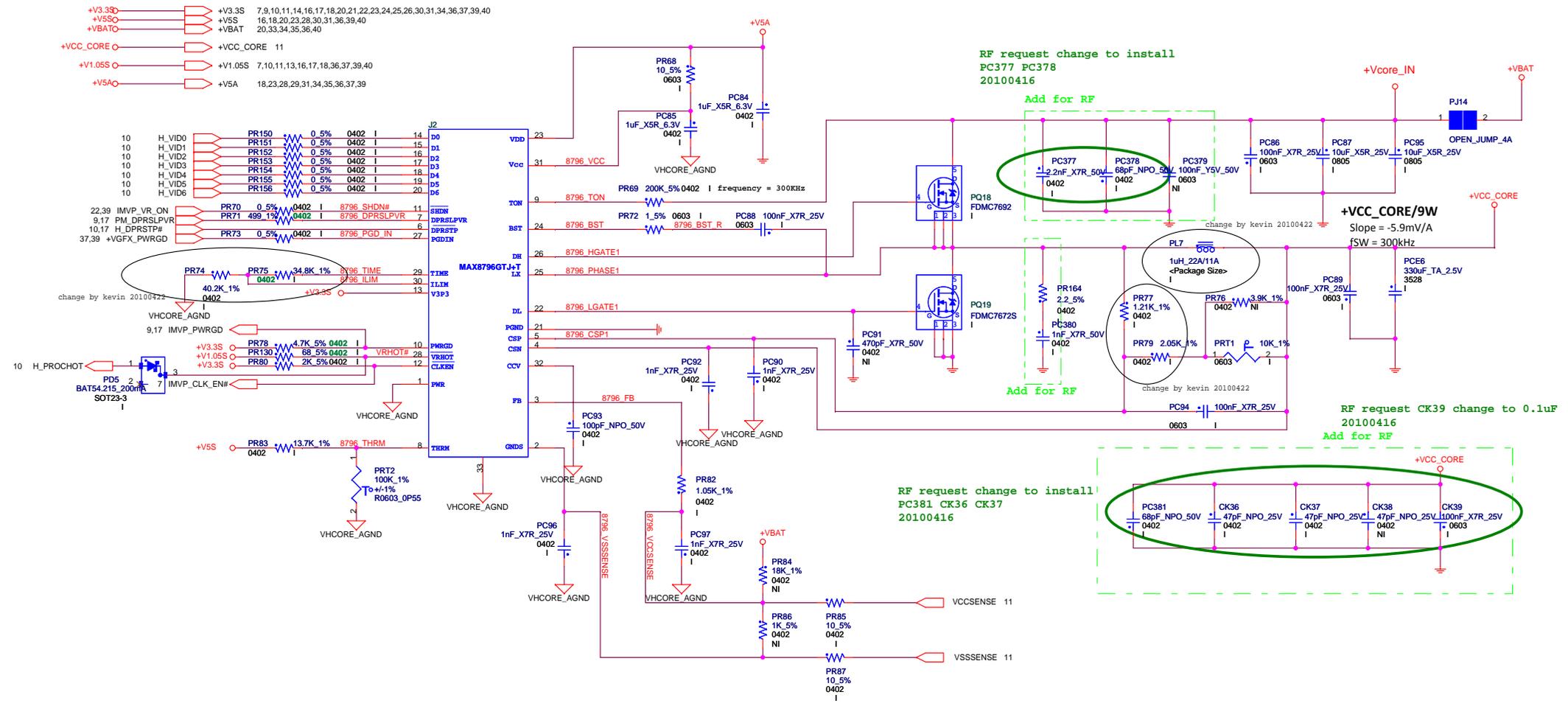


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Title: **+VGFX & +V1.8S**

Size	Document Number	Rev
Custom	Edwards	MV

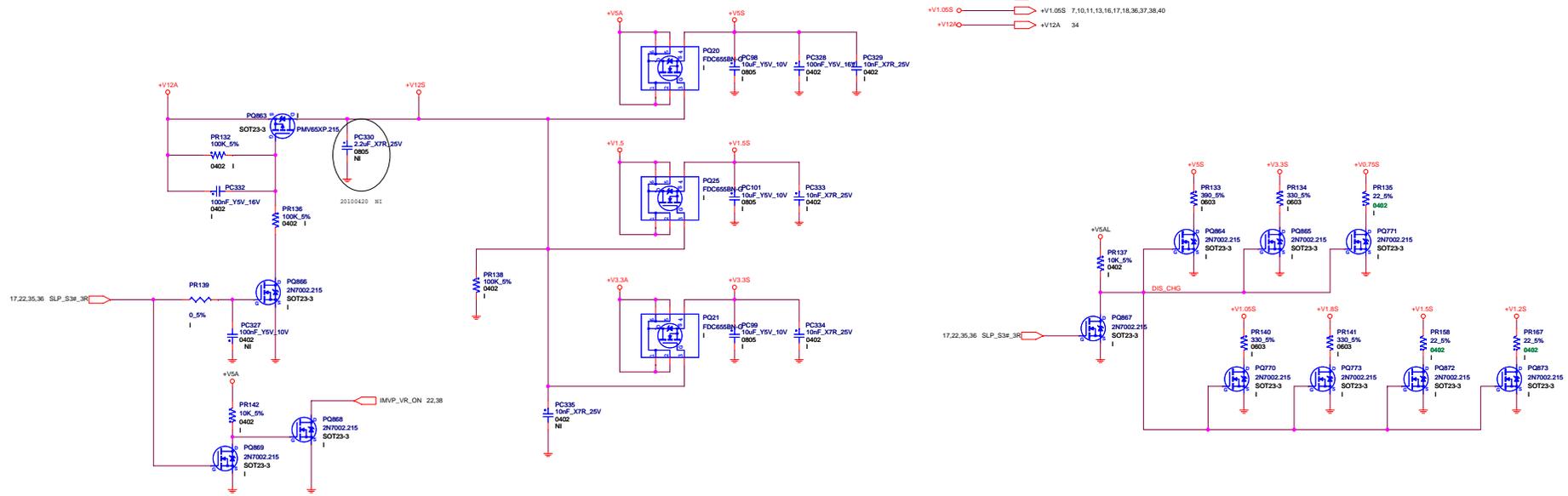
Page Modified: Tuesday, September 14, 2010 14:12:19 (UTC+GMT) Sheet 37 of 40



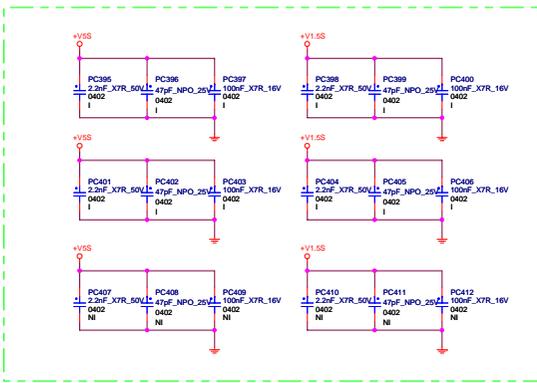
FOXCONN		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
Title		VCCORE MAX8796	
Size	Document Number	Rev	MV
Custom	Edwards		
Page Modified: Friday, October 08, 2010		15:18:47 (UTC/GMT) Sheet 38 of 40	



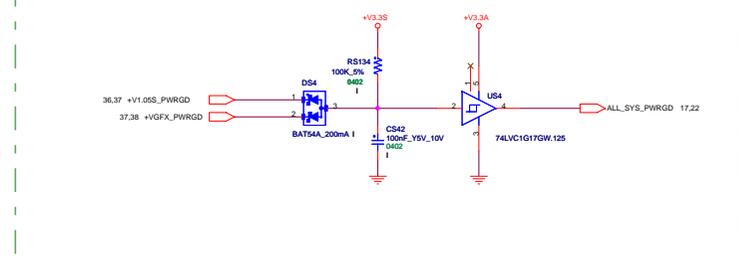
- +V12S 23
- +VSAL 34
- +VSA 18,23,28,29,31,34,35,36,37,38
- +VSS 16,18,20,23,28,30,31,36,38,40
- +V1.5 8,11,14,35,36
- +V1.550 11,15,18,21,26
- +V3.3A 15,17,18,21,22,24,33,34,35,40
- +V3.3SD 7,9,10,11,14,16,17,18,20,21,22,23,24,25,26,30,31,34,36,37,38,40
- +V0.75S 14,35
- +V1.8S 11,37
- +V1.05S 7,10,11,13,16,17,18,36,37,38,40
- +V12A 34



Add for RF 20100709



System Power Good



- +V3.3Q +V3.3S 7,9,10,11,14,16,17,18,20,21,22,23,24,25,26,30,31,34,36,37,38,39
- +V3.3A +V3.3A 15,17,18,21,22,24,33,34,35,39
- +VSS +VSS 16,18,20,23,28,30,31,36,38,39
- +V5A +V5A 18,23,28,29,31,34,35,36,37,38,39
- +VBATO +VBAT 20,33,34,35,36,38
- +V1.05S +V1.05S 7,10,11,13,16,17,18,36,37,38,39

For EMI Decoupling and All 47pF Caps are all RF Request

For RF Decoupling
All 47pF are RF Request in SI-Small build phase

