

Designer's™ Data Sheet
SWITCHMODE Series
NPN Silicon Power Transistors

The BUS98 and BUS98A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

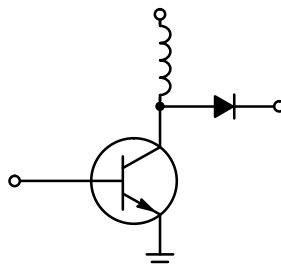
Fast Turn-Off Times

- 60 ns Inductive Fall Time –25°C (Typ)
- 120 ns Inductive Crossover Time –25°C (Typ)

Operating Temperature Range –65 to +200°C

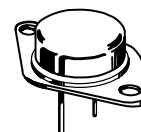
100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)



BUS98
BUS98A

30 AMPERES
NPN SILICON
POWER TRANSISTORS
400 AND 450 VOLTS
(BVCEO)
250 WATTS
850–1000 V (BVCEs)



CASE 1-07
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	BUS98	BUS98A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous	I_C	30		Adc
— Peak (1)	I_{CM}	60		
— Overload	I_{ol}	120		
Base Current — Continuous	I_B	10		Adc
— Peak (1)	I_{BM}	30		
Total Power Dissipation — $T_C = 25^\circ C$	P_D	250		Watts
— $T_C = 100^\circ C$		142		
Derate above 25°C		1.42		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 7

BUS98 BUS98A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (Table 1) (I _C = 200 mA, I _B = 0) L = 25 mH	BUS98 BUS98A	V _{CEO(sus)}	400 450	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 125°C)		I _{CEV}	— —	— —	0.4 4.0	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 10 Ω)	T _C = 25 °C T _C = 125 °C	I _{CER}	— —	— —	1.0 6.0	mAdc
Emitter Cutoff Current (V _{EB} = 7 Vdc, I _C = 0)		I _{EBO}	—	—	0.2	mAdc
Emitter–Base Breakdown Voltage (I _E = 100 mA – I _C = 0)		V _{EBO}	7.0	—	—	Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}		See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 20 Adc, V _{CE} = 5 Vdc) (I _C = 16 Adc, V _{CE} = 5 V)	BUS98 BUS98A	h _{FE}	8	—	—	—
Collector–Emitter Saturation Voltage (I _C = 20 Adc, I _B = 4 Adc) (I _C = 30 Adc, I _B = 8 Adc) (I _C = 20 Adc, I _B = 4 Adc, T _C = 100°C) (I _C = 16 Adc, I _B = 3.2 Adc) (I _C = 24 Adc, I _B = 5 Adc) (I _C = 16 Adc, I _B = 3.2 Adc, T _C = 100°C)	BUS98 BUS98A	V _{CE(sat)}	— — — — — —	— — — — — —	1.5 3.5 2.0 1.5 5.0 2.0	Vdc
Base–Emitter Saturation Voltage (I _C = 20 Adc, I _B = 4 Adc) (I _C = 20 Adc, I _B = 4 Adc, T _C = 100°C) (I _C = 16 Adc, I _B = 3.2 Adc) (I _C = 16 Adc, I _B = 3.2 Adc, T _C = 100°C)	BUS98 BUS98A	V _{BE(sat)}	— — — —	— — — —	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 100 kHz)	C _{ob}	—	—	700	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	(V _{CC} = 250 Vdc, I _C = 20 A, I _{B1} = 4.0 A, t _p = 30 μs, Duty Cycle ≤ 2%, V _{BE(off)} = 5 V) (for BUS98A: I _C = 16 A, I _{B1} = 3.2 A)	t _d	—	0.1	0.2	μs
Rise Time		t _r	—	0.4	0.7	
Storage Time		t _s	—	1.55	2.3	
Fall Time		t _f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	I _{C(pk)} = 20 A (BUS98) I _{B1} = 4 A V _{BE(off)} = 5 V, V _{CE(c1)} = 250 V	(T _C = 25°C)	t _{sv}	—	1.55	—	μs
Fall Time			t _{fi}	—	0.06	—	
Storage Time	I _{C(pk)} = 16 A (BUS98A) I _{B1} = 3.2 A	(T _C = 100°C)	t _{sv}	—	1.8	2.8	
Crossover Time			t _c	—	0.3	0.6	
Fall Time			t _{fi}	—	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

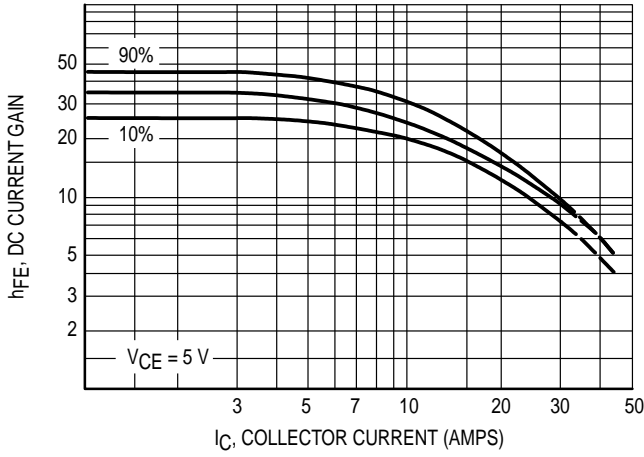


Figure 1. DC Current Gain

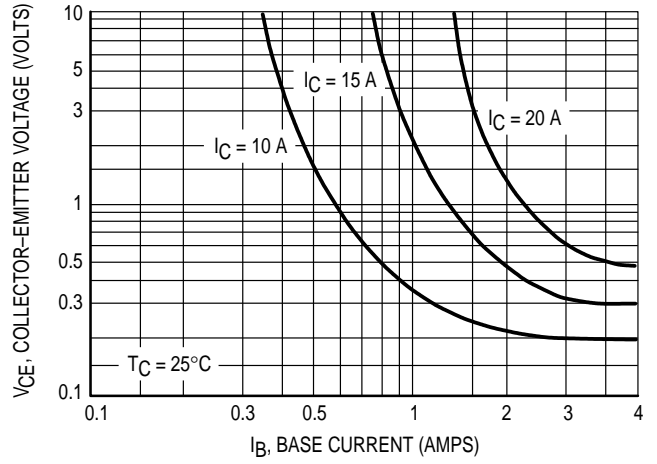


Figure 2. Collector Saturation Region

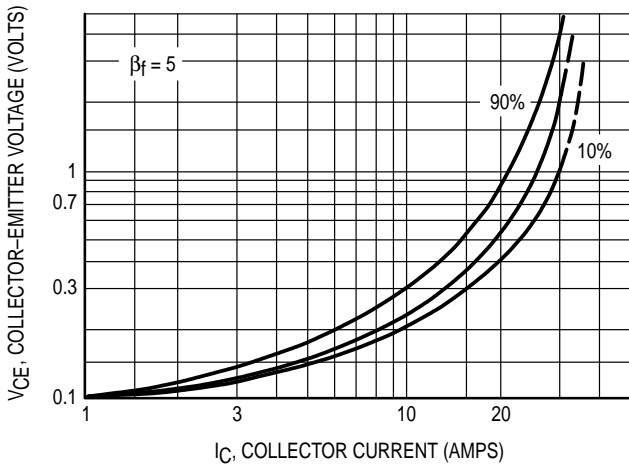


Figure 3. Collector-Emitter Saturation Voltage

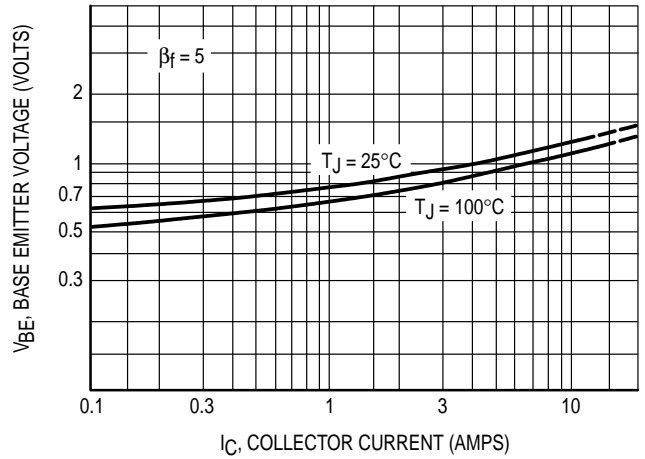


Figure 4. Base-Emitter Voltage

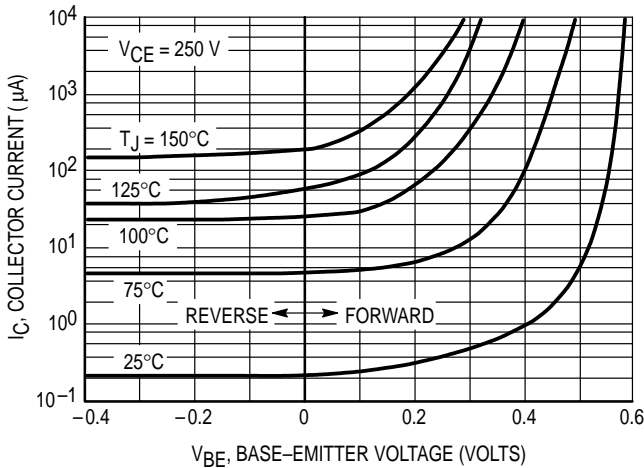


Figure 5. Collector Cutoff Region

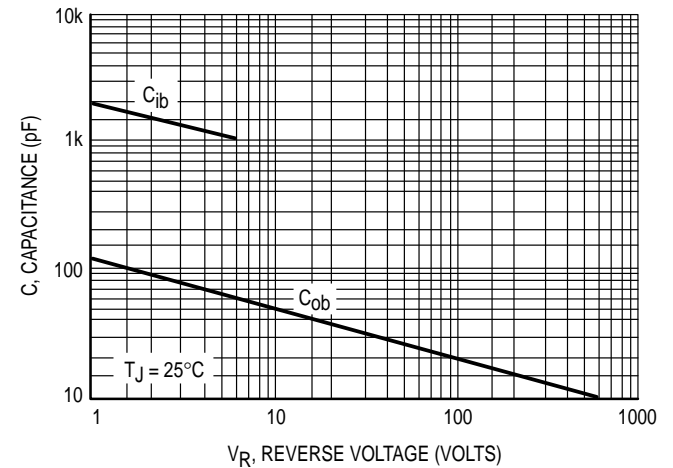
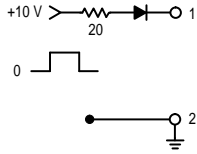
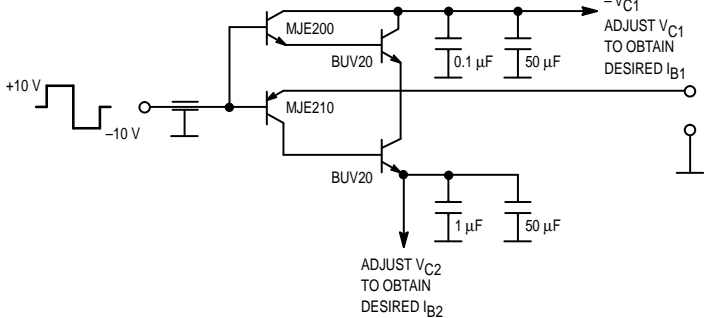
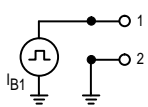
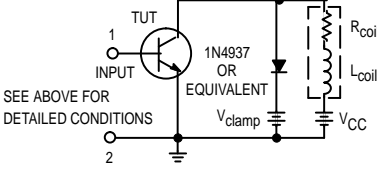
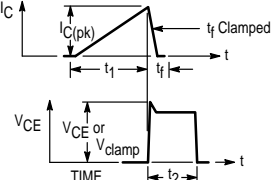
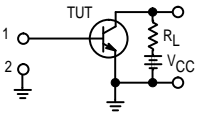


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>		<p>TURN-ON TIME</p>  <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 25 mH, V _{CC} = 10 V R _{coil} = 0.7 Ω	L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V V _{clamp} = 250 V	V _{CC} = 250 V Pulse Width = 10 μs
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> 	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{\text{coil}} (I_C(\text{pk}))}{V_{CC}}$ $t_2 \approx \frac{L_{\text{coil}} (I_C(\text{pk}))}{V_{\text{clamp}}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

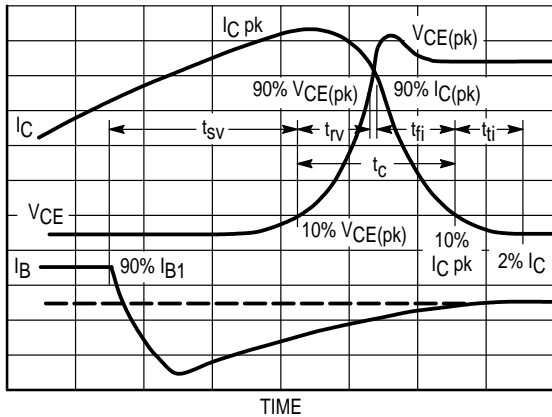


Figure 7. Inductive Switching Measurements

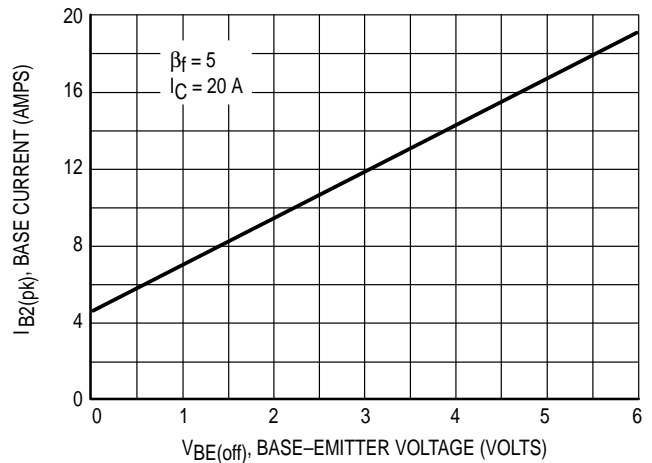


Figure 8. Peak-Reverse Current

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{RV} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_C = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is

shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_C) f$$

In general, $t_{RV} + t_{fi} \approx t_C$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

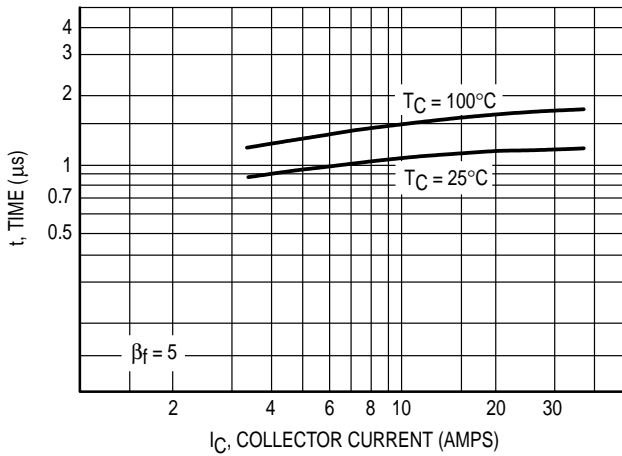


Figure 9. Storage Time, t_{SV}

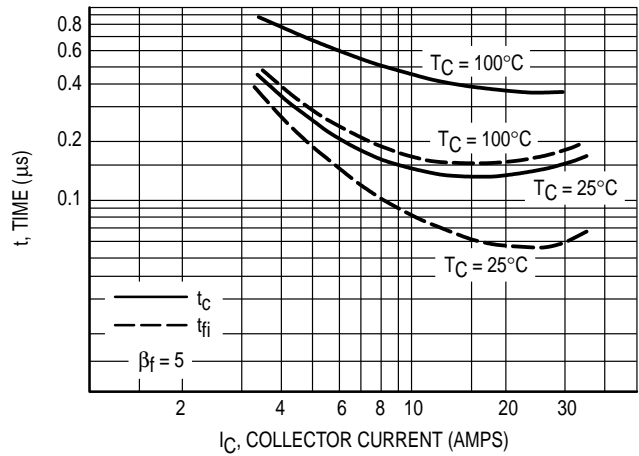


Figure 10. Crossover and Fall Times

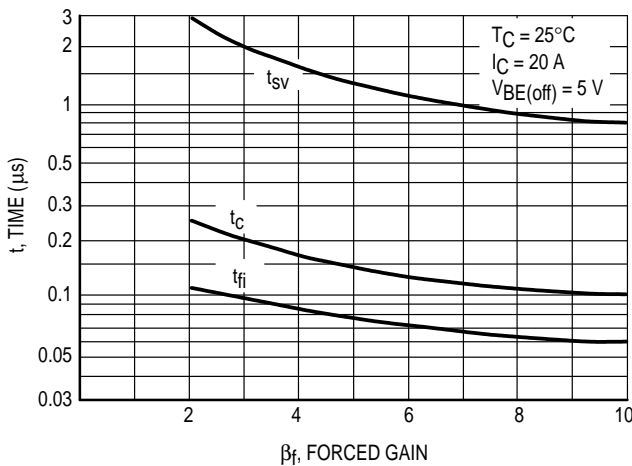


Figure 11a. Turn-Off Times versus Forced Gain

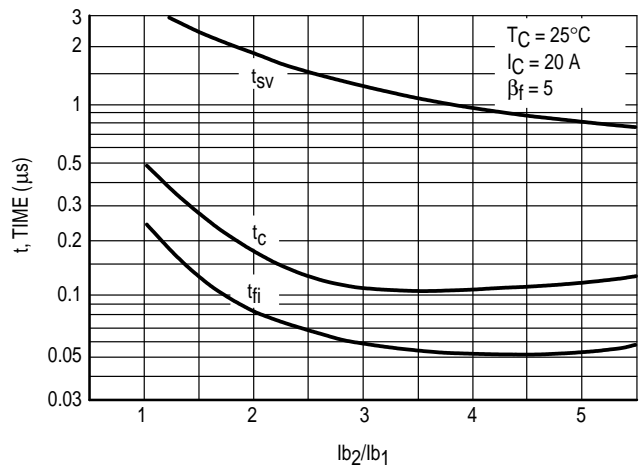


Figure 11b. Turn-Off TM Times versus I_{b2}/I_{b1}

BUS98 BUS98A

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

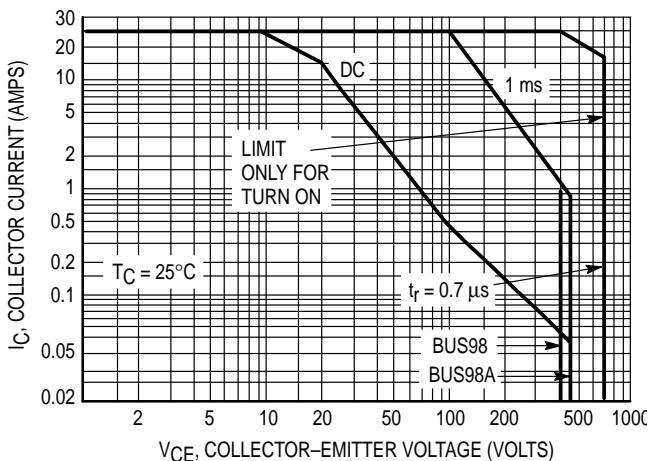


Figure 12. Forward Bias Safe Operating Area

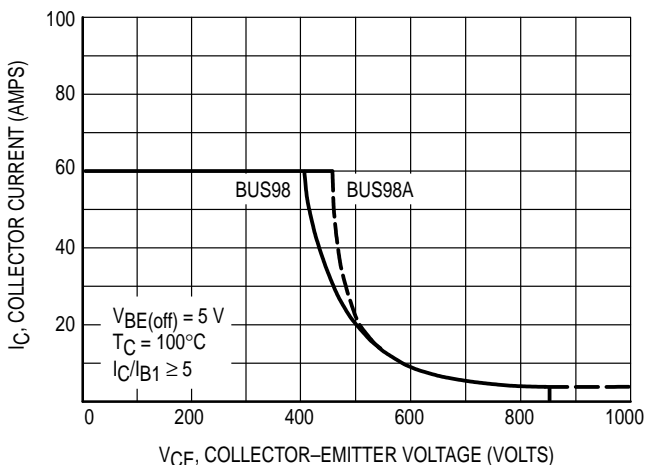


Figure 13. Reverse Bias Safe Operating Area

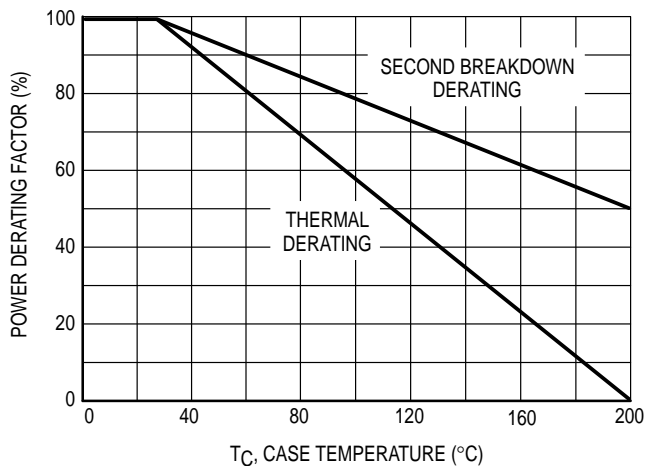


Figure 14. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

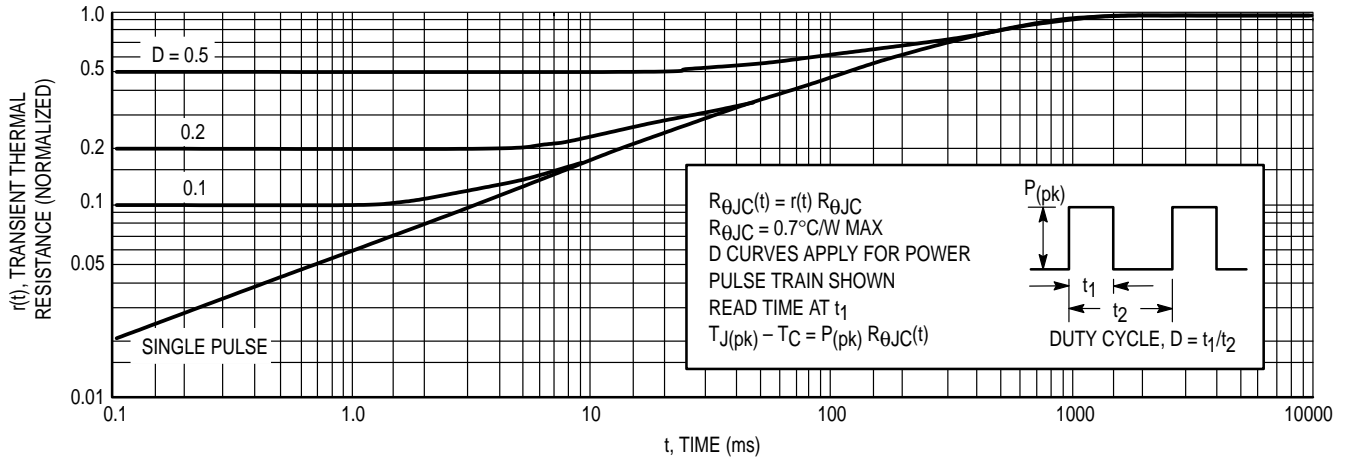


Figure 15. Thermal Response

OVERLOAD CHARACTERISTICS

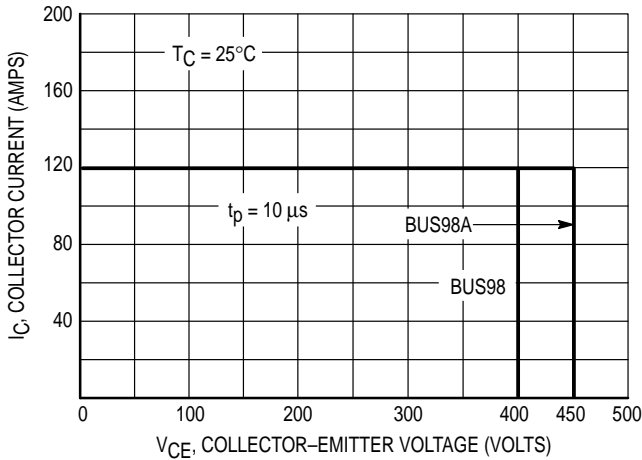


Figure 16. Rated Overload Safe Operating Area (OLSOA)

OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

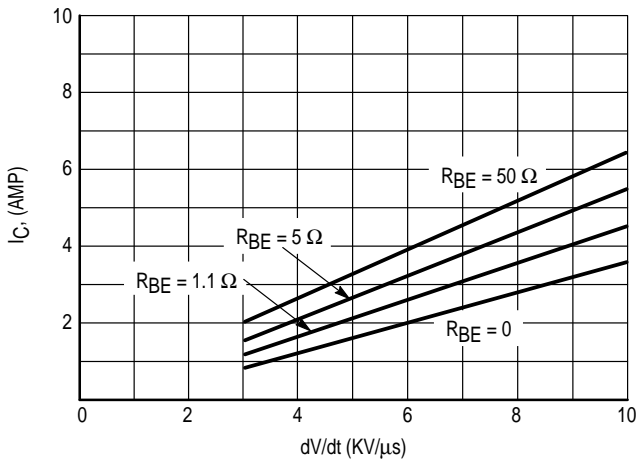
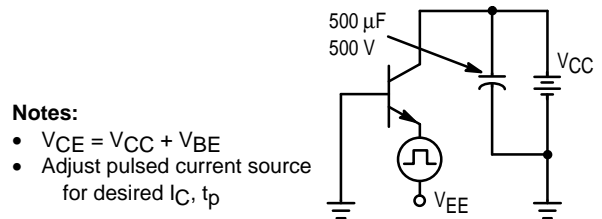


Figure 17. $I_C = f(dV/dt)$

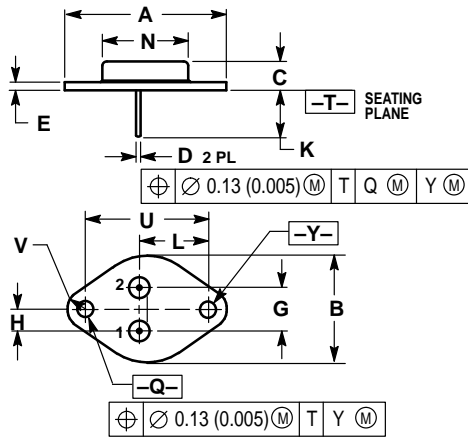


Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p

Figure 18. Overload SOA Test Circuit

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF	—	39.37 REF	—
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC	—	10.92 BSC	—
H	0.215 BSC	—	5.46 BSC	—
K	0.440	0.480	11.18	12.19
L	0.665 BSC	—	16.89 BSC	—
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC	—	30.15 BSC	—
V	0.131	0.188	3.33	4.77

STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

CASE 1-07
 TO-204AA (TO-3)
 ISSUE Z

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 USA / EUROPE: Motorola Literature Distribution;
 P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609
 INTERNET: <http://Design-NET.com>

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

