

TOSHIBA CMOS LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TC75S51F, TC75S51FU

SINGLE OPERATIONAL AMPLIFIER

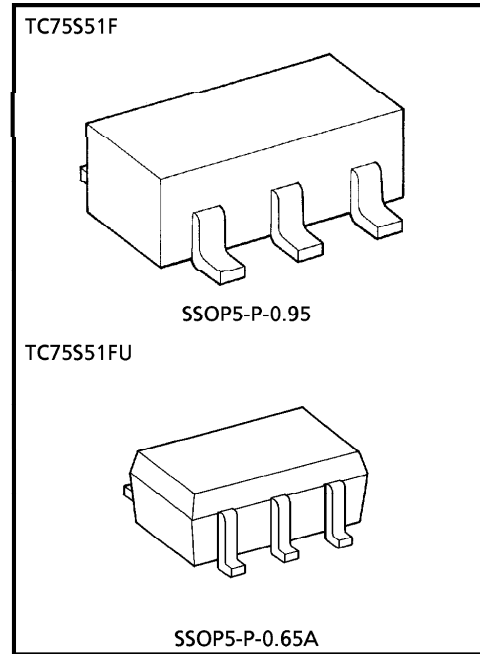
TC75S51F, TC75S51FU are CMOS operational amplifier with low supply voltage, low supply current.

FEATURES

- Low supply voltage : $V_{DD} = \pm 0.75 \sim \pm 3.5V$ or $1.5 \sim 7V$
- Low supply current : $I_{DD} (V_{DD} = 3V) = 60\mu A$ (Typ.)
- The internally phase compensated operational amplifier.
- Small package

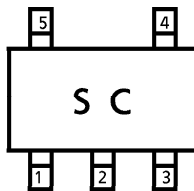
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}, V_{SS}	7	V
Differential Input Voltage	DV_{IN}	± 7	V
Input Voltage	V_{IN}	$V_{DD} \sim V_{SS}$	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{opr}	-40~85	°C
Storage Temperature	T_{stg}	-55~125	°C

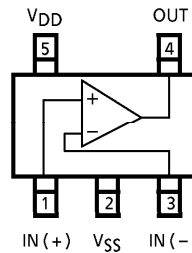


Weight
 SSOP5-P-0.95 : 0.014g (Typ.)
 SSOP5-P-0.65A : 0.006g (Typ.)

MARKING (TOP VIEW)



PIN CONNECTION (TOP VIEW)



961001EBA2

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ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS ($V_{DD} = 3.0V$, $V_{SS} = GND$, $T_a = 25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_S = 1k\Omega$, $R_F = 100k\Omega$	—	2	10	mV
Input Offset Current	I_{IO}	—	—	—	1	—	pA
Input Bias Current	I_I	—	—	—	1	—	pA
Common Mode Input Voltage	CMV_{IN}	2	$R_S = 1k\Omega$, $R_F = 100k\Omega$	0	—	2.5	V
Voltage Gain (Open Loop)	G_V	—	—	60	70	—	dB
Maximum Output Voltage	V_{OH}	3	$R_L \geq 100k\Omega$	2.9	—	—	V
	V_{OL}	4	$R_L \geq 100k\Omega$	—	—	0.1	V
Common Mode Input Signal Rejection Ratio	CMRR	2	$V_{IN} = 0.0 \sim 2.5V$	55	65	—	dB
Supply Voltage Rejection Ratio	SVRR	1	$V_{DD} = 1.5 \sim 7.0V$	60	70	—	dB
Supply Current	I_{DD}	5	—	—	60	200	μA

DC CHARACTERISTICS ($V_{DD} = 1.5V$, $V_{SS} = GND$, $T_a = 25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_S = 10k\Omega$, $R_F = 100k\Omega$	—	2	10	mV
Input Offset Current	I_{IO}	—	—	—	1	—	pA
Input Bias Current	I_I	—	—	—	1	—	pA
Common Mode Input Voltage	CMV_{IN}	2	$R_S = 10k\Omega$, $R_F = 100k\Omega$	0	—	1.0	V
Voltage Gain (Open Loop)	G_V	—	—	60	70	—	dB
Maximum Output Voltage	V_{OH}	3	$R_L \geq 100k\Omega$	1.4	—	—	V
	V_{OL}	4	$R_L \geq 100k\Omega$	—	—	0.1	V
Supply Current	I_{DD}	5	—	—	50	150	μA

(Note) This device should be operated less than $70\mu A$ source current.AC CHARACTERISTICS ($V_{DD} = 3.0V$, $V_{SS} = GND$, $T_a = 25^\circ C$)

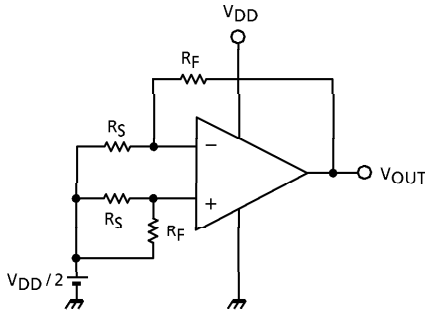
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate	SR	—	$A_V = 0dB$	—	0.5	—	$V / \mu s$
Unity Gain Cross Frequency	f_T	—	$A_V = 40dB$	—	0.6	—	MHz

AC CHARACTERISTICS ($V_{DD} = 1.5V$, $V_{SS} = GND$, $T_a = 25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate	SR	—	$A_V = 0dB$	—	0.3	—	$V / \mu s$
Unity Gain Cross Frequency	f_T	—	$A_V = 40dB$	—	0.5	—	MHz

TEST CIRCUIT

1. SVRR, V_{IO}



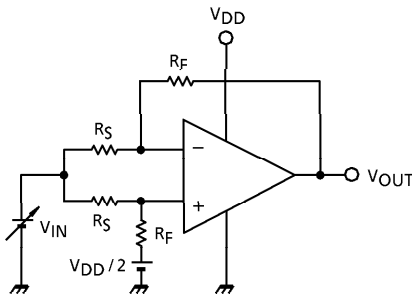
- SVRR
 $V_{DD} = 1.5V : V_{DD} = V_{DD1}, V_{OUT} = V_{OUT1}$
 $V_{DD} = 7.0V : V_{DD} = V_{DD2}, V_{OUT} = V_{OUT2}$

$$SVRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{DD1} - V_{DD2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

- V_{IO}

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMV_{IN}

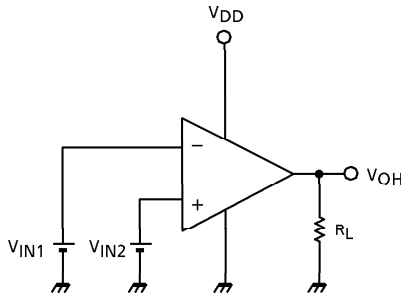


- CMRR
 $V_{IN} = 0.0V : V_{IN} = V_{IN1}, V_{OUT} = V_{OUT1}$
 $V_{IN} = 2.5V : V_{IN} = V_{IN2}, V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{IN1} - V_{IN2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

- CMV_{IN}

3. V_{OH}

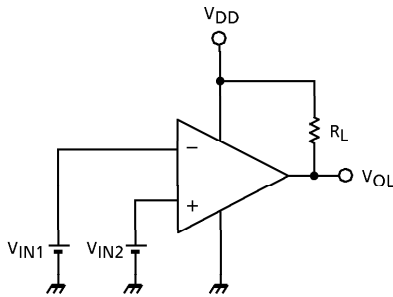


- V_{OH}

$$V_{IN1} = \frac{V_{DD}}{2} - 0.05V$$

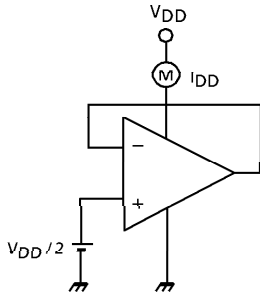
$$V_{IN2} = \frac{V_{DD}}{2} + 0.05V$$

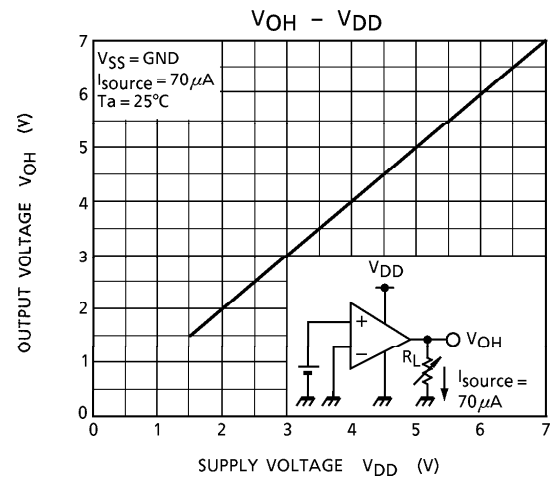
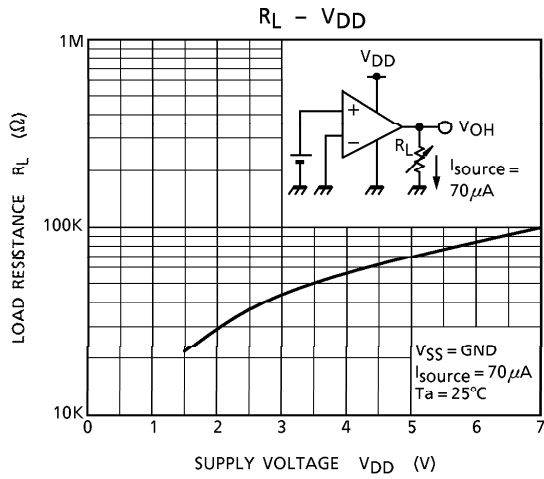
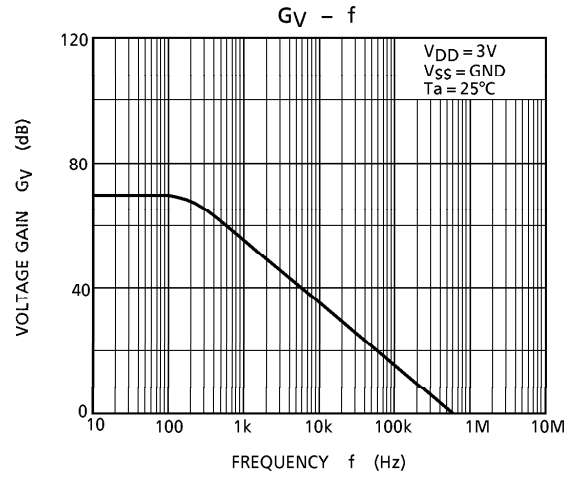
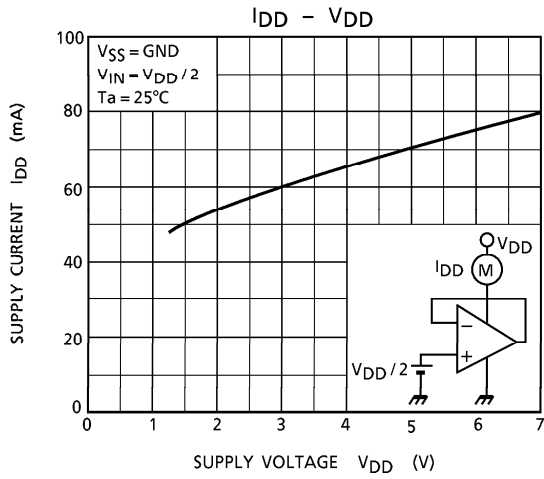
4. VOL

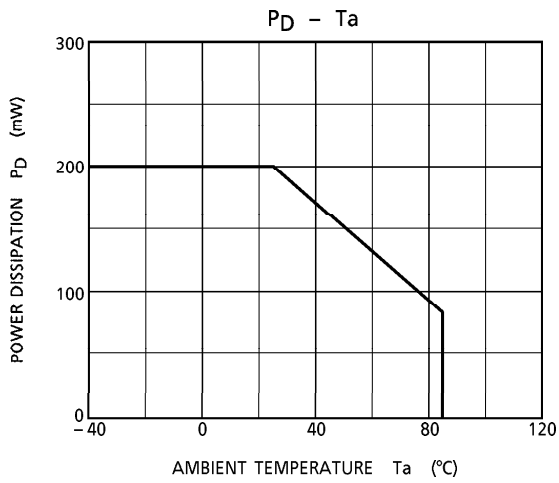
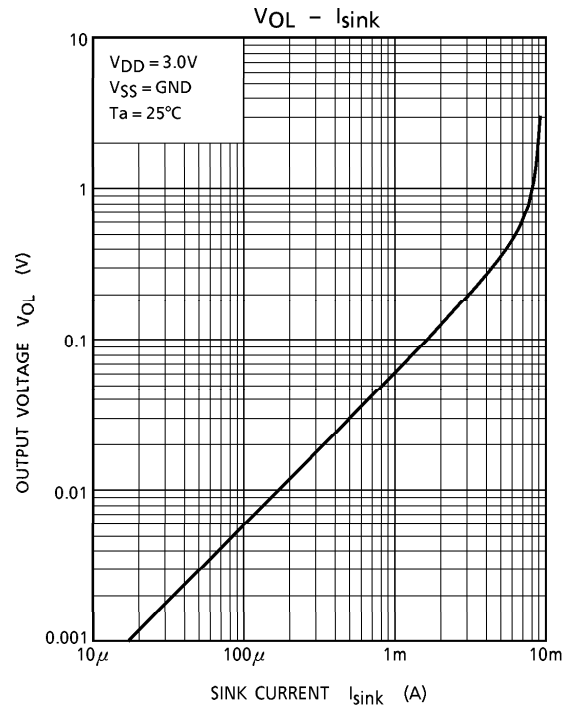
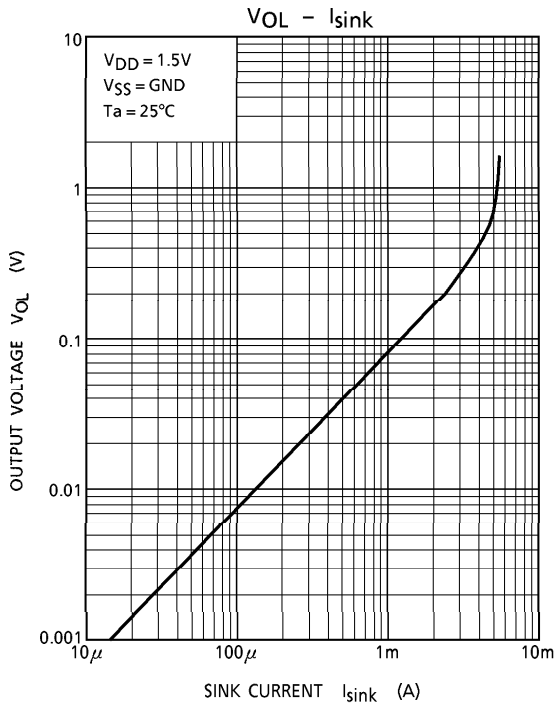


- VOL
$$V_{IN1} = \frac{V_{DD}}{2} + 0.05V$$
$$V_{IN2} = \frac{V_{DD}}{2} - 0.05V$$

5. IDD

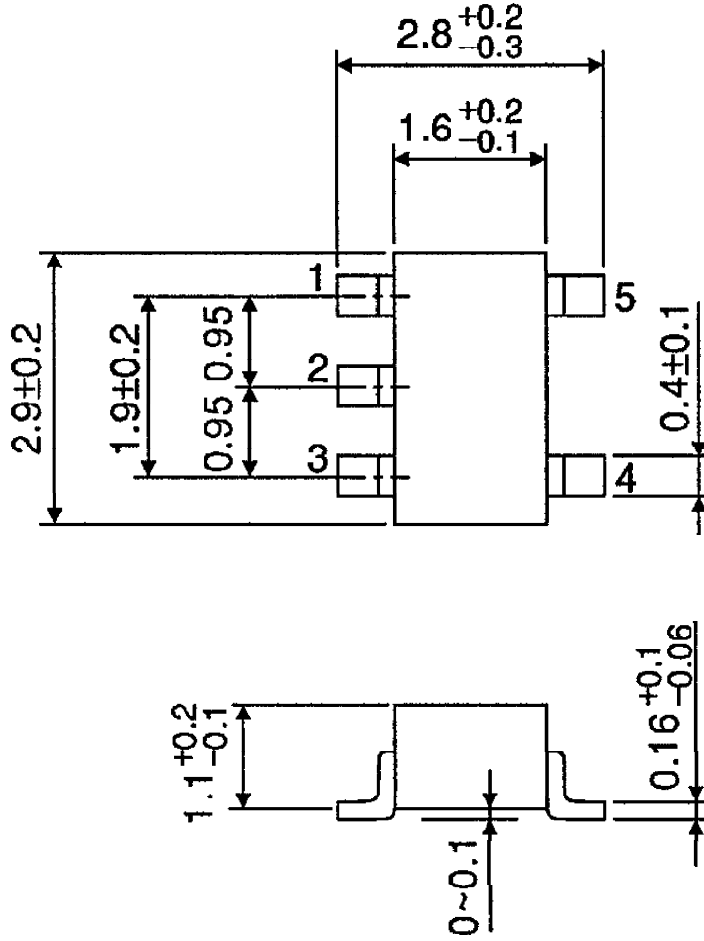






OUTLINE DRAWING
SSOP5-P-0.95

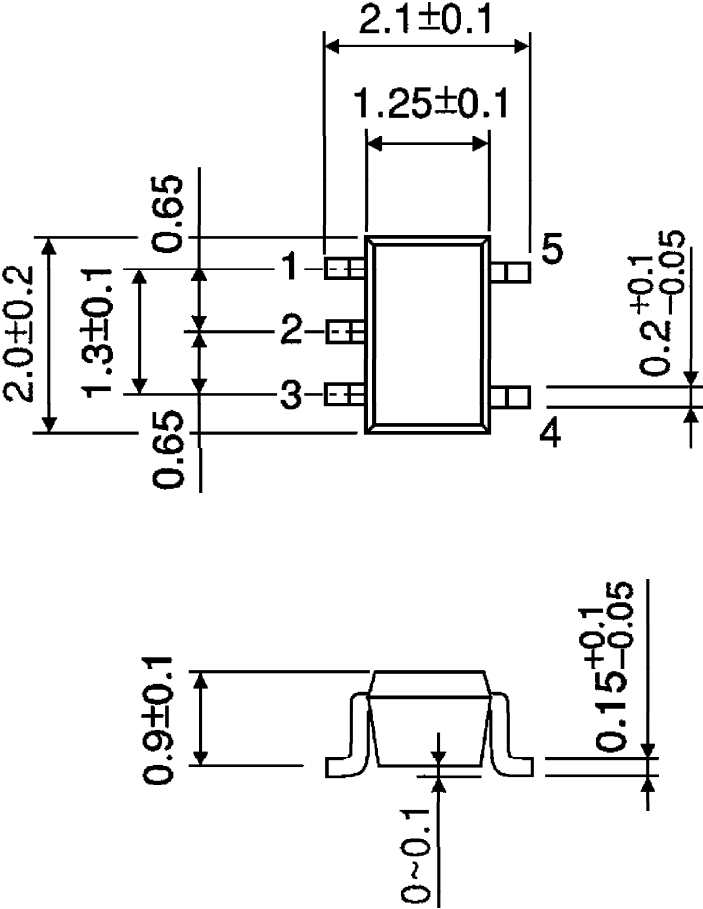
Unit : mm



Weight : 0.014g (Typ.)

OUTLINE DRAWING
SSOP5-P-0.65A

Unit : mm



Weight : 0.006g (Typ.)