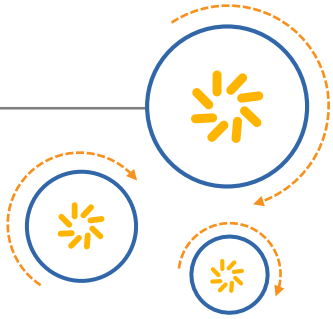
Qualcomm Technologies, Inc.



PM8916/PM8916-1

Device Specification

August 2015

Qualcomm Technologies, Inc.
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LM80-P0436-35 Rev. A

Revision history

Revision	Date	Description
A	August 11, 2015	Initial release

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1 Introduction

1.1 Documentation overview

This device specification defines the following power management IC devices: PM8916 and PM8916-1. Throughout this document, the devices are referred to as PM8916 when material being presented applies to both, unless mentioned otherwise for PM8916-1.

Technical information for PM8916 is primarily covered by the documents listed in Table 1-1, and all should be studied for a thorough understanding of the IC and its applications. Released PM8916 documents are available for download at https://developer.qualcomm.com/hardware/dragonboard-410c/tools.

Table 1-1 Primary PM8916 device documentation

Document number	Title/description
LM80-P0436-34	PM8916/PM8916-1 Device Revision Guide Provides a history of PM8916 revisions. It explains how to identify the various IC revisions and discusses known issues (or bugs) for each revision and how to work around them.
LM80-P0436-35 (this document)	PM8916/PM8916-1 Device Specification Provides all PM8916 electrical and mechanical specifications. Additional material includes pin assignment definitions; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by the company purchasing departments to facilitate procurement.
LM80-P0436-36	PM8916 Hardware Register Description Document

This PM8916 device specification is organized as follows:

Chapter 1 – Provides an overview of PM8916 documentation, shows a high-level PM8916 functional block diagram, lists the device features, and lists terms and acronyms used throughout the document.

Chapter 2 – Defines the IC pin assignments.

Chapter 3 – Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions.

Chapter 4 – Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 – Discusses shipping, storage, and handling of PM8916 devices.

Chapter 6 – Presents procedures and specifications for mounting the PM8916 onto printed circuit boards (PCBs).

Chapter 7 – Presents PM8916 reliability data, including definitions of the qualification samples and a summary of qualification test results.

1.2 PM8916 introduction

The PM8916 device (Figure 1-1) integrates all wireless handset power management, general housekeeping, and user interface support functions into a single mixed-signal IC. Its versatile design is suitable for multimode, multiband phones, and other wireless products such as data cards and PDAs.

The PM8916 mixed-signal HV-CMOS device is available in the 176-pin nanoscale package (NSP) that includes several ground pins for improved electrical ground, mechanical stability, and thermal continuity.

PM8916 supports APQ8016 platforms and PM8916-1 supports APQ8009 platforms. The only difference between PM8916 and PM8916-1 is the default power-on voltage settings.

Since the PM8916 device includes many diverse functions, its operation can be understood better by studying the major functional blocks individually. Therefore, the PM8916 document set is organized by the device functionality as follows:

- Input power management
- Output power management
- General housekeeping
- User interfaces
- IC interfaces
- Configurable pins – either multipurpose pins (MPPs) or general-purpose input/output (GPIOs) – that can be configured to function within some of the other categories.
- Most of the information contained in this document is organized accordingly – including the circuit groupings within the block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3). Refer to the *PM8916 Power Management IC Training Slides* (80-NK808-21) for more detailed diagrams and descriptions of the PM8916 device functions and interfaces.

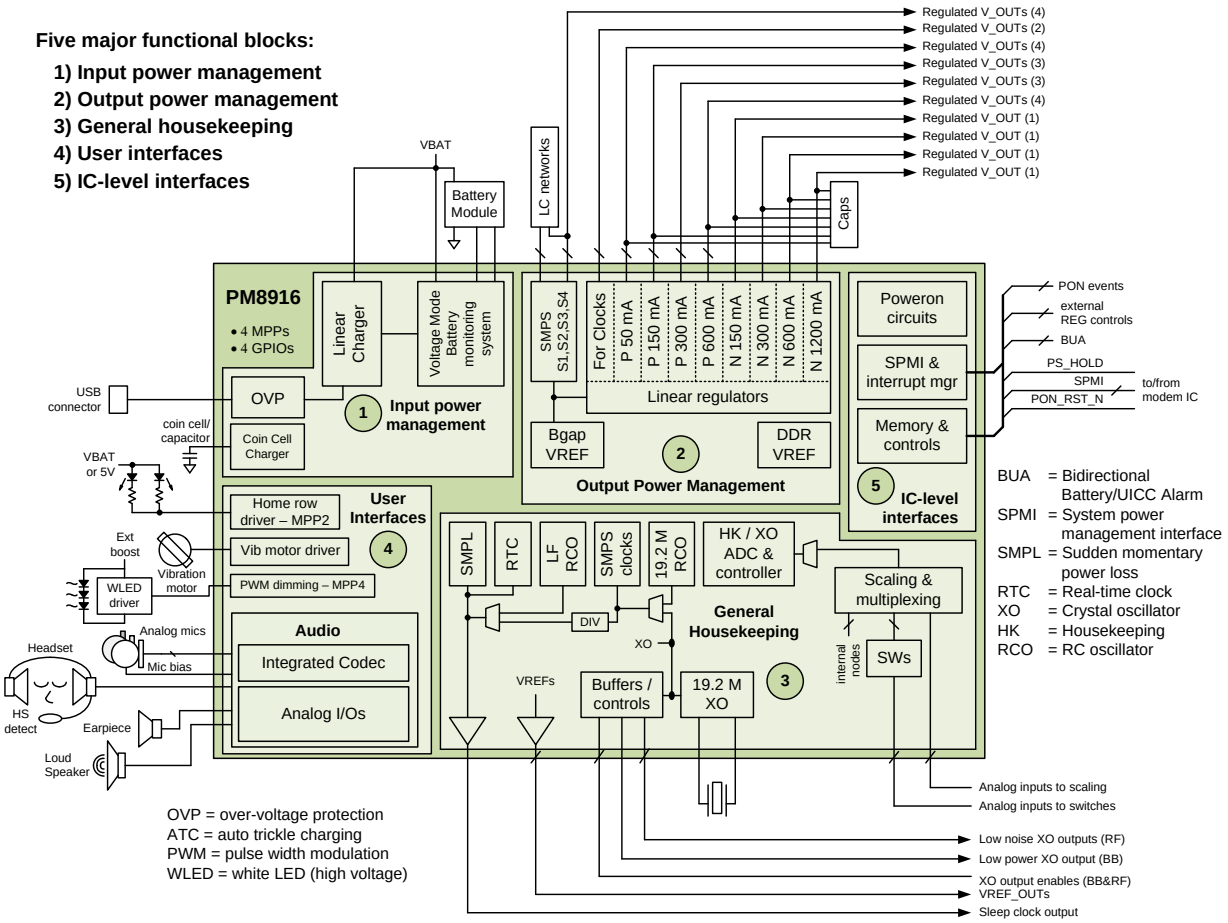


Figure 1-1 High-level PM8916 functional block diagram

1.3 PM8916 features

NOTE: Some of the hardware features integrated within the PM8916 must be enabled through the host IC software. Refer to the latest version of the applicable software release notes to identify the enabled PMIC features.

1.3.1 Highlighted features integrated into the PM8916

- Dual SIM dual active (DSDA) support
- Bidirectional battery UICC alarm (BUA) for graceful UICC shutdown upon battery or UICC removal.
- Linear battery charger
  - USB source with built-in 16 V over-voltage protection (OVP)
  - Integrated OVP FET
- Four GPIOs of which two can output high-speed clocks
- Pulse width modulator (PWM) for dimming control of external WLED IC driver

- Home row LED driver
- Plug-and-play support
- Programmable reset control
- Audio codec (ADCs and DACs), stereo head phone, ear and speaker amplifiers. The digital decimator and interpolator chains exist in the corresponding APQ8016/APQ8009.

1.3.2 Summary of PM8916 device features

Table 1-2 lists the features of the PM8916 device.

Table 1-2 PM8916 device features

Feature	PM8916 capability
Input power management	
Supported external power source	USB
Over-voltage protection	Fully integrated up to +16 V (integrated OVP FET)
Supported battery technologies	Lithium-ion, lithium-ion polymer
Charger regulation method	Linear battery charger ▪ Autonomous charging modes ▪ Trickle charging
Supported charging modes	Trickle, constant current, and constant voltage modes. Enhanced automation for lesser software interaction
Charger on indication	Dedicated charging indication LED current sink
Voltage, current, and temperature sensors	Internal and external nodes; reported to on-chip state-machine
Battery monitoring system	Voltage Mode Battery Monitoring system (VM-BMS)
Coin cell or capacitor backup	Keep-alive power source; orchestrated charging
Output voltage regulation	
Switched-mode power supplies:	▪ Four buck converters ▪ One 5 V boost converter
Low dropout linear regulators	▪ 20 LDOs ▪ Three NMOS LDOs ▪ 15 PMOS LDOs ▪ Two custom low-noise LDOs for the clock system
Pseudo-capless LDO designs	All LDOs except L1, L2, and L3
LPDDR support	Reference voltage output for LPDDR2/LPDDR3
General housekeeping	
On-chip ADC	Shared housekeeping (HK) and XO support
Analog multiplexing for ADC ▪ HK inputs ▪ XO input	▪ Many internal nodes and external inputs, including configurable MPPs ▪ Dedicated pin (XO_THERM)
Over-temperature protection	Multistage smart thermal control

Feature	PM8916 capability
19.2 MHz oscillator support	XO (with on-chip ADC)
XO controller and XO outputs	Four sets: ▪ Two low-noise RF outputs ▪ Two low-power baseband outputs
Sleep clock output	One (dedicated)
32 kHz clock source	XO/586 and RC CAL circuits provide real-time clock with alarm. 32,768 Hz crystal oscillator is not supported.
Real-time clock	RTC clock circuits and alarms
Audio inputs	▪ Three single-ended inputs ▪ Two ADCs
Multi-button headset control (MBHC)	▪ Up to five button MBHC headset support ▪ One input for headset jack detection
Audio outputs	▪ Four outputs – Ear, HPHL + HPHR, Class-D speaker driver ▪ Three DACs ▪ Over current protection on HPH, EAR, and speaker outputs
Multiple input/output audio sample rates	Supports sample rates 8 kHz, 16 kHz, 32 kHz, and 48 kHz
User interfaces	
Pulse width modulator	Dimming control of external WLED driver
Home row LED driver	Current sink through even MPPs
Other current drivers	Even MPPs can be configured to sink up to 40 mA ATC indicator (see input power management features)
Vibration motor driver	1.2 to 3.1 V in 100 mV increments
IC-level interfaces	
Primary status and control	2-line SPMI
Interrupt managers	Supported by SPMI
Optional hardware configurations	OPT bits select hardware configuration
Power sequencing	Power on, power off, and soft resets
Extra features	External regulator; detects inputs; battery-enabled UICC alarm; UIM support (x2)
Configurable I/Os	
MPPs	Four; configurable as digital in/out; unidirectional level-translating I/Os; analog multiplexer inputs; current sinks; VREF buffer outputs; MPP1 and MPP3 is fixed for VDD_PX_BIAS and VREF_DAC respectively
GPIO pins	Four; configurable as digital inputs or outputs or level-translating I/Os; all are faster than MPPs
Package	
Size	6.2 mm × 6.2 mm
Pin count and package type	176 pin WB-NSP

1.4 Terms and acronyms

Table 1-3 defines terms and acronyms used throughout this document.

Table 1-3 Terms and acronyms

Term or acronym	Definition
ADC	Analog-to-digital converter
AMSS	Advanced mobile subscriber station (software)
ANC	Active noise cancellation
BOM	Bill of materials
BPF	Bandpass filter
bps	Bits per second
CDMA	Code division multiple access
CP	Charge pump
DAC	Digital-to-analog converter
DMIC	Digital microphone
DRE	Dynamic range enhancement
ESD	Electrostatic discharge
ESR	Effective series resistance
I2C	Inter-integrated circuit
I2S	Inter-IC sound
IIR	Infinite impulse response
kbps	Kilobits per second
LBC	Linear battery charger
LDO	Low dropout (linear regulator)
LPF	Low-pass filter
MAD	Microphone activity detection
MBHC	Multi-button headset control
MIC or mic	Microphone
NS	Noise shaper
NVM	Nonvolatile memory
OEM	Original equipment manufacturer
OSR	Over-sampling rate
PA	Power amplifier
PCB	Printed circuit board
PCM	Pulse-coded modulation
PGA	Programmable gain amplifier
RoHS	Restriction of hazardous substances
Rx	Receive, receiver
SLIMbus	Serial low-power inter-chip media bus
SMT	Surface-mount technology

Term or acronym	Definition
SNR	Signal-to-noise ratio
ST	Sidetone
TCXO	Temperature-compensated crystal oscillator
Tx	Transmit, transmitter
VM-BMS	Voltage mode battery monitoring system
WCD	WSP coder/decoder
WLNSP	Wafer-level nanoscale package
WSP	Wafer-scale package
XO	Crystal oscillator
ZIF	Zero intermediate frequency

1.5 Special marks

Table 1-4 lists some special symbols used in this document.

Table 1-4 Special symbols

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA [7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, PON_RESET_N.
0x0000	Hexadecimal numbers are identified with an x in the number, (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number [for example, 0011 (binary)].
|	A vertical bar in the outside margin of a page indicates that a change has been made since the previous revision of this document.

2 Pin Definitions

The PM8916 is available in the 176 NSP – see Chapter 4 for package details. Figure 2-1 shows a high-level view of the pin assignments for the PM8916.

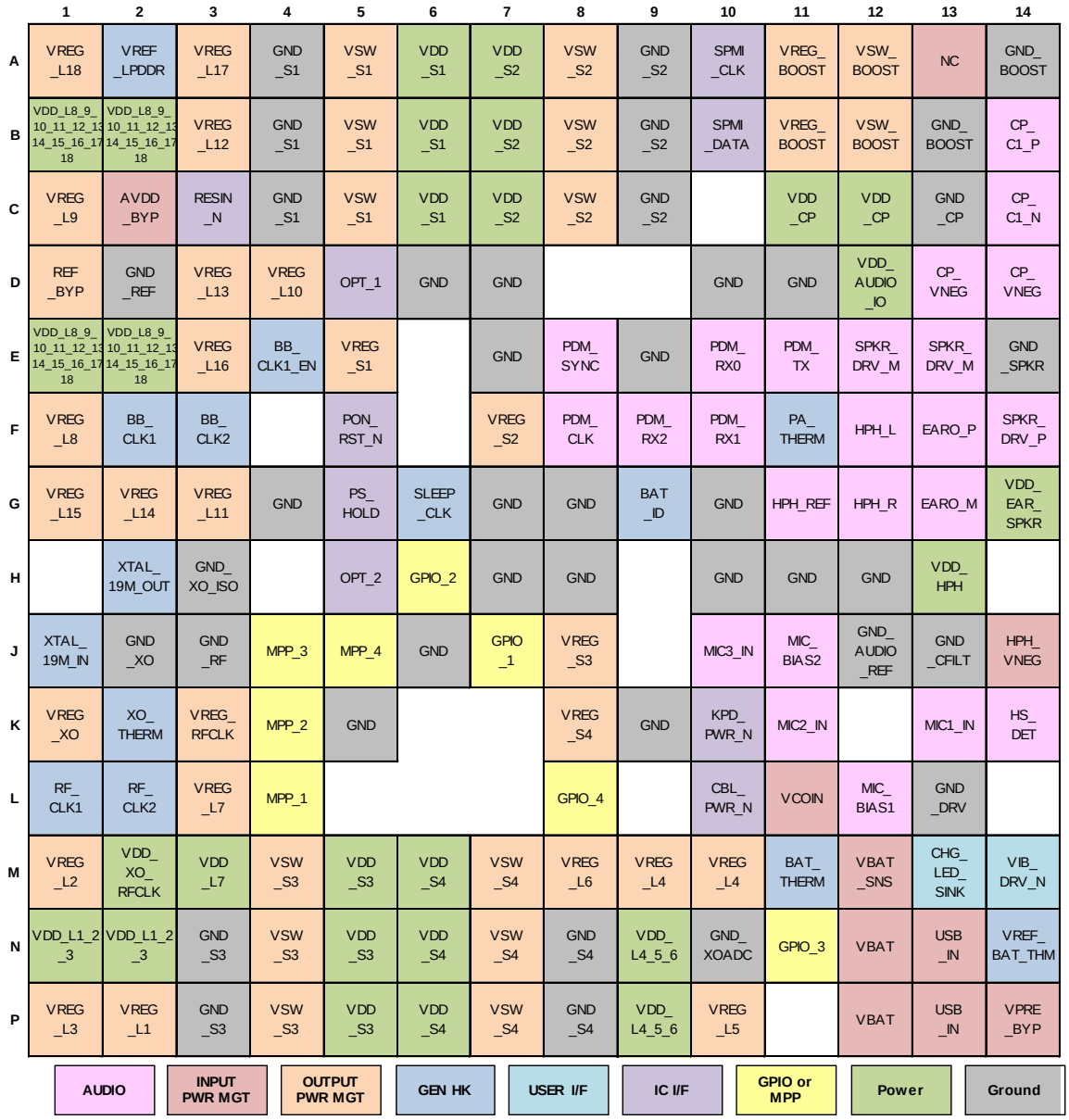


Figure 2-1 PM8916 pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
PI	Power input; a pin that handles 10 mA or more of current flow into the device
PO	Power output; a pin that handles 10 mA or more of current flow out of the device
Z	High-impedance (high-Z) output
Pad voltage groupings	
V_INT	Internally generated supply voltage for some power on circuits
V_PAD	Supply for host IC interfaces; connected internally to VREG_L5
V_XBB	Supply for XO low-power (BB) output buffers; connected internally to VREG_L7
V_XRF	Supply for XO low-noise (RF) output buffers; connected internally to LDO VREG_RFCLK
V_G	Pad voltage grouping (GPIO_1 and GPIO_2 cannot be configured to VBAT supply group) Selectable supply for GPIO circuits; options include: 0 = VBAT 1 = VBAT 2 = VREG_L2 3 = VREG_L5
V_M	Selectable supply for MPP circuits; options include: 0 = VBAT 1 = VBAT 2 = VREG_L2 3 = VREG_L5
GPIO pin configurations	
GPIO pins, when configured as inputs, have configurable pull settings	
NP	No internal pull enabled
PU	Internal pull-up enabled
PD	Internal pull-down enabled
GPIO pins, when configured as outputs, have configurable drive strengths	
H	High: ~ 0.9 mA at 1.8 V; ~ 1.9 mA at 2.6 V
M	Medium: ~ 0.6 mA at 1.8 V; ~ 1.25 mA at 2.6 V
L	Low: ~ 0.15 mA at 1.8 V; ~ 0.3 mA at 2.6 V

2.2 Pin descriptions

The following tables list the descriptions of all the respective pins, organized by their functional group:

- Table 2-2 – Input power management
- Table 2-3 – Output power management
- Table 2-4 – General housekeeping
- Table 2-5 – User interfaces
- Table 2-6 – Audio
- Table 2-7 – IC-level interfaces
- Table 2-8 – Configurable input/output – GPIO and MPPs
- Table 2-9 – Power supply pins
- Table 2-10 – Ground pins

Table 2-2 Pin descriptions – Input power management functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
Linear charger					
N13, P13	USB_IN		–	PI	Input power from USB source
C2	AVDD_BYP		–	AO	Bypass cap for internal analog circuits
P14	VPRE_BYP		–	AO	VPRE regulator load capacitor
BMS circuits					
N12, P12	VBAT		–	PI, PO	Battery node; input during battery operation, output during charging, and sense point for UVLO detection
M12	VBAT_SNS		–	AI	Main battery voltage sense point for VM-BMS, Vtrkl, VDD_MAX, and VBAT_WEAK
Coin cell or keep-alive battery					
L11	VCOIN		–	AI, AO	Sense input or charge output

[1]See Table 2-1 for parameter and acronym definition.

Table 2-3 Pin descriptions – output power management functions

Pad #	Pad name and/or function	Pad characteristics[1]		Functional description
		Voltage	Type	
Switched-mode power supply (SMPS) circuits				
A5, B5, C5	VSW_S1	–	PO	Buck converter S1 switching output
E5	VREG_S1	–	AI	Buck converter S1 sense point
A8, B8, C8	VSW_S2	–	PO	Buck converter S2 switching output
F7	VREG_S2	–	AI	Buck converter S2 sense point
M4, N4, P4	VSW_S3	–	PO	Buck converter S3 switching output
J8	VREG_S3	–	AI	Buck converter S3 sense point
M7, N7, P7	VSW_S4	–	PO	Buck converter S4 switching output
K8	VREG_S4	–	AI	Buck converter S4 sense point
A12, B12	VSW_BOOST	–	PI	Boost converter switching net
A11, B11	VREG_BOOST	–	PO	Boost converter output voltage
LDO linear regulators				
P2	VREG_L1	–	PO	Linear regulator L1 output
M1	VREG_L2	–	PO	Linear regulator L2 output
P1	VREG_L3	–	PO	Linear regulator L3 output
M10, M9	VREG_L4	–	PO	Linear regulator L4 output
P10	VREG_L5	–	PO	Linear regulator L5 output
M8	VREG_L6	–	PO	Linear regulator L6 output
L3	VREG_L7	–	PO	Linear regulator L7 output
F1	VREG_L8	–	PO	Linear regulator L8 output
C1	VREG_L9	–	PO	Linear regulator L9 output
D4	VREG_L10	–	PO	Linear regulator L10 output
G3	VREG_L11	–	PO	Linear regulator L11 output
B3	VREG_L12	–	PO	Linear regulator L12 output
D3	VREG_L13	–	PO	Linear regulator L13 output
G2	VREG_L14	–	PO	Linear regulator L14 output
G1	VREG_L15	–	PO	Linear regulator L15 output
E3	VREG_L16	–	PO	Linear regulator L16 output
A3	VREG_L17	–	PO	Linear regulator L17 output
A1	VREG_L18	–	PO	Linear regulator L18 output
K3	VREG_RFCLK	–	PO	Linear regulator for RF CLK output
K1	VREG_XO	–	PO	Linear regulator for XO output
Bandgap voltage reference (VREF) circuits				
D1	REF_BYP	–	AO	Bandgap reference bypass cap

[1]See Table 2-1 for parameter and acronym definition.

Table 2-4 Pin descriptions – general housekeeping functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
GPIO assignments for general housekeeping functions[2]					
MPP assignments for general housekeeping functions[3]					
Analog multiplexer and HK/XO ADC circuits					
K2	XO_THERM		–	AI	ADC input – XO thermistor
F11	PA_THERM		–	AI	AMUX input – PA thermistor output
M11	BAT_THERM		–	AI	AMUX input – Battery thermistor output
G9	BAT_ID		–	AI	AMUX input – Battery ID
19.2 MHz XO circuits					
J1	XTAL_19M_IN		–	AI	19.2 MHz crystal input
H2	XTAL_19M_OUT		–	AO	19.2 MHz crystal output
L1	RF_CLK1		V_XRF	DO	RF (low-noise) XO output 1
L2	RF_CLK2		V_XRF	DO	RF (low-noise) XO output 2
F2	BB_CLK1		V_XBB	DO	Baseband (low power) XO output 1
F3	BB_CLK2		V_XBB	DO	Baseband (low power) XO output 2
E4	BB_CLK1_EN		V_PAD	DI	Baseband XO output 1 enable
Sleep clock					
G6	SLEEP_CLK		V_PAD	DO	Sleep clock to host IC and others
VREF outputs					
N14	VREF_BAT_THM		–	AO	Reference voltage for XO thermistor
A2	VREF_LPDDR		–	AO	Reference voltage for LPDDR 2 / LPDDR 3 memory

[1]See Table 2-1 for parameter and acronym definition

[2]GPIOs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign a GPIO a particular function, identify the application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. Table 2-8 lists all the GPIOs.

[3]MPPs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign an MPP a particular function, identify the application's requirements and map each MPP to its function – carefully avoiding assignment conflicts. Table 2-8 lists all the MPPs.

Table 2-5 Pin descriptions – User interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
GPIO assignments for user interface functions[2]					
MPP assignments for user interface functions[3]					
Low-voltage current drivers					
M13	CHG_LED_SINK		–	AO	Charging indication LED driver output
Vibration motor driver					
M14	VIB_DRV_N		–	PO	Vibration motor driver output control

Table 2-6 Pin descriptions – Audio

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[4]		Functional description
			Voltage	Type	
L12	MIC_BIAS1		–	AO	Microphone bias #1
J11	MIC_BIAS2		–	AO	Microphone bias #2
D13, D14	CP_VNEG		–	AO	Charge pump negative output
B14	CP_C1_P		–	AO	Charge pump fly cap terminal 1
C14	CP_C1_N		–	AO	Charge pump fly cap terminal 2
K13	MIC1_IN		–	AI	Main mic
K11	MIC2_IN		–	AI	Headset mic
J10	MIC3_IN		–	AI	Second mic
K14	HS_DET		–	AI	Headset detection
F13	EARO_P		–	AO	Earpiece PA + output
G13	EARO_M		–	AO	Earpiece PA – output
F12	HPH_L		–	AO	Headphone PA left channel output
G11	HPH_REF		–	AI	Headphone PA ground sensing
G12	HPH_R		–	AO	Headphone PA right channel output
F14	SPKR_DRV_P		–	AO	Class-D speaker amp + output
E12, E13	SPKR_DRV_M		–	AO	Class-D speaker amp – output
F8	PDM_CLK		–	DI	PDM clock signal and master clock for codec
E8	PDM_SYNC		–	DI	PDM synchronization signal
E11	PDM_TX		–	DO	PDM Tx data channel
E10	PDM_RX0		–	DI	PDM RX0 data channel

[1] See Table 2-1 for parameter and acronym definition.

[2] GPIOs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign a GPIO a particular function, identify the application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. Table 2-8 lists all the GPIOs.

[3] MPPs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign an MPP a particular function, identify the application's requirements and map each MPP to its function – carefully avoiding assignment conflicts. Table 2-8 lists all the MPPs.

[4] See Table 2-1 for parameter and acronym definitions.

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[4]		Functional description
			Voltage	Type	
F10	PDM_RX1		–	DI	PDM RX1 data channel
F9	PDM_RX2		–	DI	PDM RX2 data channel
J14	HPH_VNEG		–	AI	Headphone amplifier negative supply

Table 2-7 Pin descriptions – IC-level interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
GPIO assignments for IC-level interface functions[2]					
MPP assignments for IC-level interface functions[3]					
Poweron circuit inputs					
L10	CBL_PWR_N		V_INT	DI	Cable poweron detect input
K10	KPD_PWR_N		V_INT	DI	Keypad poweron detect input
H5	OPT_2		V_INT	DI	Option HW configuration control bit 2
D5	OPT_1		V_INT	DI	Option HW configuration control bit 1
G5	PS_HOLD		V_PAD	DI	Power-supply hold control input
C3	RESIN_N		V_INT	DI	PMIC reset input
Poweron circuit outputs and primary PM/host IC interface signals					
A10	SPMI_CLK		V_PAD	DI	Slave and PBUS interface clock
B10	SPMI_DATA		V_PAD	DI, DO	Slave and PBUS interface data
F5	PON_RST_N		V_PAD	DO	Poweron reset output control

[1]See Table 2-1 for parameter and acronym definitions.

[2]GPIOs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign a GPIO a particular function, identify the application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. Table 2-8 lists all the GPIO1s.

[3]MPPs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign an MPP a particular function, identify the application's requirements and map each MPP to its function – carefully avoiding assignment conflicts. Table 2-8 lists all the MPPs.

Table 2-8 Pin descriptions – configurable input/output functions

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
Predefined MPP functions – available only at the assigned MPPs					
L4	MPP_1	VDD_PX_BIAS Digital I/O (optional)	– – V_M	AO-Z AO DI, DO	Configurable MPP Reference for host IC I/O Digital input/output usage (optional)
K4	MPP_2	SKIN_TEMP HR_LED_SNK Digital I/O (optional)	– – – V_M	AO-Z AI AI DI, DO	Configurable MPP Skin temperature measurement Home row LED current sink Digital input/output usage (optional)
J4	MPP_3	VREF_DAC Digital I/O (optional)	– – V_M	AO-Z AO DI, DO	Configurable MPP Reference for host IC DAC Digital input/output usage (optional)
J5	MPP_4	WLED_PWM Digital I/O (optional)	– V_M V_M	AO-Z DO DI, DO	Configurable MPP PWM control for external WLED driver Digital input/output usage (optional)
Predefined GPIO functions – available only at the assigned GPIOs					
J7	GPIO_1	UIM_BATT_ALM	V_G –	DO-Z DI, DO	Configurable GPIO Battery removal alarm for UIM and UIM battery alarm input to the APQ
H6	GPIO_2	NFC_CLK_REQ	V_G –	DO-Z DI	Configurable GPIO NFC control signal to request clock
N11	GPIO_3	WCN_LDO_EN	V_G –	DO-Z DO	Configurable GPIO Enable signal to power WCN with external 1.35 V LDO in PM8916-1
L8	GPIO_4	EXT_BUCK_EN	V_G –	DO-Z DO	Configurable GPIO Enable signal for external buck converter to power applications core.

NOTE: All MPPs default to their high-Z state at powerup and must be configured after powerup for their intended purposes. All GPIOs default to 10 µA pulldown at powerup and must be configured after powerup for their intended purposes.

NOTE: Configure unused MPPs as 0 mA current sinks (high-Z) and GPIOs as digital inputs with their internal pull-downs enabled.

NOTE: Only even MPPs can be configured as current sink and only odd MPPs can be configured as analog output.

[1]See Table 2-1 for parameter and acronym definitions.

Table 2-9 Pin descriptions – input DC power

Pad #	Pad name	Functional description
N1, N2[1]	VDD_L1_2_3	Power supply for LDO L1, L2, and L3 circuits
N9, P9	VDD_L4_5_6	Power supply for LDO L4, L5, and L6 circuits
B1, B2, E1, E2[2]	VDD_L8_9_10_11_12_13_14_15_16_17_18	Power supply for LDO L8 to L18 circuits
M2	VDD_XO_RFCLK	Power supply for LDO VREG_XO and VREG_RFCLK circuits
M3	VDD_L7	Power supply for LDO L7 circuits
A6, B6, C6	VDD_S1	Power supply for S1 buck converter
A7, B7, C7	VDD_S2	Power supply for S2 buck converter
M5, N5, P5	VDD_S3	Power supply for S3 buck converter
M6, N6, P6	VDD_S4	Power supply for S4 buck converter
Audio input power		
A13	NC	Can be connected to VBAT to maintain backward compatibility with version 1.1 of PM8916
H13	VDD_HPH	Headphone amplifier positive supply
G14	VDD_EAR_SPKR	Ear and class-D speaker amplifier supply
D12	VDD_AUDIO_IO	I/O supply for codec
C11, C12	VDD_CP	Charge pump power supply

Table 2-10 Pin descriptions – grounds

Pad #	Pad name	Functional description
PM88916		
A14, B13	GND_BOOST	Boost ground net
D6, D7, D10, D11, E7, E9, G4, G7, G8, G10, H7, H8, H10, H11, H12, J6, K5, K9	GND	Ground for non-specialized circuits
L13	GND_DRV	Ground for vibrator driver
D2	GND_REF	Ground for bandgap reference circuit
A4, B4, C4	GND_S1	Ground for S1 buck converter circuits
A9, B9, C9	GND_S2	Ground for S2 buck converter circuits
N3, P3	GND_S3	Ground for S3 buck converter circuits
N8, P8	GND_S4	Ground for S4 buck converter circuits
J2	GND_XO	Ground for XO circuits
J3	GND_RF	Ground for RF circuits
N10	GND_XOADC	Ground for XO ADC circuits
H3	GND_XO_ISO	Dedicated ground for XO substrate noise isolation

[1]Pad N1 and N2 have been combined to same input voltage group from Rev. 2.0.

[2]Pads B1, B2 and E1, E2 have been combined to same input voltage group from Rev 2.0.

Pad #	Pad name	Functional description
C13	GND_CP	Charge pump ground
E14	GND_SPKR	Class-D speaker amp ground
J13	GND_CFILT	Ground reference for PMIC bias
J12	GND_AUDIO_REF	Ground reference; connection for audio codec

3 Electrical Specifications

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-1) reflect conditions that PM8916 may be exposed to outside of the operating limits, without experiencing immediate functional failure. They are limiting values, to be considered individually when all other parameters are within their specified operating ranges. Functionality and long-term reliability can only be expected within the operating conditions, as described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Power supply and related sense voltages				
USB_IN	Input power from USB source	-0.5	16	V
VDD_xx	PMIC power-supply voltages not listed elsewhere	-0.5	6	V
VBAT, VBAT_SNS	Main battery voltage Steady state Transient (< 10 ms)	 -0.5 -0.5	 6 7	 V V
VDD_CDC_VBAT	Power for audio codec	-0.5	6	V
VDD_EAR_SPKR	Power for ear and speaker driver	-0.5	6	V
Signal pins				
V_IN	Voltage on any non-power-supply pin[1]	-0.5	VXX + 0.5	V
ESD protection and thermal conditions – see Section 7.1.				

[1]VXX is the supply voltage associated with the input or output pin to which the test voltage is applied

3.2 Operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 3-2). The PM8916 meets all performance specifications listed in Section 3.3 through Section 3.11 when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Units
Power supply and related sense voltages					
USB_IN	Input power from USB source	4.35	–	6.2	V
VDD_xx	PMIC power-supply voltages not listed elsewhere1	3.0	3.6	4.5	V
VBAT, VBAT_SNS	Main battery voltage1	3.0	3.6	4.5	V
VCOIN	Coin cell voltage	2.0	3.0	3.25	V
VDD_CDC_VBAT	Power for audio codec	TBD	3.7	TBD	V
VDD_EAR_SPKR	Power for ear and speaker driver	3.0	3.7/5.0	5.50	V
Signal pins					
V_IN	Voltage on any non-power-supply pin1	0	–	VXX + 0.5	V
Thermal conditions					
Tc	Operating temperature (case)	- 30	+25	+85	°C

[1] V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.3 DC power consumption

This section specifies DC power supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default parameter settings.

Table 3-3 DC power supply currents

Parameter		Comments	Min	Typ	Max	Units
$IDD_{active1}$[1]	Supply current, active mode		–	4.2	6	mA
$IDD_{active2}$[2]	Supply current, active mode		–	5.5	7.5	mA
IDD_{sleep}[3]	Supply current, sleep mode 32 kHz sleep clock		–	290	450	µA
IDD_{off_ship}[4]	Supply current, off mode		–	5	18	µA
IDD_{coin}	Coincell supply current, off mode XTAL off (IDDcc_xoff)[5] RC calibration (IDDcc_rccal)[6]	 Average current	 – –	 2 5	 2.5 8	 µA µA
IDD_{CHG}[7]	USB charger supply current	Sleep mode	–	13.3	15	mA
IDD_{USB}[8]	USB charger current in suspend	Good battery, not charging	–	–	1.65	mA

Table 3-4 Audio power supply peak current

Parameter		Min	Typ	Max	Units
VDD_EAR_SPKR	Power for ear and speaker driver	–	–	1.0	A

[1] IDD_{Active}1 is the total supply current from a main battery with PM8916 on, crystal oscillators on, XO and BBCLK1 on at 19.2 MHz, driving no load, and these voltage regulators on with no load at the following: VREG_S1 = 1.15 V, VREG_S2 = 1.15 V, VREG_S3 = 1.35 V, VREG_S4 = 2.15 V, VREG_L2 = 1.2 V, VREG_L3 = 1.15 V,VREG_L5 = 1.8 V, VREG_L7 = 1.8 V, VREG_L8 = 2.9 V, VREG_L11 = VREG_L12 = 2.95 V, VREG_L13 = 3.075 V, MPP1 is on as analog buffer, and VREF_LPDDR is on.

[2] IDD_{Active}2 is the total supply current from a main battery with PM8916 on and IDD_{Active}1 condition plus: VREG_L1 = 1.225 V, VREG_L4 = 2.05 V, VREG_L6 = 1.8 V, VREG_L14 = 1.8 V, VREG_L17 = 2.85 V, VREG_RFCLK and RFCLK1 on.

[3] IDD_{Sl}eep is the total supply current from a main battery with PM8916 on, crystal oscillators on and these voltage regulators on with no load at the following: VREG_S1 = 1.15 V (PFM), VREG_S3 (PFM) = 1.35 V,VREG_S4 (PFM) = 2.15 V, VREG_L2 (LPM) = 1.2 V, VREG_L3 (LPM) = 1.15 V, VREG_L5 (LPM) = 1.8 V, and VREF_LPDDR is on.

[4] Total supply current from a main battery with PM8916 off and the 32 kHz crystal oscillator on. This only applies when the temperature is between -30°C and 60°C.

[5] IDD_{Cc_x}off is the total supply current from a 3.0 V coin cell with PM8916 off and the 32 kHz crystal oscillator off. This only applies when the temperature is between -30°C and 60°C.

[6] IDD_{Cc_rc}cal is the total supply current from a 3.0 V coin cell with PM8916 off, the 32 kHz crystal oscillator off and RCCAL enabled with nominal settings. This only applies when the temperature is between -30°C and 60°C.

[7] 5CHG is the total supply current from a charger, with the device configured into the sleep mode as specified in Note 2 above with USB_IN = 6 V and VMAXSEL setting = 4.2 V.

[8] IDD_{U}SB is the total supply current drawn from a USB charger when the phone has a good battery (> 3.2 V), and the phone is not drawing charging current from USB. When USB is suspended, the phone is not allowed to draw more than 2.5 mA from a PC. Specification allows for 850 µA current into external components connected to VBUS in this case.

3.4 Digital logic characteristics

PM8916 digital I/O characteristics such as voltage levels, current levels, and capacitance are specified in Table 3-5.

Table 3-5 Digital I/O characteristics

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High-level input voltage[1]		0.65 × V_{IO}	–	V_{IO} + 0.3[2]	V
V_{IL}	Low-level input voltage		-0.3	–	0.35 × V_{IO}[2]	V
V_{SHYS}	Schmitt hysteresis voltage		15	–	–	mV
I_L	Input leakage current[3]	V_{IO} = max, V_{IN} = 0 V to V_{IO}	-200	–	+ 200	nA
V_{OH}	High-level output voltage	I_{out} = I_{OH}	V_{IO} – 0.5	–	V_{IO}	V
V_{OL}	Low-level output voltage	I_{out} = I_{OL}	0	–	0.45	V
I_{OH}	High-level output current [4]	V_{out} = V_{OH}	3	–	–	mA
I_{OL}	Low-level output current[4]	V_{out} = V_{OL}	–	–	-3	mA
I_{OH_XO}	High-level output current[4]	XO digital clock outputs only	6	–	–	mA
I_{OL_XO}	Low-level output current[4]	XO digital clock outputs only	–	–	-6	mA
C_{IN}	Input capacitance[5]		–	–	5	pF

3.5 Input power management

All parameters associated with input power management functions are specified.

3.5.1 Over-voltage protection

PM8916 has power FET and charging current sensing feature. After the OVP/UVD comparators detect a valid charging source, the power FET driver is enabled. The USB_IN voltage is monitored by the OVP comparator with a threshold voltage of 6.2 V. When USB_IN exceeds this threshold, the comparator outputs a logic signal to turn off the power FET driver, which turns off the power FET within 1 μs.

3.5.2 External supply detection

The PMIC continually monitors the external supply voltages like USB_IN and the battery supply voltage VBAT. Internal detector circuits measure these voltages to recognize when an external supply is connected or removed, and verify that it is within its valid range when connected. Hysteresis prevents undesired switching near the thresholds, and status is reported to the on-chip state machine and to the host IC via interrupts.

[1] VIO is the supply voltage for the APQ/PMIC interface (most PMIC digital I/Os).

[2] MPP and GPIO pins comply with the input leakage specification only when configured as digital inputs, or set to their tristate mode.

[3] Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins (such as MPP and GPIO pins.

[4] Input capacitance is guaranteed by design, but is not 100% tested.

[5] VIO = VREG_L5.

Performance specifications related to detecting external supply voltages and protecting the PMIC are presented in future revisions of this document.

For a valid USB detection and PON trigger to happen, USB_IN voltage must be greater than under-voltage detection (UVD) and less than over-voltage detection (OVD) threshold.

Table 3-6 External source interface performance specifications

Parameter		Comments	Min	Typ	Max	Units
Negative voltage protection						
V_NEG	Negative input voltage	USB_IN	-0.3	–	–	V
UVD						
V(thr_coarse)	Coarse detect threshold	USB_IN – rising	1.0	1.7	2.0	V
V(thr_uvd_r)[1]	UVD threshold	USB_IN – rising		4.0		V
V(hyst_uvd)	UVD threshold hysteresis	USB_IN	150	200	250	mV
OVD						
V(thr_ovd_r)	OVD setting	USB_IN – rising	6.0	6.2	6.4	V
V(hyst_ovd)	OVD threshold hysteresis	USB_IN – falling	150	200	250	mV
t(db_ovd_r)	OVD debounce	USB_IN – rising	–	1.0		µs
t(db_ovd_f)	OVD debounce	USB_IN – falling	–	0	–	ms
R(ovp_fet_on)	OVP FET Rds(on)[2]	USB_IN = 5 V	–	220	300	mΩ
Recommended OVP output (LBC input)						
USB_IN	Charger input voltage[3]		4.35	–	6.5	V
V_{IN_MIN}	Charge current accuracy		-10		+10	%
	Input voltage limit programmable range	26.2 mV steps	4.229		5.0652	V
	Input voltage limit accuracy		-3		3	%

[1]Meets the 4.4 V VBUS minimum from an unloaded bus-powered hub as specified in the USB 2.0 specification.

[2]USB OVP FET on, USB_IN voltage jumps from 10 V to 15 V in 20 µs.

[3]This is the recommended operating range. The acceptable operating range is defined by the UVD and OVD thresholds specified elsewhere in this table.

3.5.3 Linear battery charger

3.5.3.1 LBC specifications

Table 3-7 Linear charger specifications

Parameter	Min	Typ	Max	Unit	Note
Battery/VDD voltage programmable range	4.0	4.20	4.775	V	25 mV steps
Battery/VDD voltage accuracy (Including line & load regulation and temperature variation – up to 150 mA load)	-1		1	%	
Charge current programmable range	90		1440	mA	90 mA steps
Charge current accuracy	-10		+10	%	
FET resistance from USBIN to VBAT		332	420	mΩ	
VBATDET comparator threshold accuracy	-2		2	%	
Battery charge termination current I_{BAT_MAX}: 90–450 mA I_{BAT_MAX}: 540–1440 mA		7 7.4		%	
IBAT_TERM accuracy I_{BAT_MAX} = 90 mA I_{BAT_MAX}: 180–450 mA I_{BAT_MAX}: 540–810 mA I_{BAT_MAX}: 900–1440 mA	 -3 -7 -20 -15		 +7 +7 +20 +15	 mA mA % %	

3.5.3.2 Charging-specific linear charger specifications

Battery charging is controlled by a PMIC state-machine. The first step in the automated charging process determines if trickle charging is needed. Charging of a *severely* depleted battery must begin with trickle charging (Table 3-8) to limit the current, avoid pulling VDD down, and protect the battery from more charging current than it can handle. Once a minimum battery voltage is established using trickle charging, constant-current charging is enabled to charge the battery quickly – this mode is sometimes called fast charging. Once the battery approaches its target voltage, the charge is completed using constant-voltage charging.

Table 3-8 Trickle charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Trickle charge – current		81	90	99	mA
Trickle charge – current accuracy		±10%			
Trickle voltage – threshold programmable range	15.62 mV steps, 2.796 V default	2.5	–	2.9842	V
Trickle voltage – threshold accuracy		-2	–	+2	%
Trickle voltage – threshold hysteresis	VBAT falling	50	90	130	mV
Trickle voltage – threshold debounce	VBAT rising VBAT falling	– –	2 1	– –	sec ms

Parameter	Comments	Min	Typ	Max	Units
System weak – threshold programmable range	18.75 mV steps; 3.2 V default Detect depleted battery	3.0	3.206	3.581	V
System weak – threshold accuracy		-2	–	+2	%
System weak – threshold falling hysteresis	VBAT falling	70	110	150	mV
System weak – threshold debounce	VBAT rising/falling	–	1	–	ms

Constant-current charging

The PMIC parameters associated with constant-current charging are specified in the following subsections:

- External supply detection Section 3.5.2
- Battery voltage monitoring system Section 3.5.4

Additional performance specifications for constant-current charging are not required.

Constant-voltage charging

The PMIC parameters associated with constant-voltage charging are specified in the following subsections:

- External supply detection Section 3.5.2
- Battery voltage monitoring system Section 3.5.4

Additional performance specifications for constant-voltage charging are not required.

Figure 3-1 shows the LBC flowchart.

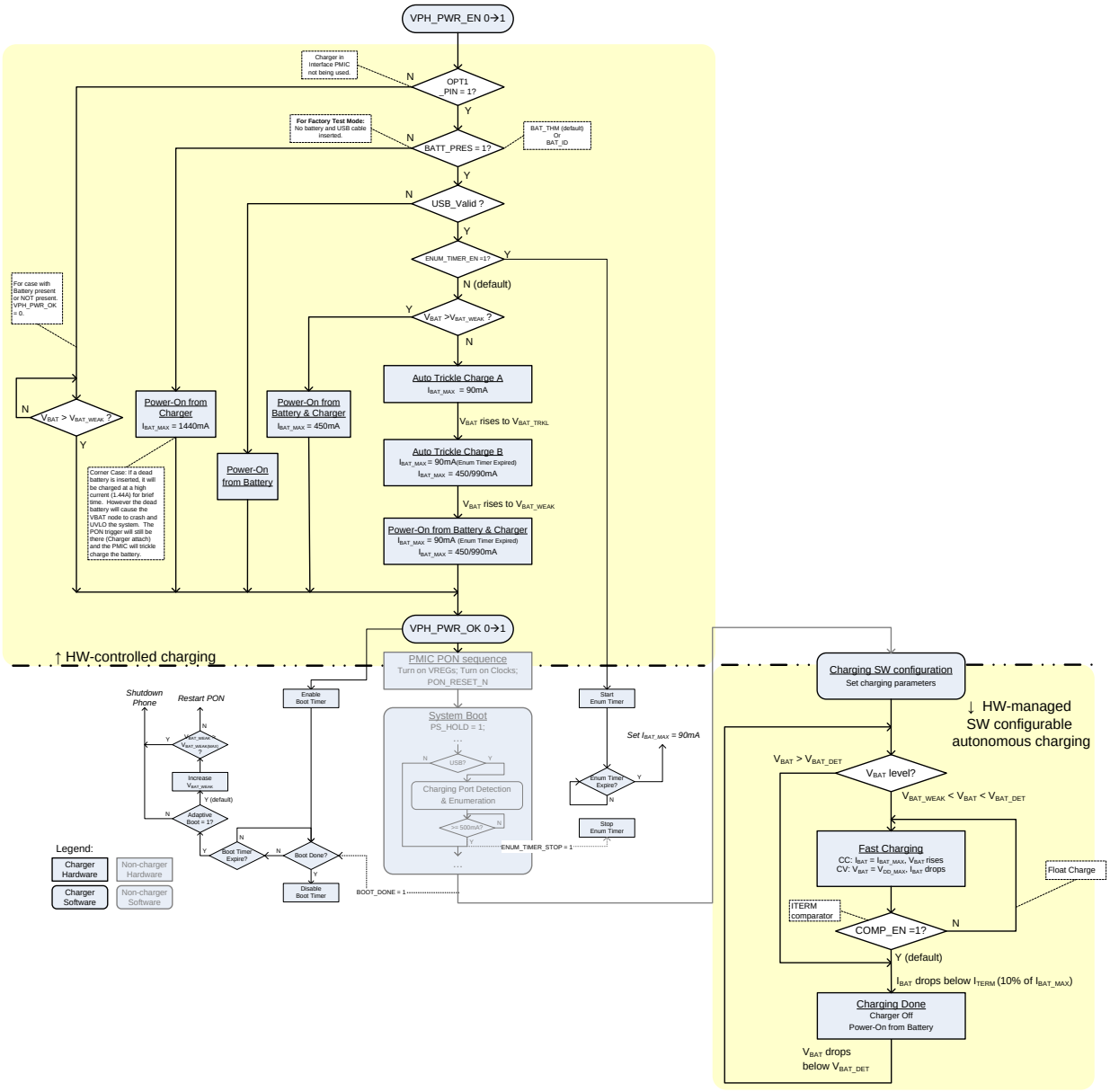


Figure 3-1 LBC flowchart

3.5.4 Battery voltage monitoring system

3.5.4.1 Under-voltage lockout

The handset supply voltage (VDD) is monitored continuously by a circuit that automatically turns off the device at severely low VDD conditions.

UVLO events do not generate interrupts. They are reported to the host IC via the PON_RESET_N signal. UVLO-related voltage and timing specifications are listed in Table 3-9.

Table 3-9 UVLO performance specifications

Parameter	Comments	Min	Typ	Max	Units
Rising threshold voltage	Programmable value, 50 mV steps	1.675	2.725	3.225	V
Hysteresis	175 mV setting	125	175	225	mV
	300 mV setting	250	300	350	mV
Falling threshold voltage	175 mV hysteresis setting	1.500	2.550	3.050	V
	300 mV hysteresis setting	1.375	2.425	2.925	V
UVLO detection interval		–	1	–	µs

3.5.4.2 SMPL

The PMIC SMPL feature initiates a power-on sequence if the monitored VDD drops out of range and then returns in-range within a programmable interval. When enabled by software, SMPL achieves immediate and automatic recovery from momentary power loss (such as a brief battery disconnect when the device is jarred).

SMPL performance specifications are given in Table 3-10.

Table 3-10 SMPL performance specifications

Parameter	Comments	Min	Typ	Max	Units
Minimum SMPL interval	Programmable range	0.5	–	2	s

3.5.5 Voltage mode battery monitoring system (VM-BMS)

Table 3-11 Battery fuel-gauge specifications

Parameter	Comments	Min	Typ	Max	Units
Effective number of bits (ENOB) of battery-voltage measurement		–	13	–	bits
OCV measurement	Accuracy	-15	–	15	mV
	Repeatability (with charger attached)	-3	–	3	mV

Table 3-12 State of charge (SOC) specifications

Parameter	Comments	Typ	Max[1]	Units
SOC accuracy at power on				
Battery capacity > 80% or < 20%) Battery capacity between 20% and 80%	SOC accuracy immediately after powering on with settled battery with capacity > 80% or < 20% SOC accuracy immediately after powering on with settled battery, with capacity between 20% and 80%	±0.5 ±3	±3 ±15	% %
SOC accuracy after power on				
Battery capacity > 80% or < 20%)	SOC accuracy at any time during a charge or discharge cycle after powering on with settled battery with capacity > 80% or < 20%	–	±15	%
Battery capacity between 20% and 80%	SOC accuracy at any time during a charge or discharge cycle after powering on with settled battery, with capacity between 20% and 80%	–	±25	%
Battery capacity 0% to 100%	Average SoC accuracy over complete charge/discharge cycle	5	–	%

3.5.6 Battery interface parameters (BTM and BPD)

The PMIC interface with the battery enables battery-temperature monitoring (BTM) and battery-presence detection (BPD); pertinent performance specifications are given in Table 3-13.

If BAT_ID is not used, that pin can be grounded. If BAT_THERM is not used, it too can be grounded, and the software's battery temperature feature ***must be*** disabled. If external charger is used, then BAT_THERM should be grounded.

Table 3-13 Battery interface specifications

Parameter	Comments	Min	Typ	Max	Units
Battery-temperature monitoring (BTM)					
Cold-comparator threshold programmable settings	Fraction of VREF_BAT_THM; selectable as 70% or 80%	70	–	80	%
Cold-comparator offset		-10	–	+10	mV
Cold-comparator voltage hysteresis 70% setting 80% setting	VREF_BAT_THM falling (battery warming)	 -80 -70	 – –	 -40 -35	 mV mV
Cold-comparator debounce	VBAT_THM rising VBAT_THM falling	0.5 0.5	– –	2.5 2.5	ms s
Hot-comparator threshold programmable settings	Fraction of VREF_BAT_THM; selectable as 25% or 35%	25	–	35	%
Hot-comparator offset		-10	–	+10	mV

[1]Valid over a temperature range of -20°C to 70°C.

Parameter	Comments	Min	Typ	Max	Units
Hot-comparator voltage hysteresis 35% setting 25% setting	VREF_BAT_THM failing (battery cooling)	 25 15	 – –	 50 30	 mV mV
Hot-comparator debounce	VBAT_THM rising VBAT_THM falling	0.5 0.5	– –	2.5 2.5	ms s
Battery-presence detection (BPD)					
BPD-comparator threshold	Fraction of VREF_BAT_THM	–	95	–	%
BPD-comparator offset		-50	–	+50	mV
BPD-comparator debounce VREF_BAT_THM rising (battery removal) VREF_BAT_THM falling (battery insertion)		1 –	– 2	6 –	µs s

Figure 3-2 shows the BTM block diagram, and Table 3-14 lists the equations for calculating the R_{S1} and R_{S2} external resistors needed to support the BTM feature.

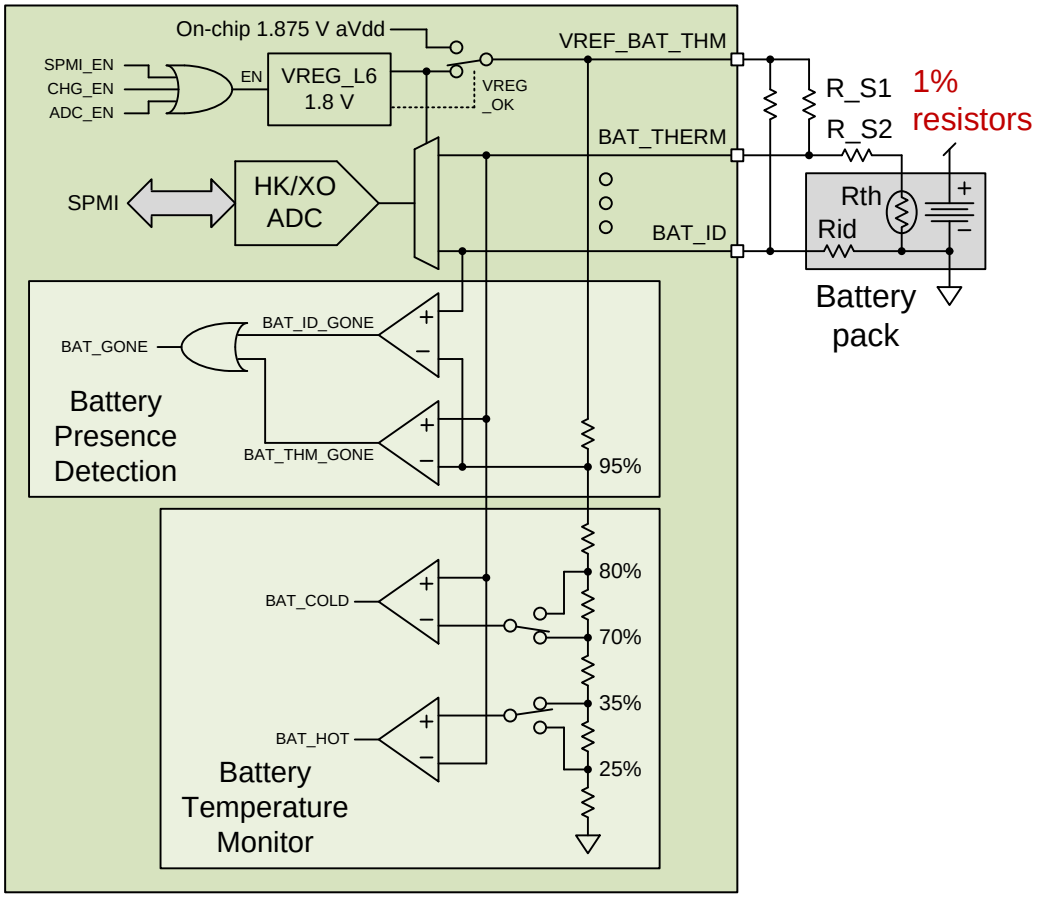


Figure 3-2 Battery-temperature monitoring

Table 3-14 Battery-temperature monitoring calculations

Battery charging window	BTM comparator thresholds	Minimum resistor values
0 to 40 or 45ºC	70% to 35%	R_S1 = 39 × (R_cold – R_hot) / 70 R_S2 = (3 × R_cold –13×R_hot) / 10
-10 to 60ºC	80% to 25%	R_S1 = 3 × (R_cold – R_hot) / 11 R_S2 = (R_cold – 12 × R_hot) / 11

3.5.7 Coin cell charging

Coin cell charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage source and a programmable series resistor. The host IC reads the coin cell voltage through the PMIC's analog multiplexer to monitor charging. Coin cell charging performance is specified in Table 3-15.

Table 3-15 Coin cell charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Target regulator voltage	VIN > 3.3 V, ICHG = 100 µA	2.5	3.1	3.2	V
Target series resistance		800	–	2100	□
Coin cell charger voltage error	ICHG = 0 µA	-5	–	5	%
Coin cell charger resistor error		-20	–	20	%
Dropout voltage[1]	ICHG = 2 mA	–	–	200	mV
Ground current, charger enabled VBAT = 3.6 V, T = 27ºC VBAT = 2.5 to 5.5 V	PMIC = off; VCOIN = open	 – –	 4.5 –	 – 8	 µA µA

3.6 Output power management

Output power management circuits include:

- Bandgap voltage reference circuit
- Buck SMPS circuits
- LDO linear regulators

The PM8916 provides all the regulated voltages needed for most wireless handset applications. Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, support power-management sequencing, and to meet different voltage-level requirements.

A total of 24 programmable voltage regulators are provided by the PM8916, with all outputs derived from a common bandgap reference circuit. Each regulator can be set to a low-power mode for power savings.

A high-level summary of all regulators and their intended uses is presented in Table 3-16.

[1]Set the input voltage (VBAT) to 3.5 V. Note the charger output voltage; call this value V_0. Decrease the input voltage until the regulated output voltage (V_1) drops 100 mV ($V_1 = V_0 – 0.1$ V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout} = VBAT – V_1$).

Table 3-16 Regulator high-level summary

Function	Circuit type	Default voltage (V) with P code = 0[1]	Default voltage (V) with P code = 11	Programmable range (V)	Specified range (V)	Rated current[2] (mA)	Default on	Expected use
S1	SMPS	1.15	1.225	0.375–1.562	0.5–1.35	2500	Y	APQ8016/APQ8009 camera SS, graphics core, etc.
S2	SMPS	1.15	1.225	0.375–1.562	0.9–1.35	3000	Y	APQ8016/APQ8009application processor cores
S3	SMPS	1.35	1.35	0.375–1.562	1.25–1.35	1800	Y	Analog blocks of WAN, WLAN, source for GR1 (LDOs L1 and L3) and GR2 (LDO L2) rails
S4	SMPS	2.1	2.05	1.55–2.325	1.85–2.15	1500	Y	Codec analog and source for GR3 (LDOs L4, L5 & L6) and GR7 (LDO L7) rails
L1	NMOS LDO	1.2875	1.0	0.375–1.525	1.0–1.2875	250	N	Low voltage rail
L2	NMOS LDO	1.2	1.2	0.375–1.525	1.2	600	Y	Memory (EBI/LPDDR2/LPDDR3/eMMC) and MIPI analog rails
L3	NMOS LDO	1.15	1.225	0.375–1.525	0.65–1.35	350	Y	Host IC
L4	PMOS LDO	2.05	1.8	1.75–3.337	1.8–2.1	250	N	GPS eLNA
L5	PMOS LDO	1.8	1.8	1.75–3.337	1.8	200	Y	Codec and memory 1.8 V rails, WLAN IO
L6	PMOS LDO	1.8	1.8	1.75–3.337	1.8	150	Y	Camera, display and transducer 1.8 V rails and HK ADC
L7	PMOS LDO	1.8	1.8	1.75–3.337	1.8–1.9	110	Y	Host, BB_CLK driver

[1]Default voltages and power-on states may depend on option pin (OPT_x) or SBL settings.

[2]Since PM8916 has wire bond package, rated current of the LDOs will be less than the design specification. For example, although L1 is N1200 LDO type which is designed for 1.2 A, its rated current is limited to 250 mA mainly due to losses in the bond wire.

Function	Circuit type	Default voltage (V) with P code = 0[1]	Default voltage (V) with P code = 11	Programmable range (V)	Specified range (V)	Rated current[2] (mA)	Default on	Expected use
L8	PMOS LDO	2.9	2.9	1.75–3.337	2.9	400	Y	eMMC/NAND core
L9	PMOS LDO	3.3	3.3	1.75–3.337	3.3	600	N	Connectivity IC (WCN3620/WCN3660)
L10	PMOS LDO	2.8	2.8	1.75–3.337	2.8	150	N	Camera (Front and Rear) analog rails
L11	PMOS LDO	2.95	2.95	1.75–3.337	2.95	8001	Y	SD/MMC card
L12	PMOS LDO	2.95	2.95	1.75–3.337	1.8/2.95	50	Y	APQ8016/APQ8009 memory rail for SD
L13	PMOS LDO	3.075	3.075	1.75–3.337	3.075	50	Y	Codec and USB 3 V analog rails
L14	PMOS LDO	1.8	1.8	1.75–3.337	1.8/3.3	55	N	UIM 1
L15	PMOS LDO	1.8	1.8	1.75–3.337	1.8/3.3	55	N	UIM 2
L16	PMOS LDO	1.8	1.8	1.75–3.337	1.8/3.3	55	N	UIM 3
L17	PMOS LDO	2.85	2.85	1.75–3.337	2.85	450	N	LCD, transducers and camera 2.85 V rails
L18	PMOS LDO	2.7	2.7	1.75–3.337	2.7	150	N	Qualcomm RF360™
VREF_LPDDR	—	0.6125	0.6125	—	—		Y	LPDDR reference
MPP1	—	1.250	1.250	—	—		Y	APQ pad bias
VREG_XO	Low noise LDO	1.8	1.8	1.38–2.22	1.8	5		XO oscillator circuits
VREG_RFCLK	Low noise LDO	1.8	1.8	1.38–2.22	1.8	5		Low noise clock buffers

[1]LDO L11 would be able to provide current of 800 mA to support SDR104 mode. The regulation specification of 3% would not be met. Since minimum voltage needed at SD card is only 2.7 V, accuracy of 8.4% will be sufficient. The LDO L11 can provide current of 600 mA meeting all regulation specification.

3.6.1 Reference circuit

All PMIC regulator circuits and some other internal circuits are driven by a common, on-chip voltage reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pin to create a low-pass function that filters the reference voltage distributed throughout the device.

NOTE: Do not load the REF_BYP pin. Use an odd MPP configured as an analog output if the reference voltage is needed off-chip.

Applicable voltage-reference performance specifications are given in Table 3-17.

Table 3-17 Voltage-reference performance specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal internal VREF	At REF_BYP pin	–	1.250	–	V
Output voltage deviations Normal operation Normal operation Sleep mode	 Over-temperature only, -20 to +120ºC All operating conditions All operating conditions	 -0.32 -0.50 -1.0	 – – –	 +0.32 +0.50 +1.0	 % % %

3.6.2 Buck SMPS

The buck converter is a switched-mode power supply that provides an output voltage lower than its input voltage, and is therefore also known as a step-down converter. The PM8916 IC includes four SMPS. The SMPS bucks support PWM and PFM modes.

Pertinent performance specification is given in Table 3-18.

Table 3-18 SMPS performance specifications

Parameter	Comments	Min	Typ	Max	Units
Input voltage range		3		4.5	V
Output voltage ranges Programmable range	 25 mV steps 12.5 mV steps	 TBD TBD	 – –	 TBD TBD	 V V
Rated load current (I_rated) PWM mode	Continuous current delivery				
S1	V_{IN} = 3.0 V V_{IN} = 3.2 V V_{IN} = 3.4 V	1.5 2.0 2.5	– – –	– – –	
S2	V_{IN} = 3.0 V V_{IN} = 3.2 V V_{IN} = 3.4 V	2.0 2.2 3.0	– – –	– – –	A
S3	V_{IN} = 3.0 V V_{IN} = 3.2 V V_{IN} = 3.4 V	1.0 1.2 1.8	– – –	– – –	
S4	V_{IN} = 3.0 V V_{IN} = 3.2 V V_{IN} = 3.4 V	0.8 1.0 1.5	– – –	– – –	
PFM mode	Programmable	80			mA
Peak current limit (through inductor)	VREG pin shorted; current limit is set via SPMI programming.	70% * I_limit	I_limit	130% * I_limit	mA
Voltage error PWM mode PFM mode	 V_out > 1.0 V, I_rated / 2 V_out < 1.0 V, I_rated / 2 V_out > 1.0 V, I_rated / 2 V_out < 1.0 V, I_rated / 2	 -1 -10 -3 -30	 – – – –	 1 10 3 30	 % mV % mV
Overall error (includes voltage error, load and line regulation and errors due to temperature and process) PWM mode PFM mode	 V_out > 1.0 V, I_rated /2 V_out < 1.0 V, I_rated /2 V_out > 1.0 V, I_rated /2 V_out < 1.0 V, I_rated /2	 -2 -20 -5 -50	 – – – –	 2 20 5 50	 % mV % mV
Temperature coefficient		-100	–	100	ppm/C
Efficiency PWM mode PFM mode	VBAT 3.6 V V_out = 1.8 V, I_load = 300 mA V_out = 1.8 V, I_load = 10 to 600 mA V_out = 1.8 V, I_load = 800 mA V_out = 1.2 V, I_load = 5 mA	 – – – –	 TBD TBD TBD TBD	 – – – –	 % % % %
Enable settling time	From enable to within 1% of final value programmable in PBS		500		µs
Enable overshoot	V_out > 1.0 V, no load V_out < 1.0 V, no load	 –	 –	3 30	% mV
Voltage step settling time per LSB	To within 1% of final value	–	–	10	µs
Response to load transitions Dip due to low-to-high load Spike due to high-to-low load	PWM mode S1, S3, S4: 40 mA to 440 mA S2: 40 mA to 1040 mA S1, S3, S4: 440 mA to 40 mA S2: 1040 mA to 40 mA	 – –	 40 70	 – –	 mV mV

Parameter	Comments	Min	Typ	Max	Units
Line transient response	Using 3.6 V to 3.0 V square waveform with 10 µs rise/fall time and frequency of 217 Hz, I_load = 750 mA		8		mV
Output ripple voltage PWM pulse-skipping mode PWM non-pulse-skipping mode PFM mode	Tested at the switching frequency; Cap ESR < 20 mΩ 40 mA load; 20 MHz measurement bandwidth I_rated; 20 MHz measurement bandwidth 50 mA load; 20 MHz measurement bandwidth	 – – –	 20 10 50	 40 20 70	 mVpp mVpp mVpp
Load regulation	V_in ≥ V_out + 1 V; I_load = 0.05 * I_rated to I_rated	–	0.25	–	%
Line regulation	V_in = 3.2 V to 4.2 V; I_load = 100 mA	–	0.25	–	%/V
Power-supply ripple rejection (PSRR) 50 Hz to 1 kHz 1 kHz to 100 kHz 100 kHz to 1 MHz		 – – –	 40 20 30	 – – –	 dB dB dB
Output noise F < 5 kHz F = 5 kHz to 10 kHz F = 10 kHz to 500 kHz F = 500 kHz to 1 MHz F > 1 MHz	VREF = 0.625 V	 – – – – –	 -101 -106 -106 -116 -116	 – – – – –	 dBm/Hz dBm/Hz dBm/Hz dBm/Hz dBm/Hz
Peak output impedance vs frequency	1 kHz–1 MHz	–	150	–	mΩ
Ground current PWM mode, no load PFM mode, no load PFM mode, no load (with current boost)		 – – –	 550 20 30	 750 30 45	 µA µA µA

3.6.2.1 Efficiency plots

Figure 3-3 through Figure 3-6 show the efficiency plots for V_{in} = 3.7 V.

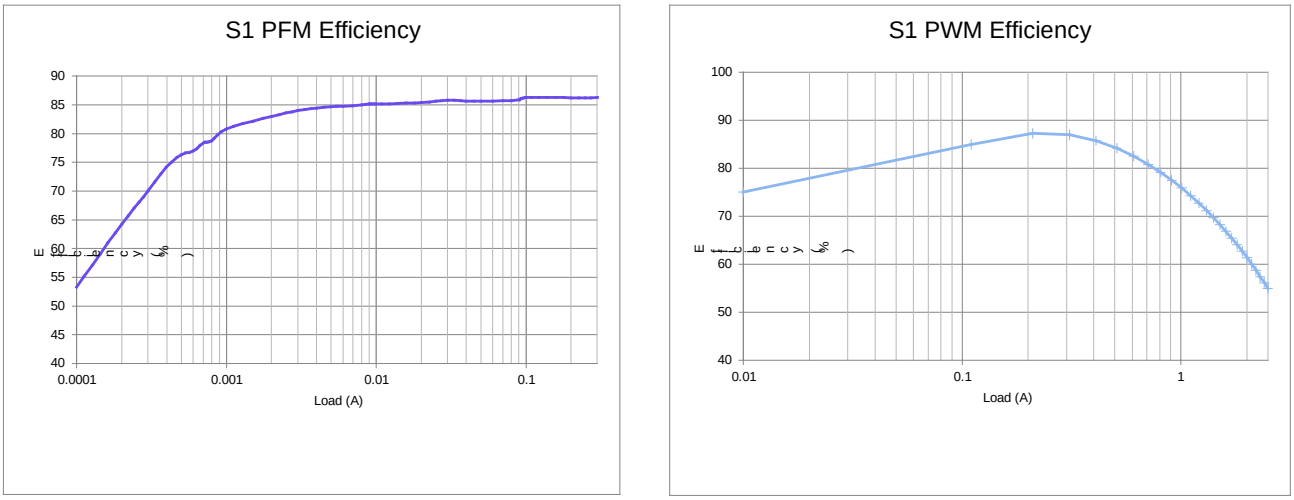
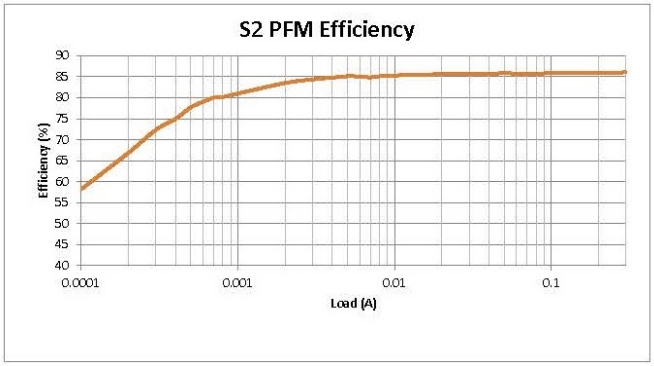


Figure 3-3 S1 PFM efficiency plots



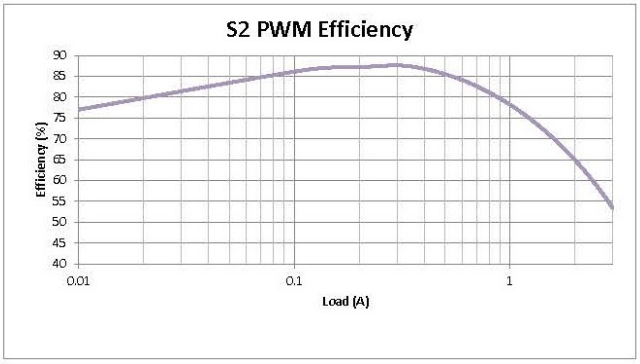
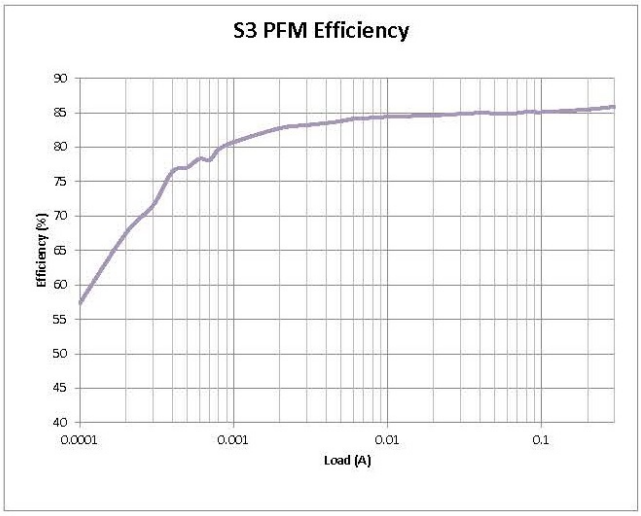


Figure 3-4 S2 PFM efficiency plots



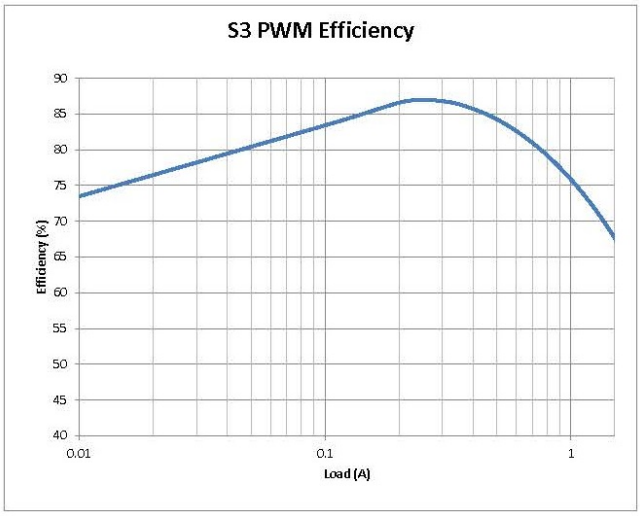


Figure 3-5 S3 PFM efficiency plots

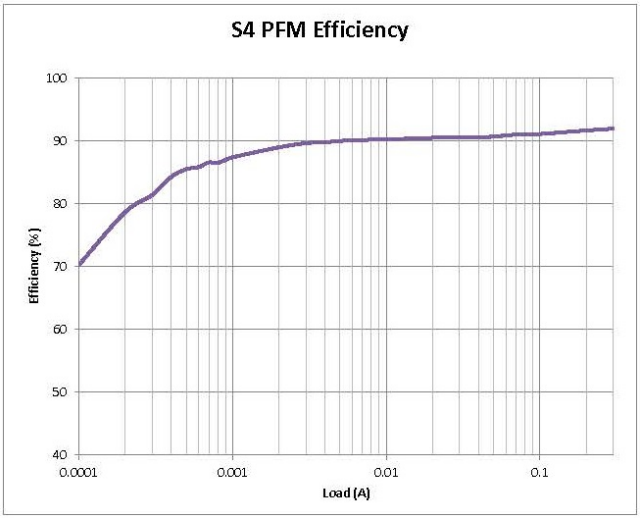


Figure 3-6 S4 PFM efficiency plots

3.6.3 Linear regulators

20 low dropout linear regulator designs are implemented within the PMIC:

- 3 NMOS LDOs
- 15 PMOS LDOs
- PMOS for on-chip clock circuits
  - These LDOs are not used off-chip, so their performance specifications are not published.

All other LDO performance specifications are presented in Table 3-19.

Table 3-19 LDO performance specifications

Parameter	Comments	Min	Typ	Max	Units
Output voltage ranges Programmable range All NMOS All PMOS	 12.5 mV steps 12.5 mV steps	 0.375 1.75	 – –	 1.525 3.337	 V V
Rated load current (I_rated), normal L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15 L16 L17 L18	Continuous current delivery	 – – – – – – – – – – – – – – – – – –	 – – – – – – – – – – – – – – – – – –	 250 600 350 250 200 150 110 400 600 150 800[1] 50 50 55 55 55 450 150	 mA mA mA mA mA mA mA mA mA mA mA mA mA mA mA mA mA mA
Rated load current, low-power mode L1, L2 L3 L4 – L13, L17, L18 L14 – L16	Continuous current delivery	 – – – –	 – – – –	 100 60 10 5	 mA mA mA mA
Pass FET power dissipation		–	–	600	mW

[1]For LDO L11 alone, overall error is specified for a load of 0-400 mA instead of its rated current.

Parameter	Comments	Min	Typ	Max	Units
Overall error at default voltage (includes DC voltage error, load[1] and line regulations and errors due to temperature and process) Normal mode Low-power mode		 -3 -4	 – –	 3 4	 % %
Temperature coefficient		-100	–	100	ppm°C
Transient settling time	To within 1% of final value	20	100	200	µs
Transient over/under-shoot Normal mode All NMOS LDOs All PMOS LDOs	 0.25 * I_rated to 0.75 * I_rated load step 0.1 * I_rated to 0.9 * I_rated load step	 -4 -70	 – –	 4 100	 % mV
Normal dropout voltage[2] [3] L1, L3 L2, L4 L5, L6, L7 L8, L11 L9 L10 L12, L13, L14, L15, L16 L17 L18	NPM, I_load = I_rated	 – – – – – – – – –	 – – – – – – – – –	 62.5 150 250 450 275 600 325 550 700	 mV
All NMOS LDOs All PMOS LDOs	LPM, I_load = I_rated	– –	– –	15 300	mV mV

[1]LDO voltage dropout measurement:

- Program the LDO for its desired operating voltage (V_set_d).
- Measure the output voltage; call this value V_set_m.
- Adjust the load such that the LDO delivers its rated output current (I_rated).
- Adjust the input voltage until V_in = V_set_m + 0.5 V.
- Decrease V_in until V_out drops 100 mV (until V_out = V_set_m – 0.1 V); call the resulting input value V_in_do and call this output value V_out_do.
- The voltage drop across the regulator under this condition is the dropout voltage (V_do = V_in_do – V_out_do).

[3]The dropout voltage is specified at rated current of the LDO. The voltage headroom required to maintain the LDO in regulation depends on the load current of the LDO. The current that an LDO can provide needs to be derated based on the headroom. Typical example, the LDO L5 has a dropout voltage of 250 mV. When headroom is 75 mV, the PMOS LDO can provide 200 * (75/250) = 60 mA current without going out of regulation.

[2] If a short is anticipated at the output of any of the LDOs, additional current protection circuits should be added. Alternatively, an external LDO with short circuit protection in lieu of PM8916 internal LDO should be used.

[3]LDO L11 would be able to provide current of 800 mA to support SDR104 mode. The regulation specification of 3% would not be met. Since minimum voltage needed at SD card is only 2.7 V, accuracy of 8.4% will be sufficient. The LDO L11 can provide current of 600 mA meeting all regulation specifications.

Parameter	Comments	Min	Typ	Max	Units
Load regulation	V_in > V_out + 0.5 V;				
Normal mode, all LDOs except L11	0.01 * I_rated to I_rated	–	–	2.1	%
Normal mode, L11	6 mA to 600 mA	–	–	2.1	%
Line regulation Normal mode		–	–	0.75	%/V
Power-supply ripple rejection Normal mode					
50 Hz to 1 kHz	All NMOS LDOs	–	70	–	dB
1 kHz to 10 kHz		–	60	–	dB
10 kHz to 100 kHz		–	40	–	dB
100 kHz to 1 MHz		–	30	–	dB
50 Hz to 1 kHz	All PMOS LDOs	–	43	–	dB
1 kHz to 10 kHz		–	35	–	dB
10 kHz to 100 kHz		–	13	–	dB
100 kHz to 1 MHz			13		dB
Low-power mode	All NMOS LDOs				
50 Hz to 1 kHz		–	50	–	dB
1 kHz to 100 kHz		–	40	–	dB
Short-circuit current limiting[1]		Not present for any of the LDOs.			
Soft current limit during startup	Current above I_rated	–	I_rated + 150	–	mA
Ground current					
Normal mode, no load					
All NMOS		–	75	100	µA
All PMOS		–	35	60	µA
Low-power mode, no load					
All NMOS		–	12	15	µA
All PMOS LDOs		–	5	6.5	µA
Bypass mode					
All NMOS LDOs		–	10	13	µA
All PMOS LDOs		–	–	1	µA
Bypass mode on-resistance					
L1 & L2		–	20	40	m □
L3		–	30	60	m □
L4		–	0.75	1.15	□
L6		–	1.1	1.66	□
L7, L10, L12, L18		–	2.2	2.4	□
L8, L9, L11, L17		–	0.56	0.84	□
L13, L16		–	6.6	10	□

[1]For LDO L11 alone, overall error is specified for a load of 0-400 mA instead of its rated current.

3.6.4 Internal voltage-regulator connections

Some regulator supply voltages and/or outputs are connected internally to power other PMIC circuits. These circuits will not operate properly unless their supplies are correct; this requires:

- Certain regulator supply voltages must be delivered at the right value.
- Corresponding regulator sources must be enabled and set to the proper voltages.

These requirements are summarized in Table 3-20.

Table 3-20 Internal voltage regulator connections

Feature	Regulator/ Connection	Default V	Comments
GPIO	VPH_PWR[1]	3.6	Available supplies for GPIO
	VREG_L2	1.2	
	VREG_L5	1.8	
MPP	VPH_PWR	3.6	Available supplies for MPP
	VREG_L2	1.2	
	VREG_L5	1.8	
Clocks	VREG_L5	1.8	Sleep clock pad (Vio)
	VREG_XO	1.8	XO core
	VREG_RFCLK	1.8	Low-noise output buffers (RF_CLKx)
	VREG_L7	1.8	Low-power output buffers (BB_CLKx) The BB_CLKx buffer supply L7 is forced on by BB_CLKx_EN.
SPMI	VREG_L5	1.8	SPMI pad (Vio)
AMUX	max{VBAT, USB_IN}	–	VADC (AMUX + XOADC) supply
BMS	VREG_L6	1.8	BMS VADC supply L6 is forced on by BMS for OCV measurement.
Miscellaneous	VREG_L5	1.8	

Table 3-21 Boost specifications

Parameter	Test conditions	Min	Typ	Max	Units
Boost efficiency	3.7 V input, 2.2 µH inductor, 600 mA load	84	88	–	%
	3.7 V input, 2.2 µH inductor, 900 mA load	80	87	–	%
Absolute voltage accuracy	CCM at 5.5 V	-3	0	3	%
Temperature coefficient	600 mA load current	-100	–	100	ppm/°C
Overshoot	Regulator turn on/off, load off, voltage step	–	5	9	%
Voltage dip due to transient	6 mA to 600 mA current step	–	340	500	mV
Voltage spike due to transient	600 mA to 6 mA current step	–	300	500	mV
Settling time		–	–	200	µs

[1]GPIO_1 and GPIO_2 do not support VPH_PWR domain.

Parameter	Test conditions	Min	Typ	Max	Units
Load regulation	Vin < Vout + 1 V with load from Irated/100 to Irated	–	–	3	%
Line regulation	600 mA load current	–	2	2	%/V
Zero-load Idle current		–	0.5	2	mA
Boost output ripple	600 mA load, 20 µF capacitor, 1.6 MHz clock rate	–	–	80	mV
Boost output voltage	8 Ω	4.0	5.0	5.5	V
	4 Ω	4.0	5.0	5.0	V
Boost output voltage step		–	50	–	mV
Boost output current		–	–	900	mA

3.7 General housekeeping

The PMIC includes many circuits that support handset-level housekeeping functions – various tasks that must be performed to keep the handset in order. Integration of these functions reduces the external parts count and the associated size and cost. Housekeeping functions include an analog switch matrix, multiplexers, and voltage scaling; an HK/XO ADC circuit; system clock circuits; a real-time clock for time and alarm functions; and over-temperature protection.

3.7.1 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in Table 3-22.

Table 3-22 Analog multiplexer and scaling functions

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
0	USB_IN pin	0.5–16	1/10	0.05–1.6
1 to 4	RESERVED	–	–	–
5	VCOIN	0.15–3.25	1/3	0.05–1.08
6	VBAT_SNS	2.5–4.5	1/3	0.83–1.5
7	VBAT_VPH_PWR	0.15–1.8	1/3	0.05–0.72
8	DIE_TEMP	0.4–0.9	1/1	0.4–0.9
9	VREF_0P625	0.625	1/1	0.625
10	VREF_1P25	1.25	1/1	1.25
11	CHG_TEMP	0.1–1.7	1/1	0.1–1.7
12	BUFFERED_VREF_0P625	0.625	1/1	0.625
13	RESERVED	–	–	–
14	GND_REF	For calibration	–	–
15	VDD_VADC	For calibration	–	–
16	MPP1	0.1–1.7	1/1	0.1–1.7
17	MPP2	0.1–1.7	1/1	0.1–1.7
18	MPP3	0.1–1.7	1/1	0.1–1.7
19	MPP4	0.1–1.7	1/1	0.1–1.7
20 to 31	RESERVED	–	–	–

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
32	MPP1	0.3–4.5	1/3	0.1–1.7
33	MPP2	0.3–4.5	1/3	0.1–1.7
34	MPP3	0.3–4.5	1/3	0.1–1.7
35	MPP4	0.3–4.5	1/3	0.1–1.7
36 to 47	RESERVED	–	–	–
48	BAT_THERM	0.1–1.7	1/1	0.1–1.7
49	BAT_ID	0.1–1.7	1/1	0.1–1.7
50	XO_THERM without AMUX buffer	0.1–1.7	1/1	0.1–1.7
51 to 53	RESERVED	–	–	–
54	PA_THERM	0.1–1.7	1/1	0.1–1.7
55 to 59	RESERVED	–	–	–
60	XO_THERM through AMUX buffer[1]	0.1–1.7	1/1	0.1–1.7
255	Module power off2	–	–	–

NOTE: Gain and offset errors are different through each analog multiplexer channel. Each path should be calibrated individually over its valid gain and offset settings for best accuracy.

Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 3-23.

Table 3-23 Analog multiplexer performance specifications

Parameter	Comments[3]	Min	Typ	Max	Units
Supply voltage	Connected internally to VREG_L6	–	1.8 V	–	V
Output voltage range Full specification compliance Degraded accuracy at edges		 0.20 0.05	 – –	 VL6 – 0.20 VL6 – 0.05	 V V

[1]These AMUX inputs come from off-chip thermistor circuits.

[2]Channel 32 should be selected when the analog multiplexer is not being used; this prevents the scalers from loading the inputs.

[3]Multiplexer offset error, gain error, and INL are measured as shown in Figure 3-7. Supporting comments:

- The nonlinearity curve is exaggerated for illustrative purposes.
- Input and output voltages must stay within the ranges stated in this table; voltages beyond these ranges result in nonlinearity and are beyond specification.
- Offset is determined by measuring the slope of the endpoint line (m) and calculating its Y-intercept value (b): Offset = b = y1 – m·x1
- Gain error is calculated from the ideal response and the endpoint line as the ratio of their two slopes (in percentage):

  Gain_error = [(slope of endpoint line)/(slope of ideal response) – 1]·100%
- INL is the worst-case deviation from the endpoint line. The endpoint line removes the gain and offset errors to isolate nonlinearity:

  INLmin = min[Vout (actual at Vx input) – Vout (endpoint line at Vx input)]

  INLmax = max[Vout (actual at Vx input) – Vout (endpoint line at Vx input)]

Parameter	Comments[3]	Min	Typ	Max	Units
Input referred offset errors Channels with x1 scaling Channels with 1/3 scaling Channels with 1/4 scaling Channels with 1/6 scaling		 -2.0 -1.5 -3.0 -3.0	 – – – –	 +2.0 +1.5 +3.0 +3.0	 mV mV mV mV
Gain errors, including scaling Channels with x1 scaling Channels with 1/3 scaling Channels with 1/4 scaling Channels with 1/6 scaling	Excludes VREG_L8 output error	 -0.20 -0.15 -0.30 -0.30	 – – – –	 +0.20 +0.15 +0.30 +0.30	 % % % %
Integrated nonlinearity (INL)	Input referred to account for scaling	-3	–	+3	mV
Input resistance Channels with x1 scaling Channels with 1/3 scaling Channels with 1/4 scaling Channels with 1/6 scaling	Input referred to account for scaling	 10 1 0.5 0.5	 – – – –	 – – – –	 MΩ MΩ MΩ MΩ
Channel-to-channel isolation	f = 1 kHz	50	–	–	dB
Output settling time	C_{load} = 65 pF	–	–	25	µs
Output noise level	f = 1 kHz	–	–	2	µV/Hz[1/2]

AMUX input to ADC output end-to-end accuracy specifications are listed in Table 3-24.

[1]The AMUX output and a typical load are modeled in Figure 3-8. After S1 closes, the voltage across C2 settles within the specified settling time.

3.7.2 AMUX input to ADC output end-to-end accuracy

Table 3-24 AMUX input to ADC output end-to-end accuracy

AMUX ch #	Function	Typical input range		Automatic scaling	Typical output range		AMUX input to ADC output end-to-end accuracy, RSS[2,3] (%)				AMUX input to ADC output end-to-end accuracy, WCS[1,4](%)				Recommended method of calibration[1,5] for the channel
							Without calibration		Internal calibration		Without calibration		Internal calibration		
		Min (V)	Max (V)		Min (V)	Max (V)	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	
0	USB_IN pin (divided by 10)	4.35	6.3	1/10	0.435	0.63	4.97	3.92	2.38	2.3	9.59	7.92	3.86	3.46	Absolute
1–4		–	–	–	–	–	–	–	–	–	–	–	–	–	
5	VCOIN pin	2	3.25	1/3	0.67	1.08	3.1	2.2	0.7	0.52	5.7	4.37	1.4	1.08	Absolute
6	VBAT_SNS pin	2.5	4.5	1/3	0.83	1.5	2.64	1.89	0.6	0.47	5.0	3.76	1.24	0.93	Absolute
7	VBAT pin	2.5	4.5	1/3	0.83	1.5	2.64	1.89	0.6	0.47	5.0	3.76	1.24	0.93	Absolute
8	Die-temperature monitor	0.4	0.9	1	0.4	0.9	4.75	2.4	1.0	1.22	8.0	4.7	2.00	1.22	Absolute
9	0.625 V reference voltage	0.625	0.625	1	0.625	0.625	3.27	3.27	0.71	0.71	5.95	5.95	1.47	1.47	Absolute – part of calibration
10	1.25 V reference voltage	1.25	1.25	1	1.25	1.25	2.05	2.05	0.5	0.5	4.08	4.08	1.01	1.01	Absolute – part of calibration
11	Charger temperature	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Absolute
12	VREF_0p625_buf	0.625	0.625	1	0.625	0.625	3.27	3.27	0.71	0.71	5.95	5.95	1.47	1.47	Absolute – part of calibration
13		–	–	–	–	–	–	–	–	–	–	–	–	–	
14–15	GND_REF, VDD_ADC	–	–	–	–	–	–	–	–	–	–	–	–	–	
16–19	MPP_01 to MPP_04 pin	0.1	1.7	1	0.1	1.7	18.00	1.76	4.0	0.47	26.00	3.59	6.00	0.88	Absolute or ratiometric depending on application
20–31		–	–	–	–	–	–	–	–	–	–	–	–	–	

[1]Absolute uses 0.625 V and 1.25 V MBG voltage reference as calibration points. Ratiometric uses the GND_XO and VREF_XO_THM as calibration points.

[2]XO_THERM to ADC output end-to-end accuracy.

[3]The min and max accuracy values correspond to min and max input voltage to the AMUX channel.

[4]Accuracy is based on root sum square (RSS) of the individual errors.

[5]Accuracy is based on worst-case straight sum (WCS) of all errors.

AMUX ch #	Function	Typical input range		Automatic scaling	Typical output range		AMUX input to ADC output end-to-end accuracy, RSS[2,3] (%)				AMUX input to ADC output end-to-end accuracy, WCS[1,4](%)				Recommended method of calibration[1,5] for the channel
							Without calibration		Internal calibration		Without calibration		Internal calibration		
		Min (V)	Max (V)		Min (V)	Max (V)	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	
32–35	MPP_01 to MPP_04 pin	0.3	5.1	1/3	0.1	1.7	18.33	1.78	3.67	0.45	25.67	3.59	6.33	0.9	Absolute or Ratiometric depending on application
36–47		–	–	–	–	–	–	–	–	–	–	–	–	–	
48	BAT_THERM	0.1	1.7	1.0	0.1	1.7	18.42	1.79	3.7	0.46	25.64	3.58	6.22	0.9	Ratiometric
49	BAT_ID	0.1	1.7	1.0	0.1	1.7	18.42	1.79	3.7	0.46	25.64	3.58	6.22	0.9	Ratiometric
50	XO_THERM pin direct[1]	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
51–53		–	–	–	–	–	–	–	–	–	–	–	–	–	
54	PA THERM	0.1	2.0	1.0	0.1	1.7	18.42	1.79	3.7	0.46	25.64	3.58	6.22	0.9	Ratiometric
55–59		–	–	–	–	–	–	–	–	–	–	–	–	–	
60	XO_THERM pin through AMUX	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
255	Module power off	–	–	–	–	–	–	–	–	–	–	–	–	–	

[1]XO_THERM to ADC output end-to-end accuracy.

[2]The min and max accuracy values correspond to min and max input voltage to the AMUX channel.

[3]Accuracy is based on root sum square (RSS) of the individual errors.

[4]Accuracy is based on worst-case straight sum (WCS) of all errors.

[5]Absolute uses 0.625 V and 1.25 V MBG voltage reference as calibration points. Ratiometric uses the GND_XO and VREF_XO_THM as calibration points.

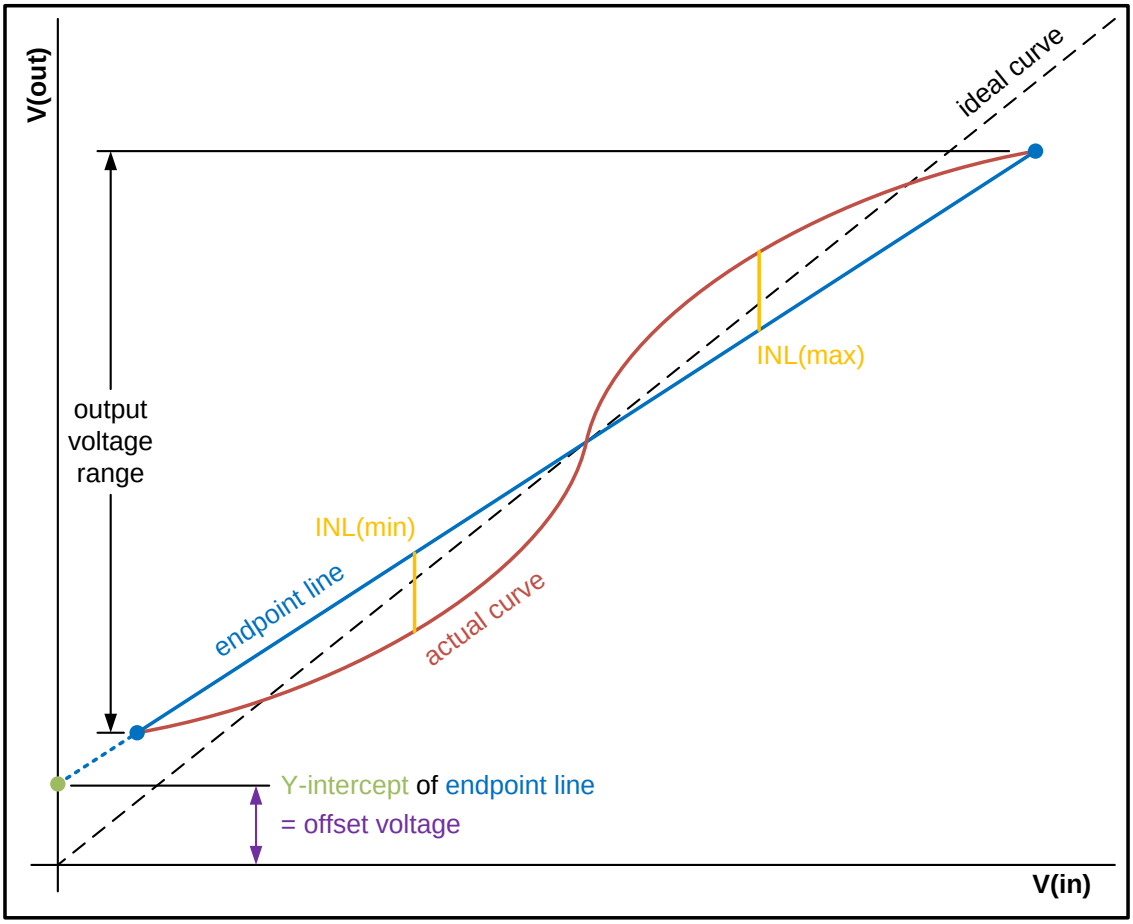


Figure 3-7 Multiplexer offset and gain errors

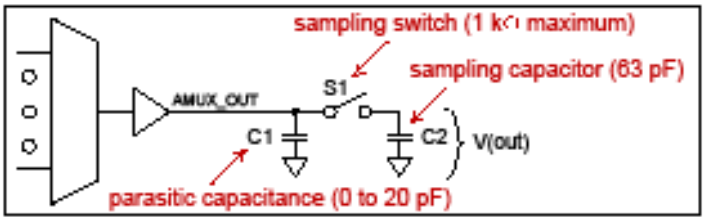


Figure 3-8 Analog-multiplexer load condition for settling time specification

3.7.3 HK/XO ADC circuit

The analog-to-digital converter circuit is shared by the housekeeping (HK) and 19.2 MHz crystal oscillator (XO) functions. A 2:1 analog multiplexer selects which source is applied to the ADC:

- The HK source – the analog multiplexer output discussed in Section 3.7.1; or
- The XO source – the thermistor network output that estimates the 19.2 MHz crystal temperature.

HK/XO ADC performance specifications are listed in Table 3-25.

Table 3-25 HK/XO ADC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage	Connected internally to VREG_L6	–	1.8	–	V
Resolution		–	–	15	bits
Analog input bandwidth		–	100	–	kHz
Sample rate	XO/8	–	2.4	–	MHz
Offset error	Relative to full-scale	-1	–	1	%
Gain error	Relative to full-scale	-1	–	1	%
INL	15-bit output	-8	–	8	LSB
DNL	15-bit output	-4	–	4	LSB

3.7.4 System clocks

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions, and elsewhere within the handset system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an RC oscillator, and sleep clock outputs. Performance specifications for these functions are presented in the following subsections.

3.7.4.1 19.2 MHz XO circuits

An external crystal is supplemented by on-chip circuits to generate the desired 19.2 MHz reference signal. Using an external thermistor network, the on-chip ADC, and advanced temperature-compensation software, the PMIC eliminates the large and expensive VCTCXO module required by previous-generation chipsets. The XO circuits initialize and maintain valid pulse waveforms and measure time intervals for higher-level handset functions. Multiple controllers manage the XO warmup and signal buffering, and generate the desired clock outputs (all derived from one source):

- Low-noise outputs RF_CLKx – enabled internally or can be enabled via properly configured GPIOs.
- Low-power output BB_CLK1 – enabled by the dedicated control pin BB_CLK1_EN; this output is used as the host IC's clock signal.
- Low-power output BB_CLK2 – enabled internally through SPMI or can be enabled through pin control by properly configuring GPIO2.

Since the different controllers and outputs are independent, circuits other than those needed for the WAN can operate even while the host IC is asleep and its RF circuits are powered down.

The XTAL_19M_IN and XTAL_19M_OUT pins are incapable of driving a load – the oscillator will be significantly disrupted if either pin is externally loaded.

As described in Section 3.7.4.3, an RC oscillator is used to drive some clock circuits until the XO source is established.

The 19.2 MHz XO circuit and related performance specifications are listed in Table 3-26.

Table 3-26 XO controller, buffer, and circuit performance specifications

Parameter	Comments	Min	Typ	Max	Units
XO circuits					
Operating frequency	Set by external crystal	–	19.2	–	MHz
Load conditions Capacitance Resistance		 – 1.1	 7.0 –	 – –	 pF kΩ
Startup time When XO is disabled in mission mode When XO is disabled in CalRC mode		 – –	 – –	 10.0 20.0	 ms ms
Supply voltage = VREG_XO	Input buffer and core XO circuits	–	1.8	–	V
Power-supply quiescent current		–	60	–	µA
Low-noise outputs: RF_CLKx					
Voltage swing		1.65	1.8	1.95	Vpp
Duty cycle		48	50	52	%
Buffer output impedance at 1x drive strength at 2x drive strength at 3x drive strength at 4x drive strength		 40 31 24 17	 50 38 28 20	 62 50 36 25	 Ω Ω Ω Ω
Phase noise in NPM at 10 Hz at 100 Hz at 1 kHz at 10 kHz at 100 kHz at 1 MHz		 – – – – – –	 -86 -116 -134 -144 -144 -144	 – – – – – –	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Supply = VREG_RFCLK	Output buffers	–	1.8	–	V
Low-power outputs: BB_CLKx					
Output levels Logic high (V_{OH}) Logic low (V_{OL})		 0.65 x V_{DD} –	 – –	 – 0.35 x V_{DD}	 V V
Output duty cycle		44	50	56	%
USB jitter 0.5 MHz to 2 MHz > 2 MHz	Specified values are peak-to-peak period jitter.	 – –	 – –	 50 100	 ps ps

Parameter	Comments	Min	Typ	Max	Units
Buffer output impedance at 1x drive strength at 2x drive strength at 3x drive strength at 4x drive strength	Current drive capabilities meet the output levels specified above.	 40 31 24 17	 50 38 28 20	 62 50 36 25	 Ω Ω Ω Ω
Supply voltage = VREG_L7	Output buffers	–	1.8	–	V

3.7.4.2 19.2 MHz XO crystal requirements

Crystal performance is critical to a wireless product's overall performance. Guidance is available within *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-V9690-19). This document includes:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
- Discussion of various schematic options

3.7.4.3 RC oscillator

The PMIC includes an on-chip RC oscillator that is used during startup, and as a backup to other oscillators. Pertinent performance specifications are listed in Table 3-27.

Table 3-27 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Oscillation frequency		14	19.2	24	MHz
Duty cycle		30	50	70	%
Divider in SLEEP_CLK path		–	586	–	–
Power-supply current		–	–	80	μA

3.7.4.4 Sleep clock

Source options:

- Calibrated low-frequency RC oscillator.
  - Used as a source of RTC clock when PMIC is off; requires a qualified coin cell or super capacitor to support RTC when the battery is removed.
  - Periodically uses the XO signal for calibration, achieving accuracy suitable for RTC without an external crystal.
- The 19.2 MHz XO divided by 586 (32.7645 kHz nominal) – This is the source of sleep clock and RTC clock when the device is in active and sleep mode.
- The 19.2 MHz RC oscillator divided by 586 (32.7645 kHz nominal) – The 19.2 MHz RC oscillator is an on-chip circuit with coarse frequency accuracy.
  - Used during PMIC power-up until the software switches over to XO/586.
  - Used in active or sleep mode only if other sources are unavailable.

The PMIC sleep-clock output is routed to the host IC via SLEEP_CLK. It is also available for other applications using properly configured GPIOs.

Related specifications presented elsewhere include:

- 19.2 MHz XO circuits (Section 3.7.4.1)
- RC oscillator (Section 3.7.4.3)
- Output characteristics (voltage levels, drive strength, etc.) are defined in Section 3.4.

3.7.5 Real-time clock

The real-time clock (RTC) functions are implemented by a 32-bit real-time counter and one 32-bit alarm, both configurable in one-second increments. The primary input to the RTC circuits is the selected sleep-clock source (calibrated low-frequency oscillator, or divided-down 19.2 MHz XO). Even when the phone is off, the selected oscillator and RTC continue to run off the main battery.

If the main battery is present and an SMPL event occurs, RTC contents are corrupted. As power is restored, the RTC pauses and skips a few seconds. The device must reacquire system time from the network to resume the usual RTC accuracy. Similarly, if the main battery is not present and the voltage at VCOIN drops too low, RTC contents are again corrupted. In either case, the RTC reset interrupt is generated. A different interrupt is generated if the oscillator stops, also causing RTC errors.

If RTC support is needed when the battery is removed, a qualified coin-cell or super capacitor is required on the VCOIN pin of the PMIC. If only SMPL support is needed when the battery is removed, a capacitor with effective capacitance of at least 10 µF is required on the VCOIN pin of the PMIC.

Pertinent RTC specifications are listed in Table 3-28.

Table 3-28 RTC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Tuning resolution	With known calibrated source	–	3.05	–	ppm
Tuning range		-192	–	192	ppm
Accuracy (phone off) XO/586 as RTC source CalRC as RTC source	 Phone on Phone off, valid battery present Phone off, valid coin cell present	 – – –	 – – –	 24 50 200	 ppm ppm ppm

3.7.6 Over-temperature protection (smart thermal control)

The PMIC includes over-temperature protection in stages, depending on the level of urgency as the die temperature rises:

- Stage 0 – normal operating conditions (less than 110°C).
- Stage 1 – 110°C to 130°C; an interrupt is sent to the host IC without shutting down any PMIC circuits.

- Stage 2 – 130°C to 150°C; an interrupt is sent to the host IC and unnecessary high-current circuits are shut down.
- Stage 3 – greater than 150°C; an interrupt is sent to the host IC and the PMIC is completely shut down.

Temperature hysteresis is incorporated such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC will power up immediately.

3.8 User interfaces

In addition to housekeeping functions, the PMIC also includes these circuits in support of common handset-level user interfaces: LED current sinks; and vibration motor driver.

3.8.1 Current drivers

There are three current drivers available:

- Even numbered MPPs can be used as the home row driver or other current sink function
- CHG_LED_SINK to drive LED during charging. This pin cannot be used to drive LED if LBC is not used (OPT_1 is grounded).
- MPPs or GPIOs can be used to control external LED drivers with at least 1 MΩ pull down at the output

3.8.2 Vibration motor driver

The PMIC supports silent incoming-call alarms with its vibration motor driver. The vibration driver is a programmable voltage output that is referenced to VDD; when off, its output voltage is VDD. The motor is connected between VDD and the VIB_DRV_N pin.

Performance specifications for the vibration motor driver circuit are listed in Table 3-29.

Table 3-29 Vibration motor driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Output voltage (V_m) error[1] Relative error Absolute error	VDD > 3.2 V; I_m = 0 to 175 mA; V_m setting = 1.2 to 3.1 V Total error = relative + absolute	 -6 -60	 – –	 6 60	 % mV
Headroom[2]	I_m = 175 mA	–	–	200	mV
Short-circuit current	VIB_DRV_N = VDD	225	–	600	mA

[1]The vibration motor driver circuit is a low-side driver. The motor is connected directly to VDD, and the voltage across the motor is Vm = VDD – Vout, where Vout is the PMIC voltage at VIB_DRV_N.

[2]Adjust the programmed voltage until the lowest motor voltage occurs while still meeting the voltage accuracy specification. This lowest motor voltage (Vm = VDD – Vout) is the headroom.

3.9 IC-level interfaces

The IC-level interfaces include power-on circuits; the SPMI; interrupt managers; and miscellaneous digital I/O functions like level translators, detectors, and controllers. Parameters associated with these IC-level interface functions are specified in the following subsections. GPIO and MPP functions are also considered part of the IC-level interface functional block, but they are specified in their own sections (Section 3.10 and Section 3.11).

3.9.1 Poweron circuits and the power sequences

Dedicated circuits continuously monitor several events that might trigger a poweron sequence, including KPD_PWR_N, CBL_PWR_N, charger insertion, RTC, or SMPL. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the host IC is taken out of reset.

Hardware configuration controls (OPT[2:1]) determine which regulators are included during the initial poweron sequence, as defined in Section 3.9.2. An example sequence will be made available in future revisions of the document.

The I/Os to/from the poweron circuits are basic digital control signals that must meet the voltage-level requirements stated in Section 3.4. The KPD_PWR_N and CBL_PWR_N inputs are pulled up to an internal voltage, dVdd (CBL_PWR_N is internally pulled high to dVdd using additional weak FET). Additional poweron circuit performance specifications are listed in Table 3-30. More complete definitions for time intervals included in this table are provided in the PM8916 *Power Management IC Training Slides* (80-NK808-21).

Table 3-30 Poweron circuit performance specifications

Parameter	Comments	Min	Typ	Max	Units
Internal pull-up resistor	At KPD_PWR_N and CBL_PWR_N pins	–	200	–	kΩ
Sequence time intervals[1]					
t_{reg1}	Poweron event to first regulator on[2]	–	33	–	ms
t_{reset1}	Last default regulator on to PON_RESET_N = H	–	450	–	us
t_{ps_hold}	Time after which PMIC will turn off if PS_HOLD is not driven high by APQ	133.33	200	300	ms
t_{reset0}	PON_RESET_N = L to first regulator off	–	6.4	–	ms
$t_{ps\_hold\_off}$	Delay from PS_HOLD dropping to PON_RESET_N going low	–	175	–	us
Primary PON sequence					
KYPD_PWR_N	Could be any PON trigger	–	0.00	–	ms

[1]Timing is derived from the divided-down XO clock source (32.7645 kHz typical); tolerances are set accordingly.

[2]The first regulator poweron time treg1 depends on the bandgap reference decoupling capacitor at REF_BYP. The specified value is based on 0.1 µF. This time does not include the default 16 ms keypad debounce and the16 ms UVLO debounce timers. If these debounce timers are increased, then the t_{reg1} value will also increase.

Parameter	Comments	Min	Typ	Max	Units
S4	Time from PON trigger to S4 being enabled	–	56.00	–	ms
S3	Time from S4 enable to S3 being enabled	–	4.00	–	ms
L3	Time from S3 enable to L3 being enabled	–	2.40	–	ms
S1	Time from L3 enable to S1 being enabled	–	340.00	–	us
S2	Time from S1 enable to S2 being enabled	–	1.80	–	ms
GPIO4	Time from S2 enable to GPIO4 being enabled	–	1.60	–	ms
MPP1	Time from GPIO4 enable to MPP1 being enabled	–	6.70	–	ms
L5	Time from MPP1 enable to L5 being enabled	–	725.00	–	us
L7	Time from L5 enable to L7 being enabled	–	125.00	–	us
BB_CLK1	Time from L7 enable to BB_CLK1 being enabled	–	25.00	–	ms
L6	Time from L7 enable to L6 being enabled	–	500.00	–	us
L2	Time from L6 enable to L2 being enabled	–	400.00	–	us
L13	Time from L2 enable to L13 being enabled	–	220.00	–	ms
L8	Time from L13 enable to L8 being enabled	–	350.00	–	us
L12	Time from L8 trigger to L12 being enabled	–	350.00	–	us
L11	Time from L12 trigger to L11 being enabled	–	350.00	–	us
PON_RESET_N	Time from L11 enable to PON_RESET_N going high	–	t_{reset1}	–	ms
PS_HOLD	Time from PON_RESET_N high to PS_HOLD going high	–	t_{ps_hold}	–	ms

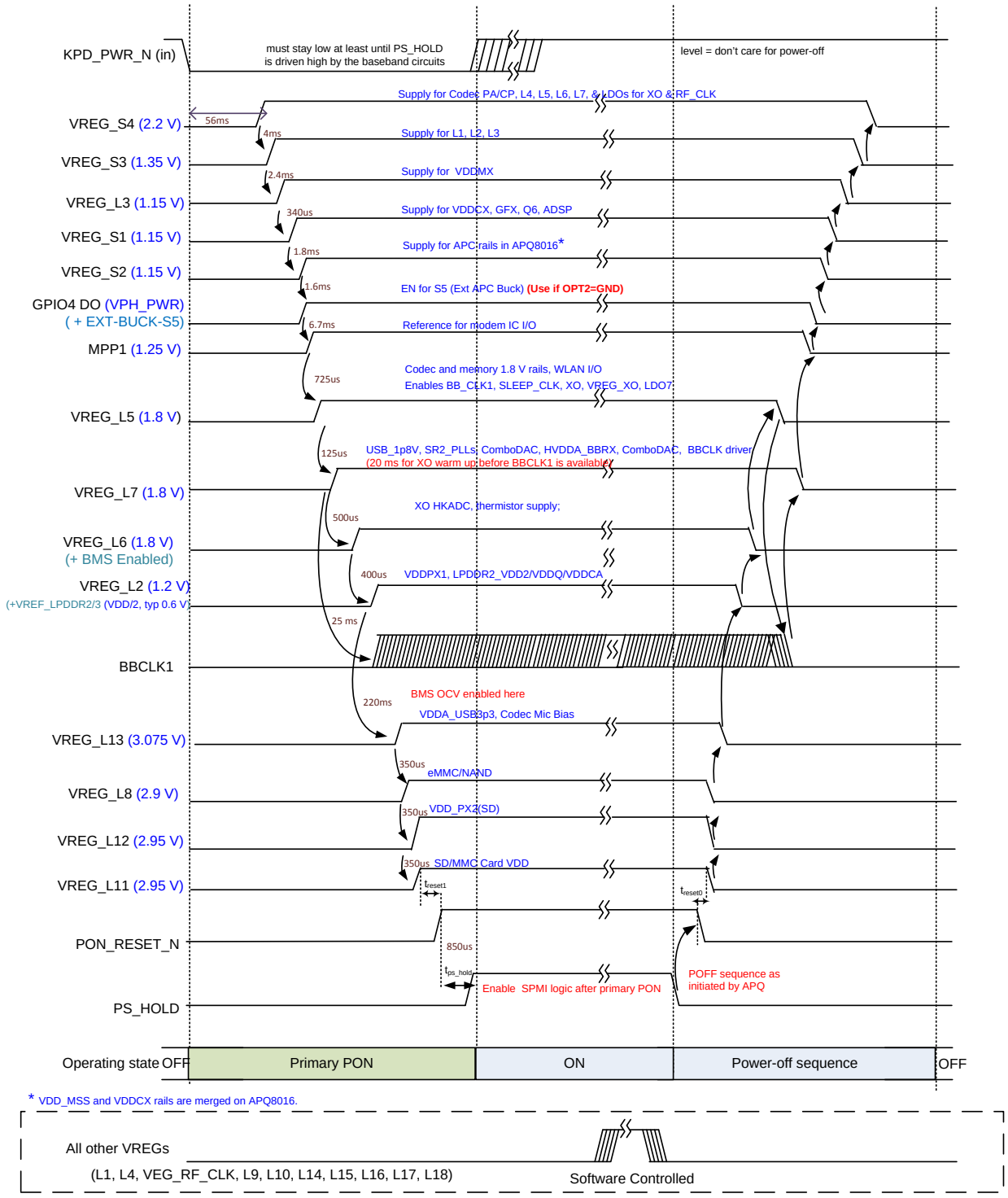


Figure 3-9 Poweron sequence for BB code '01' and '02'

NOTE: For default voltage levels of PM8916 and PM8916-1 during PON sequence see Table 3-13.

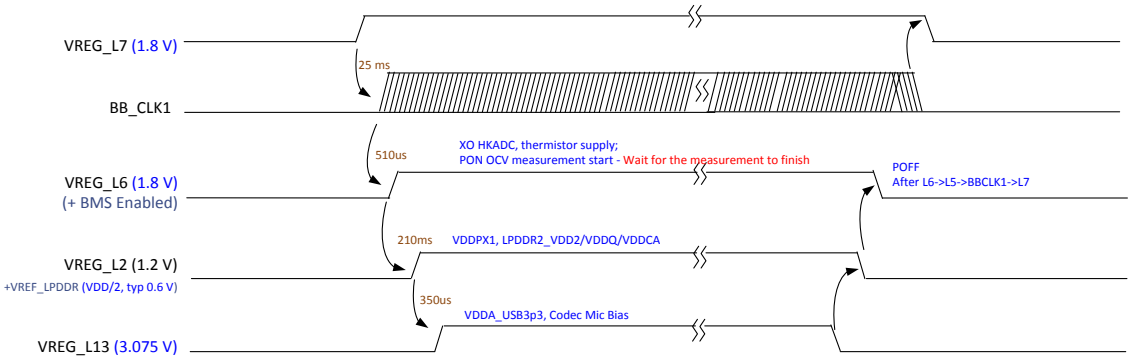


Figure 3-10 Poweron sequence for BB code 'VV'

3.9.2 OPT[2:1] hardwired controls

Two pins (OPT_1 and OPT_2) can be used to configure PON parameters. The usable configurations are shown in Table 3-31.

Table 3-31 OPT_1 and OPT_2 PON parameters

Pins	Hi-Z	GND
OPT_1	External charger not present	External charger present
OPT_2	External APC buck (S5) not present	External APC busk (S5) present

Each OPT combination results in a unique set of poweron parameters: which regulators default on at powerup, the order those regulators are turned on, the voltage settings of some of those regulators, and whether external regulators are turned on via MPP or GPIO controls during the poweron sequence. In essence, the OPT combination customizes the poweron sequence for each chipset.

NOTE: Connecting either of these pins to VDD will force the PMIC to shut down.

3.9.3 SPMI and the interrupt managers

The SPMI is a bidirectional, two-line digital interface that meets the voltage- and current-level requirements stated in Section 3.4.

PMIC interrupt managers support the chipset host and its processors, and communicate with the host IC via SPMI. Since the interrupt managers are entirely embedded functions, additional performance specifications are not required.

3.10 General-purpose input/output specifications

The four general-purpose input/output (GPIO) ports are digital I/Os that can be programmed for a variety of configurations (Table 3-32). Performance specifications for the different configurations are included in Section 3.4.

NOTE: Unused GPIO pins should be configured as inputs with 10 µA pulldown.

Table 3-32 Programmable GPIO configurations

Configuration type	Configuration description
Input	1. No pullup 2. Pullup (1.5, 30, or 31.5 μA) 3. Pulldown (10 μA) 4. Keeper
Output	Open-drain or CMOS Inverted or non-inverted Programmable drive current; see Table 3-33 for options
Input/output pair	Requires two GPIOs. Input and output stages can use different power supplies, thereby implementing a level translator. See Table 3-33 for supply options.

GPIOs default to digital input with 10 uA pulldown at poweron. During poweron (OPT2 = GND), PBS programs GPIO_4 as digital output high at VDD level to enable the external buck converter. Before they can be used for their desired purposes, they need to be reconfigured appropriately.

GPIO_4 can also be used as SLEEP_CLK output special function if OPT2 is not grounded.

GPIO_2 can be used to pin control BB_CLK2 output by configuring it appropriately.

GPIO_1 and GPIO_2 do not support VPH_PWR domain.

GPIOs are designed to run at a 4 MHz rate to support high-speed applications (only GPIO1 and GPIO2 are GPIOC capable). The supported rate depends on the load capacitance and IR drop requirements. If the application specifies load capacitance, then the maximum rate is determined by the IR drop. If the application does not require a specific IR drop, then the maximum rate can be increased by increasing the supply voltage and adjusting the drive strength according to the actual load capacitance. Table 3-33 lists output voltages for different driver strengths.

Table 3-33 VOL and VOH for different driver strengths

Supply voltage	VOL, VOH	Minimum load current		
		Low-strength driver	Medium-strength driver	High-strength driver
1.8 V	VOH = VDD – 0.3 V = 1.5 V VOL = 0.3 V	0.15 mA	0.6 mA	0.9 mA
2.6 V	VOH = VDD – 0.45 V = 2.15 V VOL = 0.45 V	0.3 mA	1.25 mA	1.9 mA
2.85 V	VOH = VDD – 0.4 V = 2.45 V VOL = 0.4 V	0.3 mA	1.1 mA	1.7 mA
3.3 V	VOH = VDD – 0.45 V = 2.85 V VOL = 0.45 V	0.39 mA	1.4 mA	2.1 mA

3.11 Multipurpose pin specifications

The PM8916 includes four multipurpose pins (MPPs), and they can be configured for any of the functions specified within Table 3-34. All MPPs are high-Z at poweron. During poweron, PBS programs MPP_1 as analog output, which is used as a reference for host IC.

Table 3-34 Multipurpose pin performance specifications

Parameter	Comments	Min	Typ	Max	Units
MPP configured as digital input[1]					
Logic high input voltage		0.65 * V_M	–	–	V
Logic low input voltage		–	–	0.35 * V_M	V
MPP configured as digital output[1]					
Logic high output voltage	Iout = IOH	V_M – 0.45	–	V_M	V
Logic low output voltage	Iout = IOL	0	–	0.45	V
MPP configured as analog input (analog multiplexer input)					
Input current		–	–	100	nA
Input capacitance		–	–	10	pF
MPP configured as analog output (buffered VREF output)[2]					
Output voltage error	-50 µA to +50 µA	–	–	12.5	mV
Temperature variation	Due to buffer only; does not include VREF variation (see Table 3-17)	-0.03	–	0.03	%
Load capacitance		–	–	25	pF
Power-supply current		–	0.17	0.2	mA
MPP configured as current sink[2]					
Power supply voltage		–	VDD	–	V
Sink current	Programmable in 5 mA increment	0		40	mA
Sink current accuracy	VOUT = 0.7 V to (VDD – 1 V)	-20		+20	%
Power-supply current			105	115	µA
MPP configured as level translator					
Maximum frequency		4	–	–	MHz

3.12 Audio codec

NOTE: All audio performance data are collected above PMIC Vbatt of 3.4 V, unless otherwise specified.

[1]Input and output stages can use different power supplies, thereby implementing a level translator. See Table 2-1 for V_M supply options. Other specifications are included in Section 3.4.

[2]Only even MPPs (MPP_2 and MPP_4) can be configured as current sink and only odd MPPs (MPP_1 and MPP_3) can be configured as analog output.

3.12.1 Audio inputs and Tx processing

Table 3-35 Analog microphone input performance

Parameter	Test conditions	Min	Typ	Max	Units
Microphone amplifier gain = 0 dB (minimum gain)					
Input referred noise	Single-ended, A-weighted, capless	–	18.5	25.1	µVrms
Signal to noise ratio	Single-ended, A-weighted, capless	92.0	94.0	–	dB
THD+N ratio	f = 1.02 kHz; single-ended input; bandwidth 200 Hz to 20 kHz, capless Analog input = -1 dBV Analog input = -60 dBV, A-weighted	 – –	 -83.0 -35.0	 -70.0 -32.0	 dB dB
Microphone amplifier gain = 6 dB					
Input referred noise	Single-ended, A-weighted, capless	–	10.0	13.0	µVrms
Signal to noise ratio	Single-ended, A-weighted, capless	91.0	94.0	–	dB
THD+N	f = 1.02 kHz; single-ended input; bandwidth 200 Hz to 20 kHz, capless Analog input = -1 dBV Analog input = -60 dBV, A-weighted	 – –	 -82.5 -34.0	 -70.0 -30.0	 dB dB
Microphone amplifier gain = 12 dB (typical gain)					
Input referred noise	Single-ended, A-weighted, capless	–	5.5	7.1	µVrms
Signal to noise ratio	Single-ended, A-weighted, capless	91.0	93.5	–	dB
THD+N	f = 1.02 kHz; single-ended input; bandwidth 200 Hz to 20 kHz, capless Analog input = -1 dBV Analog input = -60 dBV, A-weighted	 – –	 -83.0 -33.5	 -70.0 -30.0	 dB dB
Microphone amplifier gain = 18 dB					
Input referred noise	Single-ended, A-weighted, capless	–	3.5	6.3	µVrms
Signal to noise ratio	Single-ended, A-weighted, capless	87	91.0	–	dB
THD+N	f = 1.02 kHz; single-ended input; bandwidth 200 Hz to 20 kHz, capless Analog input = -1 dBV Analog input = -60 dBV, A-weighted	 – –	 -82.0 -31.0	 -70.0 -28.0	 dB dB
Microphone amplifier gain = 21 dB					
Input referred noise	Single-ended, A-weighted, capless	–	2.8	4.2	µVrms
Signal to noise ratio	Single-ended A-weighted, capless	85.0	89.0	–	dB
THD+N	f = 1.02 kHz; single-ended input; bandwidth 200 Hz to 20 kHz, capless Analog input = -1 dBV Analog input = -60 dBV A-weighted	 – –	 -81.5 -28.5	 -70.0 -25.0	 dB dB
Microphone amplifier gain = 24 dB (maximum gain)					
Input referred noise	Single-ended A-weighted, capless	–	2.6	4.2	µVrms
Signal to noise ratio	Single-ended A-weighted, capless	84.0	87.5	–	dB

Parameter	Test conditions	Min	Typ	Max	Units
THD+N	f = 1.02 kHz; single-ended input; bandwidth 200 Hz to 20 kHz, capless				
	Analog input = -1 dBV	–	-82.0	-60.0	dB
	Analog input = -60 dBV A-weighted	–	-26.0	-22.0	dB
Frequency response (from mic input to PCM all sample rates)					
Frequency response	Digital gain = 0 dB; analog gain = 0 dB; Analog input = -20 dBV				
	Passband: 20 Hz to 200 Hz	-0.05	0	0.05	dB
	Passband: 200 Hz to 0.4 * Fs	-0.05	0	0.05	dB
	Transition band 1 at 0.4375 * Fs	-1.5	-0.7	0.5	dB
	Transition band 2 at 0.499 * Fs	–	-25.0	-24.0	dB
	Stopband at 0.5625 * Fs	–	-75.0	-70.0	dB
General requirements					
Absolute gain error	Analog input = -20 dBV, 1.02 kHz	-20.5	-20.0	-19.5	dB
Full-scale input voltage	Single-ended 1 kHz input. Input signal level required to get 0 dBFS digital output	-0.5	0	0.5	dBV
Power supply rejection (1.8 V)	100 mVpp square wave imposed on the PMIC Vbatt input; analog input = 0 Vrms, terminated with 0 Ω; keep the bypass capacitors on power pins and measure 100 mV ripple at the power pins				
	0 < f < 1 kHz	75.0	86.0	–	dB
	1< f < 5 kHz	75.0	82.0	–	dB
	f > 5 kHz	60.0	70.0	–	dB
Intermodulation distortion (IMD2)	Analog input = 12993 Hz and 14993 Hz equal amplitude tones at -6 dBV; wideband (WB) audio	65.0	85.0	–	dB
	Analog input = 41 Hz and 7993 Hz equal amplitude tones at -6 dBV, WB voice	50.0	90.0	–	dB
	Analog input = 498 Hz and 2020 Hz equal amplitude tones at -6 dBV, narrowband (NB) voice	60.0	90.0	–	dB
Input impedance	Capless input	1.0	–	–	MΩ
	Input disabled	3.0	–	–	MΩ
Input capacitance	Capless input	–	–	15.0	pF
Rx →Tx crosstalk attenuation	Tx path measurement with -5 dBV Rx path signal; f = 1 kHz, 10 kHz, and 20 kHz	80.0	97.0	–	dB
Inter-channel isolation	20 < f < 20 kHz, one input terminated with 1 kΩ and the other input gets 1 kHz at -5 dBV; measure the digital output of the terminated channel	90.0	100.0	–	dB

3.12.2 Audio outputs and Rx processing

Table 3-36 Ear output performance, 32 Ω load unless specified

Parameter	Test conditions	Min	Typ	Max	Units
EAR: 8 kHz, 16 bits					
Receive noise	A-weighted; input = -999 dBFS, 6 dB gain mode	–	7.8	16.0	µVrms
	A-weighted; input = -999 dBFS, 1.5 dB gain mode	–	5.8	12.0	µVrms
Signal to noise ratio	Ratio of full scale output to output noise level, VDD_EAR_SPKR = 3.7 V or 5 V, 1.5 dB gain mode	102.0	108.0	–	dB
	Ratio of full scale output to output noise level, VDD_EAR_SPKR = 3.7 V or 5 V, 6 dB gain mode	100.0	106.0	–	dB
THD+N	PCMI = -1 dBFS (band limited from 200 Hz to 20 kHz), VDD_EAR_SPKR = 3.7 V or 5 V	–	-80.0	-70.0	dB
	PCMI = -60 dBFS (band limited from 200 Hz to 20 kHz), VDD_EAR_SPKR = 3.7 V or 5 V, A-weighted	–	-34.5	-31.0	dB
EAR: 16 kHz, 16 bits					
Receive noise	A-weighted; input = -999 dBFS, 6 dB gain mode	–	7.8	16.0	µVrms
	A-weighted; input = -999 dBFS, 1.5 dB gain mode	–	5.8	12.0	µVrms
Signal to noise ratio	Ratio of full scale output to output noise level, VDD_EAR_SPKR = 3.7 V or 5 V, 1.5 dB gain	102.0	108.0	–	dB
	Ratio of full scale output to output noise level, VDD_EAR_SPKR = 3.7 V or 5 V, 6 dB gain mode	100.0	106.0	–	dB
THD+N	PCMI = -1 dBFS (band limited from 200 Hz to 20 kHz), VDD_EAR_SPKR = 3.7 V or 5 V	–	-74.0	-70.0	dB
	PCMI = -60 dBFS (band limited from 200 Hz to 20 kHz), VDD_EAR_SPKR = 3.7 V or 5 V, A-weighted	–	-34.5	-31.0	dB
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 6 dB gain mode	1.8	2.0	2.1	Vrms
	f = 1.02 kHz, 1.5 dB gain mode	1.0	1.2	1.3	Vrms
DAC full-scale output		–	–	1.0	Vrms
Output power	f = 1.02 kHz, 6 dB gain mode, 32 Ω, THD+N <1%	120.0	124.5	–	mW
	f = 1.02 kHz, 6 dB gain mode, 16 Ω THD+N < 1%	235.0	243.0	–	mW
	f = 1.02 kHz, 6 dB gain mode, 10.67 Ω THD+N < 1%	310.0	320.0	–	mW
Output load		10.7	32.0	50000	□
Output capacitance	Total capacitance between EARO_P and EARO_M, including PCB capacitance and EMI	–	–	500	pF
Tx → Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal; f = 1 kHz	90.0	100.0	–	dB
Power supply rejection	0 < f < 1 kHz; 100 mVpp sine wave imposed on VDD_EAR_SPKR; PCMI = -999 dBFS, 6 dB gain mode	70.0	90.0	–	dB
	1 kHz < f < 5 kHz; 100 mVpp sine wave imposed on VDD_EAR_SPKR; PCMI = -999 dBFS, 6 dB gain mode	60.0	82.0	–	dB
	5 kHz < f < 20 kHz; 100 mVpp sine wave imposed on VDD_EAR_SPKR; PCMI = -999 dBFS, 6 dB gain mode	50.0	78.0	–	dB
Disabled output impedance	Measured externally, with amplifier disabled	1.0	–	–	M □

Parameter	Test conditions	Min	Typ	Max	Units
Output common mode voltage	Measured externally, with amplifier disabled	1.52	1.60	1.68	V
Output DC offset		0	0.135	3.0	mV
Turn on/off click and pop level	A-weighted	–	-66.0	-54.0	dBVpp

Table 3-37 HPH output performance, 16 Ω load unless specified

Parameter	Test conditions	Min	Typ	Max	Units
HPH: 8 kHz, 16 bits					
Receive noise	A-weighted; input = -999 dBFS, VDD_CP = 1.9 V	–	4.7	6.5	µVrms
Signal to noise ratio	Ratio of full scale output to output noise level, VDD_CP = 1.9 V	99.0	102.5	–	dB
THD+N	PCMI = -1 dBFS (band limited from 200 Hz to 20 kHz), VDD_CP = 1.9 V	–	-80.0	-70.0	dB
	PCMI = -60 dBFS (band limited from 200 Hz to 20 kHz), VDD_CP = 1.9 V, A-weighted	–	-35.0	-31.0	dB
HPH: 48 kHz, 16 bits					
Receive noise	A-weighted; input = -999 dBFS, VDD_CP = 1.9 V	–	4.7	6.5	µVrms
Signal to noise ratio	Ratio of full scale output to output noise level, VDD_CP = 1.9 V	99.0	102.5	–	dB
THD+N	PCMI = -1 dBFS (band limited from 200 Hz to 20 kHz), VDD_CP = 1.9 V	–	-88.0	-75.0	dB
	PCMI = -60 dBFS (band limited from 200 Hz to 20 kHz), VDD_CP = 1.9 V or, A-weighted	–	-36.0	-32.0	dB
HPH: 48 kHz, 24 bits					
Receive noise	A-weighted; input = -999 dBFS, VDD_CP = 1.9 V	–	4.7	6.5	µVrms
Signal to noise ratio	Ratio of full scale output to output noise level, VDD_CP = 1.9 V	99.0	102.5	–	dB
THD+N	PCMI = -1 dBFS (band limited from 200 Hz to 20 kHz), VDD_CP = 1.9 V	–	-89.0	-80.0	dB
	PCMI = -60 dBFS (band limited from 200 Hz to 20 kHz), VDD_CP = 1.9 V, A-weighted	–	-43.0	-40.0	dB
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 0 dB FS; 16 Ω load; VDD_CP = 1.9 V	0.50	0.59	0.64	Vrms
	f = 1.02 kHz, 0 dB FS; 32 Ω load; VDD_CP = 1.9 V	0.96	0.99	1.00	Vrms
DAC full-scale output		–	–	1.00	Vrms
Output power	f = 1.02 kHz, 16 Ω load; VDD_CP = 1.9 V	15.6	21.5	25.6	mW
	f = 1.02 kHz, 32 Ω load; VDD_CP = 1.9 V	27.0	30.8	32.0	mW
Output load	0 dBV maximum output	26	32	50000	Ω
	-4.5 dBV maximum output	13	16	50000	Ω

Parameter	Test conditions	Min	Typ	Max	Units
Output capacitance	Total capacitance on HPH output (single-ended), including PCB capacitance and EMI	–	–	1000	pF
Tx → Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal. f = 1 kHz	90.0	100.0	–	dB
Inter-channel isolation (separate GND for HPH_L & R)	20 < f < 20 kHz, measured channel output = -999 dBFS, second DAC channel output = -5 dBFS	90.0	97.0	–	dB
Inter-channel gain error	Delta between left and right channels, input = 1 kHz at -20 dBFS	–	0.03	0.30	dB
Inter-channel phase error	Delta between left and right channels, input = 1 kHz at -20 dBFS	–	0.07	0.50	deg
Power supply rejection	0 < f < 20 kHz; 100 mVpp sine wave imposed on VPH_PWR; PCMI = -999 dBFS	80.0	90.9	–	dB
Intermodulation distortion (IMD2)	Digital input = 12993 Hz and 14993 Hz equal amplitude tones at -6 dBFS	70.0	81.0	–	dB
	Digital input = 41 Hz and 7993 Hz equal amplitude tones at -6 dBFS	65.0	75.0	–	dB
	Analog input = 498 Hz and 2020 Hz equal amplitude tones at -6 dBFS	70.0	77.0	–	dB
Disabled output impedance	Measured externally, with amplifier disabled	1.0	–	–	MΩ
Output DC offset	Input = -999 dBFS	0	0.1	1.5	mV
Turn on/off click and pop level	A-weighted, 16 Ω or 32 Ω	–	-81.0	-62.0	dBVpp

Table 3-38 Mono speaker driver outputs performance, 8 Ω load and + 12 dB gain unless otherwise specified

Parameter	Test conditions	Min	Typ	Max	Units
SPKR_DRV; 48 kHz, 16 bits					
Receive noise	A-weighted; input = -999 dBFS, VDD_EAR_SPKR = 5 V	–	50.0	100.0	µVrms
THD+N	Pout = 1.5 W, 1 kHz, VDD_EAR_SPKR = 5.5 V	_	-86.5	-80.0	dB
	Pout = 1.2 W, 1 kHz, VDD_EAR_SPKR = 5 V	_	-86.0	-80.0	dB
	Pout = 1 W, 1 kHz, VDD_EAR_SPKR = 4.2 V	_	-36.0	-20.0	dB
	Pout = 850 mW, 1 kHz, VDD_EAR_SPKR = 4.2 V	_	-78.0	-40.0	dB
	Pout = 700 mW, 1 kHz, VDD_EAR_SPKR = 3.8 V	_	-76.0	-40.0	dB
	Pout = 250 mW 1 kHz, VDD_EAR_SPKR = 3.4 V	_	-77.0	-40.0	dB

Parameter	Test conditions	Min	Typ	Max	Units
Other characteristics					
DAC full-scale output		–	–	1	Vrms
Level translation	f = 1 kHz, gain = 12 dB				
	Input = -3 dBFS, VDD_EAR_SPKR = 3.7 V	7.3	8.9	9.5	dBV
	Input = -1.5 dBFS, VDD_EAR_SPKR = 5.5 V	9.2	10.4	11.5	dBV
Output power (Pout)	f = 1 kHz				
	Vdd = 3.6 V THD + N ≤ 1%; 15 µH + 8 Ω + 15 µH	670	690	–	mW
	Vdd = 3.6 V THD + N ≤ 1%; 15 µH + 4 Ω + 15 µH	900	1100	–	mW
	Vdd = 3.8 V THD + N ≤ 1%; 15 µH + 8 Ω + 15 µH	698	720	–	mW
	Vdd = 4.2 V THD + N ≤ 1%; 15 µH + 8 Ω + 15 µH	929	956	–	mW
	Vdd = 5 V THD+N ≤1%; 15 µH + 8 Ω + 15 µH	1200	1500	–	mW
	Vdd = 5 V THD+N ≤1%; 15 µH + 4 Ω + 15 µH	1500	2000	–	mW
Power supply rejection	200 mVpp sine wave imposed on PMIC_BATT; digital input = -999 dBFS[1]				
	f = 217 Hz	60.0	79.0	–	dB
	f = 1 kHz	60.0	79.0	–	dB
	f = 10 kHz	40.0	50.0		
	f = 20 kHz	40.0	50.0	–	dB
Output DC offset	Speaker driver enabled, input = -999 dBFS	-3.0	0.20	3.0	mV
Efficiency	Vdd = 3.7 V Pout = 500 mW; 15 µH + 8 Ω + 15 µH Pout = 1 W; 15 µH + 4 Ω + 15 µH	 85 78	 90 85	 – –	 % %
	Vdd = 5 V Pout = 1 W, 115 µH + 8 Ω + 15 µH Pout = 2 W, 15 µH + 4 Ω + 15 µH	 73 61	 81 72	 – –	 % %
Shutdown current	Amplifier disabled	–	0.1	1	µA
Turn on time		–	0.2	10	ms
Click and pop	No signal, turn on/off, mute/unmute, A-weighted	–	0.6	10	mVpp
Disabled output impedance		25	–	–	kΩ
Load capacitance		–	–	–	pF
VDD/GND inductance	Vdd = 5.5 V, square wave, 20 Hz to 20 kHz, 40 hours	–	–	0.5[2]	nH

[1]With 200 mVpp sine wave imposed on VSW_BOOST and digital input = -999 dBFS, PSRR is higher than 90 dB typical for all test cases

[2]Bypass capacitors should be placed after the series ferrite bead at the amplifier's output. Having a capacitor directly at the speaker-driver output reduces class-D efficiency and increases power consumption

3.12.3 Support circuits

Table 3-39 Microphone bias specifications

Parameter	Test conditions	Min	Typ	Max	Units
Output voltage	3 mA microphone load	1.6	–	2.85	V
Output voltage accuracy		-3		+3	%
Output current	Two microphone loads of 1 to 1.5 mA each	2.0	3.0	–	mA
Output switch to ground	On resistance	–	–	20	Ω
	Sink current	2.0	–	–	mA
Output noise	0.1 µF bypass	0.0	2.4	3.0	µVrms
Power supply rejection	100 mVpp applied to PMIC Vbatt input at 20 Hz at 200 Hz to 1 kHz at 5 Hz at 10 kHz at 20 kHz	 90 90 90 90 85	 – – – – –	 – – – – –	 dB dB dB dB dB
Inter-mic isolation	DC current = 50 µA, 2.2 kΩ bias resistor; 20 Hz to 200 Hz 200 Hz to 1 kHz 1 kHz to 2 kHz 2 kHz to 5 kHz 5 kHz to 10 kHz 10 kHz to 20 kHz 20 kHz to 80 kHz	 70.0 67.0 67.0 65.0 60.0 54.0 32.0	 72.6 72.6 72.0 70.9 69.2 66.4 –	 – – – – – – –	 dB dB dB dB dB dB dB
Output capacitor value	External bypass mode	0.1	0.1	0.5	µF
	No external bypass mode	–	–	270	pF

4 Mechanical Information

4.1 Device physical dimensions

The PM8916 is available in the 176-pin nanoscale package (176 NSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 176 NSP has a 6.2 × 6.2 mm body with a maximum height of 0.86 mm. Pin 1 is located by an indicator mark on the top of the package. Figure 4-1 shows a simplified version of the 176 NSP outline drawing.

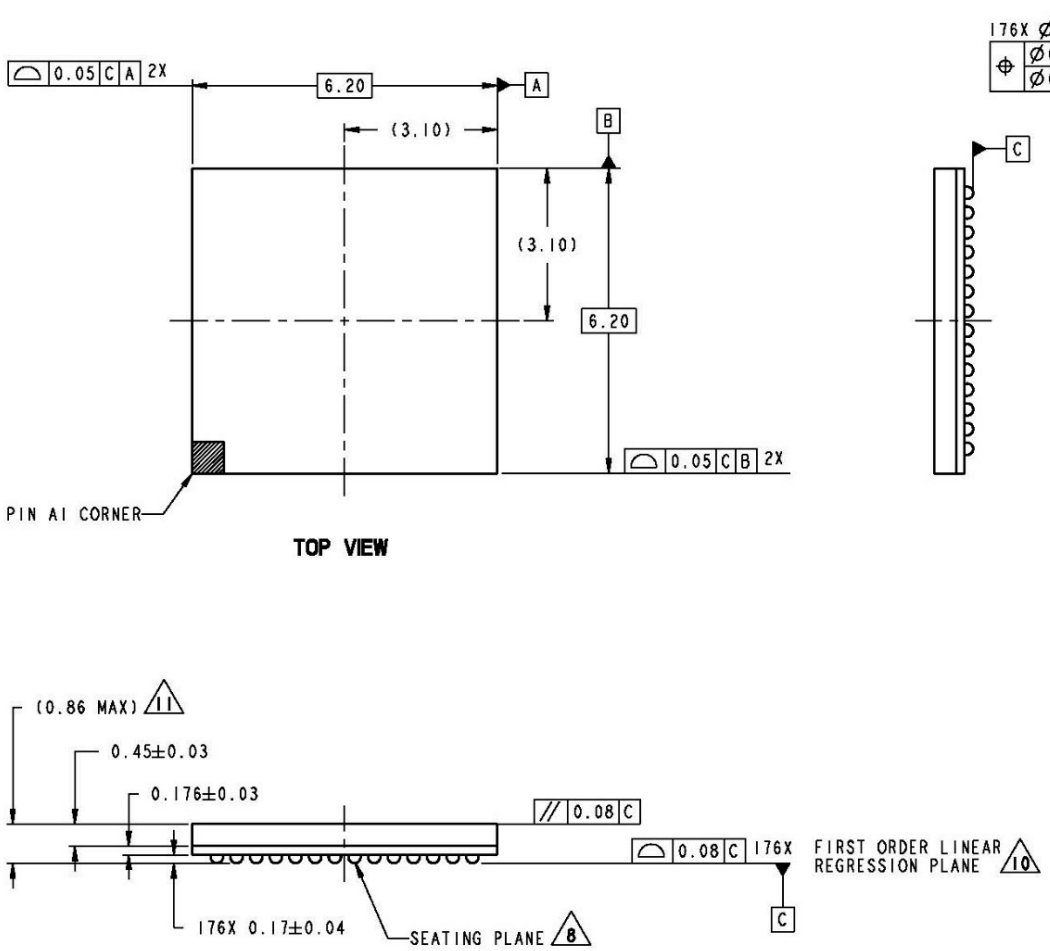


Figure 4-1 6.2 x 6.2 x 0.86 mm outline drawing

This is a simplified outline drawing.

4.2 Part marking

4.2.1 Specification-compliant devices

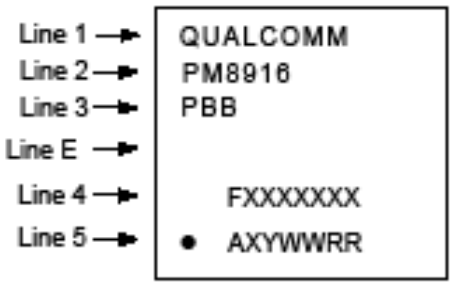


Figure 4-2 PM8916 device marking (top view, not to scale)

Table 4-1 PM8916 device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm® name or logo
2	PM8916	Qualcomm Technologies Inc. (QTI) product name
3	PBB	P = product configuration code See Table 4-2 for assigned values. BB = feature code See Table 4-2 for assigned values.
E	Blank or random	Additional content as necessary
4	FXXXXXXX	F = supply source code F = A: SMIC F = B: TSMC XXXXXXX = traceability information
5	AXYWWRR	A = assembly site code A = U: Amkor, China A = V: StatsChipPAC, China A = E: ASE, Taiwan A = K: SPIL, Taiwan X = Traceability information YWW = Date code RR = product revision See Table 4-2 for assigned values. • = dot identifying pin 1

For complete marking definitions of all PM8916 variants and revisions, refer to *PM8916/PM8916-1 Device Revision Guide* (LM80-P0436-34).

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

Device ID code ►	AA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	PM-8916	— 0	— 176	NSP	— TR	— 02	— 0	— VV
Feature code (BB) may not be included when identifying older devices. ↗								

Figure 4-3 Device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 PM8916 device identification details

PM8916 variant		Product configuration code (*P*)[1]	Product revision (*RR*)	Feature code *BB* value[2]	S value[3]	Hardware revision	Date code (YWW)
PM8916	ES1	0	01	VV	0	v1.1	≤ 418
PM8916	ES2	0	02	VV	0	v2.0	419 to 425
PM8916	CS1	0	02	VV	0	v2.0	≥ 420[4]
PM8916	CS2	0	02	01	1	v2.0.1	NA
PM8916-1	CS3	1	02	02	1	v2.0.1	NA

Table 4-3 Feature codes

BB value	Feature description
VV	PON sequence – VM-BMS OCV measurement is enabled after L6 power on.
01 & 02	PON sequence – VM-BMS OCV measurement is enabled after L2 power on.

[1] P code 0 will be called PM8916 and is integrated with the APQ8016 platform.
P code 1 will be called PM8916-1 and is integrated with the APQ8009 platform.

[2] "BB" is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants.

[3] "S" is the source configuration code that identifies all of the qualified die fabrication-source combinations available at the time a particular sample type was shipped.

[4] For date codes 420–425, contact your customer service team.

Table 4-4 Source configuration code

S value	Die	F value = TBD	F value = TBD	F value = TBD	F value = TBD
0	CMOS	TBD	–	–	–
Other columns and rows will be added in future revisions of this document if needed.					

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The PM8916 devices are classified as MSL3 at 250ºC. This is the MSL classification temperature, which is defined as the minimum temperature of moisture sensitivity testing during device qualification.

Additional MSL information is included in:

Section 5.2 – Storage

Section 5.3 – Handling

Section 7.1 – Reliability qualifications summary

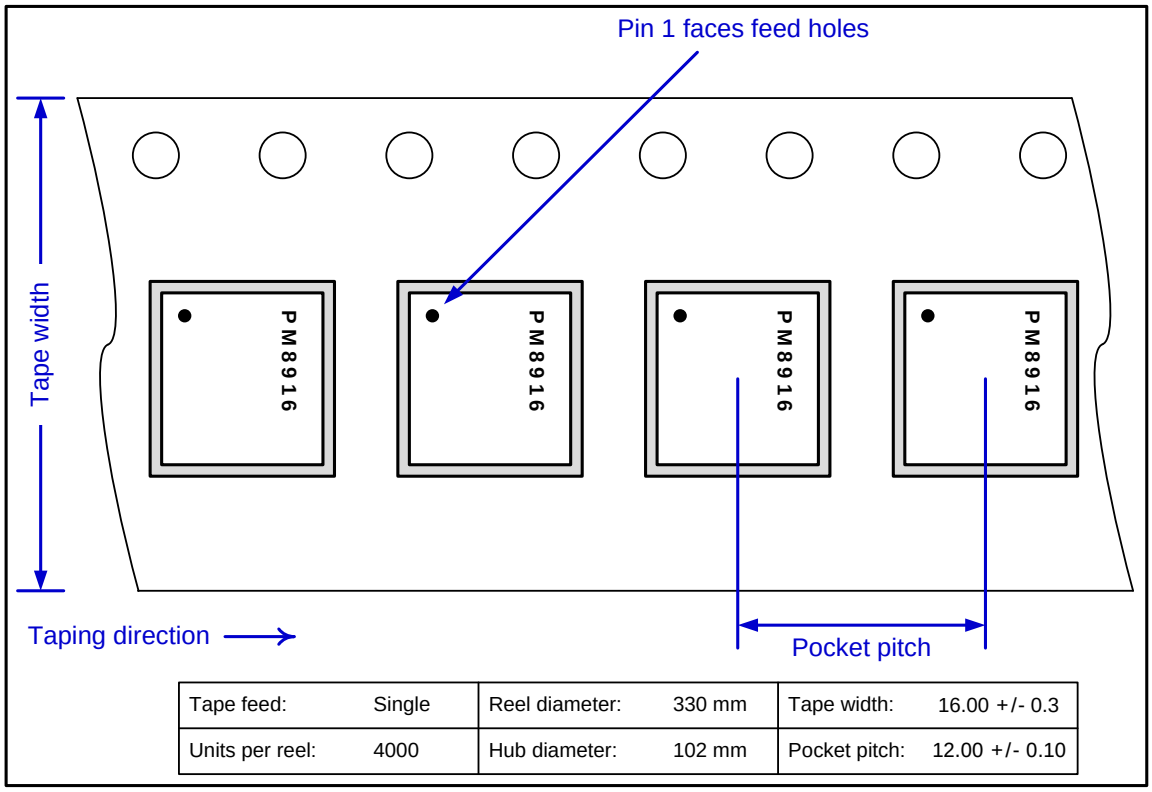
5 Carrier, Storage, and Handling Information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards.

A simplified sketch of the PM8916 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	16.00 +/- 0.3
Units per reel:	4000	Hub diameter:	102 mm	Pocket pitch:	12.00 +/- 0.10

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

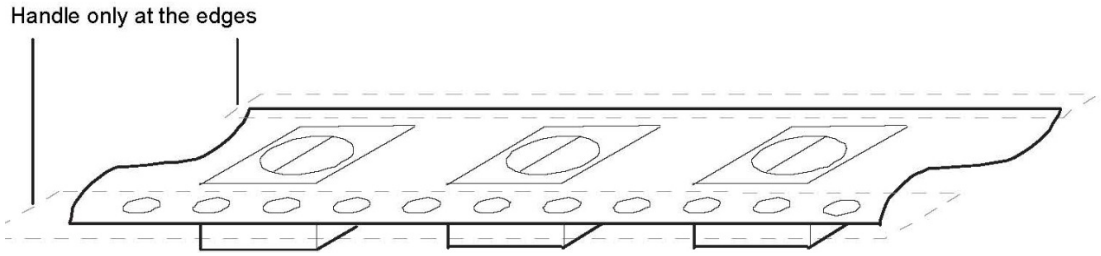


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PM8916 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is not necessary to bake the PM8916 devices if the conditions specified in Sections 5.2.1 and 5.2.2 have not been exceeded.

It is necessary to bake the PM8916 devices if any condition specified in Section 5.2.1 or 5.2.2 has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag.

If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

PM8916 ESD ratings will be available in future revisions of this document.

6 PCB Mounting Guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. QTI defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes QTI board-level characterization-process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land-pattern and stencil recommendations presented in this section are based on QTI internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

QTI recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder-stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land-pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solder-able area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). QTI recommends square apertures for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

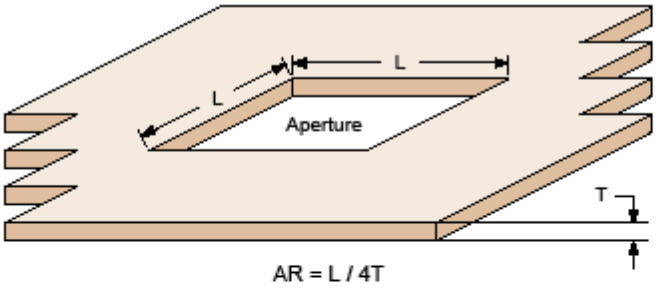


Figure 6-1 Stencil printing aperture area ratio (AR)

Guidelines for an acceptable relationship between L and T are listed below, and are shown in Figure 6-2:

- R = L/4T > 0.65 – best
- 0.60 ≤ R ≤ 0.65 – acceptable
- R < 0.60 – not acceptable

Stencil Aperture L (µm)	Stencil thickness, T (µm)							
	75	80	85	90	95	100	105	110
210	0.70	0.66	0.62	0.58	0.55	0.53	0.50	0.48
220	0.73	0.69	0.65	0.61	0.58	0.55	0.52	0.50
230	0.77	0.72	0.68	0.64	0.61	0.58	0.55	0.52
240	0.80	0.75	0.71	0.67	0.63	0.60	0.57	0.55
250	0.83	0.78	0.74	0.69	0.66	0.63	0..60	0.57
260	0.87	0.81	0.76	0.72	0.68	0.65	0.62	0.59

Figure 6-2 Acceptable solder-paste geometries

6.2.2 Reflow profile

Reflow profile conditions typically used by QTI for lead-free systems are listed in Table 6-1 and are shown in Figure 6-3.

Table 6-1 QTI typical SMT reflow-profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C[1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

[1]During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

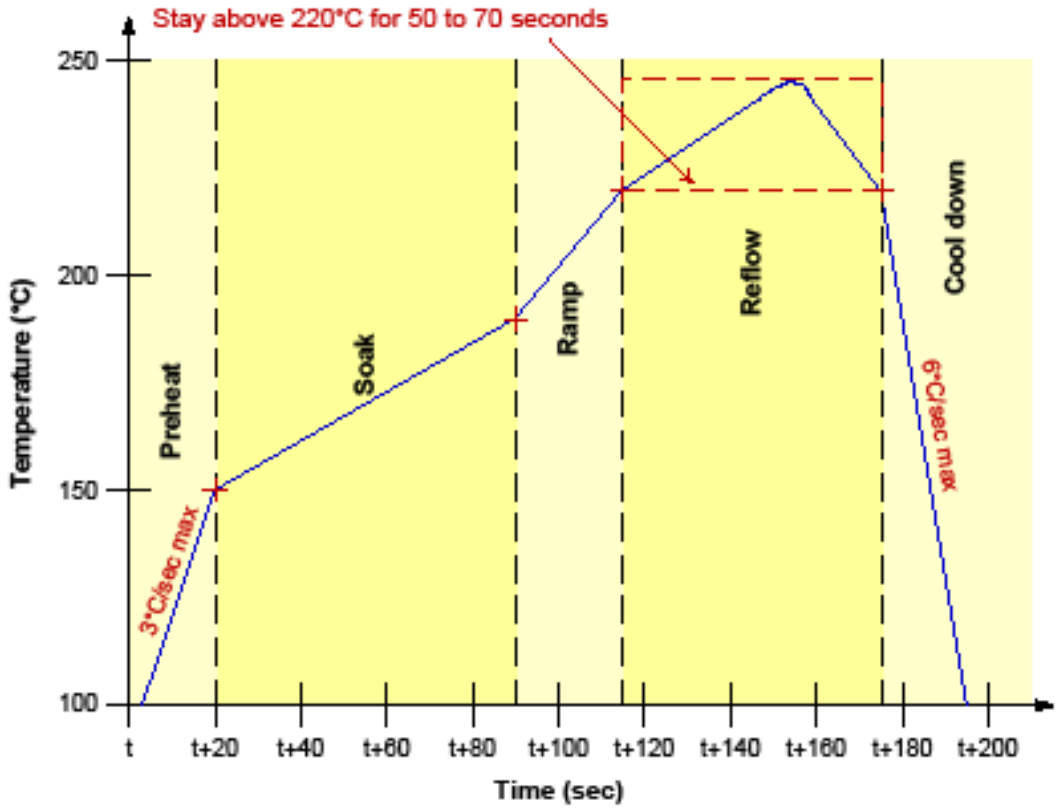


Figure 6-3 QTI typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document; without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

1. Device moisture-sensitivity level

   PM8916 devices are classified as MSL3 @ 250°C. The temperature (250°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained in #2 below.

2. Reliability qualifications summary

   One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5 C (255 to 260 °C).

3. Reflow profile

   During a production board's reflow process, the temperature seen by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections. However, it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (250°C or more).

6.2.4 SMT process verification

QTI recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow-profile measurement and verification
- Visual and X-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

7 Part Reliability

7.1 Reliability qualifications summary

7.1.1 PM8916 reliability evaluation report for NSP device

Table 7-1 Silicon reliability results for SMIC

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (l) failure in billion device-hours HTOL: JESD22-A108 Use condition: temperature: 85°C, voltage: 4.75 V Total samples from three different wafer lots	2331	DPPM < 1000[1] Cum FITs < 25 FITs[1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	2331	> 401
ESD – Human-body model (HBM) rating: JESD22-A114 Total samples from one wafer lot	3	2000 V
ESD – Charge-device model (CDM) rating: JESD22-C101 Target 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × VDD max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

[1]Cum FITs from multiple products under SMIC-S1, 0.18 µm process.

Table 7-2 Silicon reliability results for TSMC

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (l) failure in billion device-hours HTOL: JESD22-A108 Use condition: temperature: 8°C, voltage: 4.75 V Total samples from three different wafer lots	472	DPPM < 1000[1] Cum FITs < 25 FITs[1]
Mean time to failure (MTTF) t = 1/l in million hours Total samples from three different wafer lots	472	> 401
ESD – Human-body model (HBM) rating: JESD22-A114 Total samples from one wafer lot	3	2000 V[2]
ESD – Charge-device model (CDM) rating: JESD22-C101 Target 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Pass[3]
Latch-up (V supply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × VDD max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

Table 7-3 Package reliability results for SMIC/TSMC

Tests, standards, and conditions	SCC assembly source sample size	ASE-kh assembly source sample size	ATC assembly source sample size	SPIL assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020C Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT	462	462	462	462	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at min/max temperature: 8-10 min Cycle rate: 2 cycles per hour (cph) Preconditioning: JESD22-A113-F MSL1; reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	231	231	231	231	Pass

[1]Cum DPPM and FITs from multiple products under TSMC, 0.18 µm process.

[2]ESD-HBM: All pins pass 2 kV except two pins, which pass at 1.5 kV: GND_DRV and VIB_DRV_N

[3]Latch-up:

All pins pass 100 mA JEDEC specification except option 2 pin which pass at 70 mA for APQ8016/APQ8009 application. Option 2 pin is “NC” in this configuration. Chance of exposure is low.

Tests, standards, and conditions	SCC assembly source sample size	ASE-kh assembly source sample size	ATC assembly source sample size	SPIL assembly source sample size	Result
Unbiased highly accelerated stress test JESD22-A118 130 □C/85% RH and 96 h Preconditioning: JESD22-A113-F MSL1; reflow temperature: 260°C +0/-5 □C Total samples from three different assembly lots at each SAT	231	231	231	231	Pass
High-temperature storage life: JESD22-A103-C Temperature 150 □C; duration Total samples from three different assembly lots at each SAT	231	231	231	231	Pass
Flammability UL-STD-94 Note: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mount are rated V-0 (better than V-1).	NA	NA	NA	NA	Pass
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	78	78	78	78	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	15	15	15	15	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	78	78	78	78	Pass

7.2 Qualification sample description

Device characteristics

- Device name: PM8916
- Package type: 176 NSP
- Package body size: 6.2 mm × 6.2 mm × 0.86 mm
- Lead count: 176
- Lead composition: SAC125Ni
- Fab process: 0.18 µm HV-CMOS
- Fab sites: SMIC and TSMC
- Assembly sites: Amkor, China; STATSChipPAC, China; ASE, Taiwan; SPIL, Taiwan
- Solder ball pitch: 0.4 mm

A Exhibit 1

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