

HyperLynx GHz includes a complete suite of tools for pre- and post-layout signal integrity, crosstalk and EMC analysis.

#### Major product benefits:

- Easy to learn, use and deploy.
- Analyze inter-symbol interference in multi-gigabit signals with multi-bit stimulus, jitter, eye diagrams, and eye masks to define keepout regions.
- Simulate with IBIS or HSPICE<sup>®</sup> models easier than ever.
- Accurate modeling of lossy transmission-line effects-including skin effect and dielectric loss.
- Frequency-dependent via modeling.
- Differential signal simulation and analysis — including differential impedance planning, and optimization of differential terminations.
- Terminator Wizard™ recommends optimal termination strategies including series termination, parallel, parallel AC, and differential.
- Easy to use multi-board analysis.
- Provides an early look at likely EMC failures, including both radiation and trace current analysis.
- Works with all major PCB layout and routing applications.

## **Overview**

Increasingly fast edge-rates in today's integrated circuits (ICs) cause detrimental high-speed effects, even in PCB designs running at low operating frequencies. As driver ICs switch faster, a growing volume of boards suffer from signal degradation, including over/undershoot, ringing, glitching, crosstalk, and timing problems. When degradation becomes serious enough, the logic on a board can fail-making otherwise excellent designs stare blankly into space.

HyperLynx<sup>®</sup> EXT — including LineSim<sup>TM</sup> for pre-layout analysis and BoardSim<sup>TM</sup> for post-route analysis — targets designs at frequencies up to about 500 MHz. At higher speeds, lossy effects (including skin effect and dielectric loss) and via modeling take on increasing importance; the HyperLynx GHz bundle models all of these effects and addresses the special needs of multi-gigabit design.

## **Complete SI and EMC Analysis Suite**

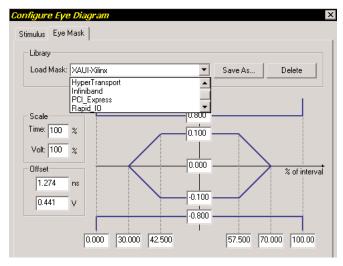
With HyperLynx, you can address high-speed PCB problems throughout your design cycle, beginning at the earliest architectural stages and moving through post-layout verification. The emphasis is on solving problems early — where it is less costly and more efficient, and on getting results without spending weeks in training, and getting it right the first time, saving recurrent layout, prototype and test cycles in the lab. Hardware engineers, PCB designers, and signal integrity specialists alike can use HyperLynx EXT or GHz as a team — it's even easier than using an oscilloscope or spectrum anlyzer in the lab.



### **LineSim GHz**

Pre-layout simulation with LineSim GHz, part of HyperLynx GHz, allows you to predict and eliminate signal integrity problems early, allowing you to proactively constrain routing, plan stackups, and optimize clock, critical signal topologies and terminations prior to board layout. LineSim's intuitive point-and-click transmission-line modeling approach is an ideal way to get it right the first time.

- Simulate with IBIS or HSPICE models easier than ever.
- Accurate modeling of lossy transmission-line effects including skin effect and dielectric loss.
- Full analysis of differential pairs to achieve desired differential impedance, and to optimize differential termination.
- Quickly enter complex interconnect scenarios, including ICs, transmission lines, cables, connectors and passive components.
- Model any combination of transmission line: microstrip, buried microstrip or symmetric/asymmetric stripline.
- Simulate immediately, using industry-standard IBIS models, HyperLynx's 7,000 model IC library, generic models, or build your own models from databook information.
- Visual IBIS Editor allows you to test and edit IBIS modelsincluding a powerful V/I-V/t auto-correct option, and dragand-drop curve correction.



Analyze inter-symbol interference in multi-gigabit signals withmulti-bit stimulus, jitter, eye diagrams and eye masks to define keepout regions.

### **BoardSim GHz**

Post-layout signal integrity simulation with BoardSim GHz, part of HyperLynx GHz, allows you to analyze signal integrity and timing at three important stages — following part placement in your PCB layout system, after critical net routing, and after detailed routing of an entire board.

- Analyze inter-symbol interference for multi-gigabit signals with multi-bit stimulus, jitter, eye diagrams, and eye masks to define keepout regions.
- Simulate with IBIS or HSPICE models easier than ever.
- Accurate modeling of lossy transmission-line effects including skin effect and dielectric loss.
- Frequency-dependent via modeling.
- Board Wizard<sup>TM</sup> automatically scans large numbers of nets on an entire PCB, flagging SI/EMC hot spots.
- Interactive analysis then takes you to the next level, simulating batch analysis-identified trouble spots.
- Terminator Wizard recommends optimal termination values, eliminating tedious calculations.
- Quick Terminators allow new termination components to be inserted on-the-fly, enabling real-time analysis.
- Full analysis of differential pairs, including the effects of inter-pair crosstalk, differential impedance and differential termination optimization with Terminator Wizard.
- Accurately predicts crosstalk waveforms for any trace topology and IC placement, also showing board designers specific cross-sections in violation of crosstalk thresholds.
- Powerful, easy to use multi-board analysis.

BoardSim is compatible with these PCB layout systems:

- Mentor Graphics PADS<sup>®</sup> PowerPCB<sup>TM</sup>, Expedition<sup>TM</sup>, Board Station<sup>®</sup>
- · Cadence Allegro, SPECCTRA and OrCAD Layout
- Altium Protel and P-CAD
- Intercept Pantheon
- Zuken CADStar, Visula and CR3000/5000 PWS or BD

# Minimum Hardware/Software Requirements

#### Windows XP, 2000, NT 4.0, ME, or 98:

- Pentium II 333 MHz CPU, or faster
- 128 MB RAM; 80 MB hard disk space
- 1024 x 768, 256 color display
- NIC, Parallel port, or USB port to supply HostID to license management software

#### Sun Solaris™ version 8 or 9:

• 300 MB hard disk space

Recommended patches for Solaris 8:

- Recommended Patch Cluster: March 19, 2002 or later
- Mach 64 Graphics card patch: 108606-31 or later

To learn more about high-speed PCB design, HyperLynx EXT and HyperLynx GHz, visit www.mentor.com/hyperlynx to download the high-speed design tutorial and online demo, or call to schedule a product demonstration.

Copyright © 2003 Mentor Graphics Corporation. Mentor Graphics, Board Station, ePlanner, HyperLynx and PADS are registered trademarks and BoardSim, BoardWizard, Expedition, ICX, LineSim, Terminator Wizard, PowerPCB and XTK are trademarks of Mentor Graphics Corporation. All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters Mentor Graphics Corporation 8005 SW Boeckman Road Wilsonville, OR 97070-7777 Phone: 503.685.7000 Fax: 503.685.1204

Sales and Product Information Phone: 800.547.3000 Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408.436.1500
Fax: 408.436.1501

North American Support Center Phone: 800.547.4303 Europe Mentor Graphics Deutschland GmbH Elsenheimer Strasse 41-43 D-80687 Munchen Germany Phone: +49.89.57096.0

Fax: +49.89.57096.4000

Pacific Rim Mentor Graphics (Taiwan) Room 1603, 16F International Trade Building No. 333, Section 1, Keelung Road Taipei, Taiwan, ROC Phone: 886.2.87252000 Fax: 886.2.27576027 Japan Mentor Graphics Japan Co., Ltd. Gotenyama Hills 7-35, Kita-Shinagawa 4-chome Shinagawa-Ku, Tokyo 140 Japan Phone: 81.3.5488.3033 Fax: 81.3.5488.3021



