

CY8CKIT-062-BLE PSoC 6 BLE Pioneer Board

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Drawing Numbers

PCBA	121-60367-01
PCB	600-60380-01
FAB DRW	610-60337-01
ASSY DRW	620-60345-01
SCH DRW	630-60357-01



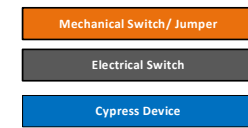
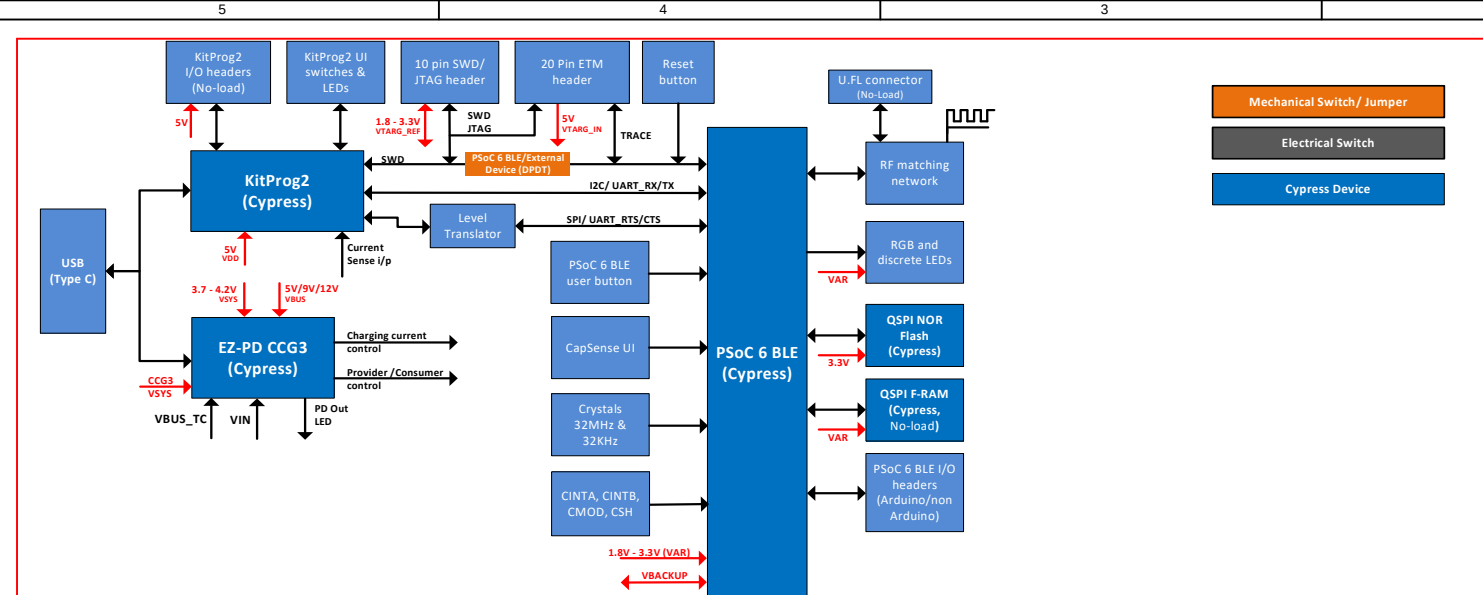
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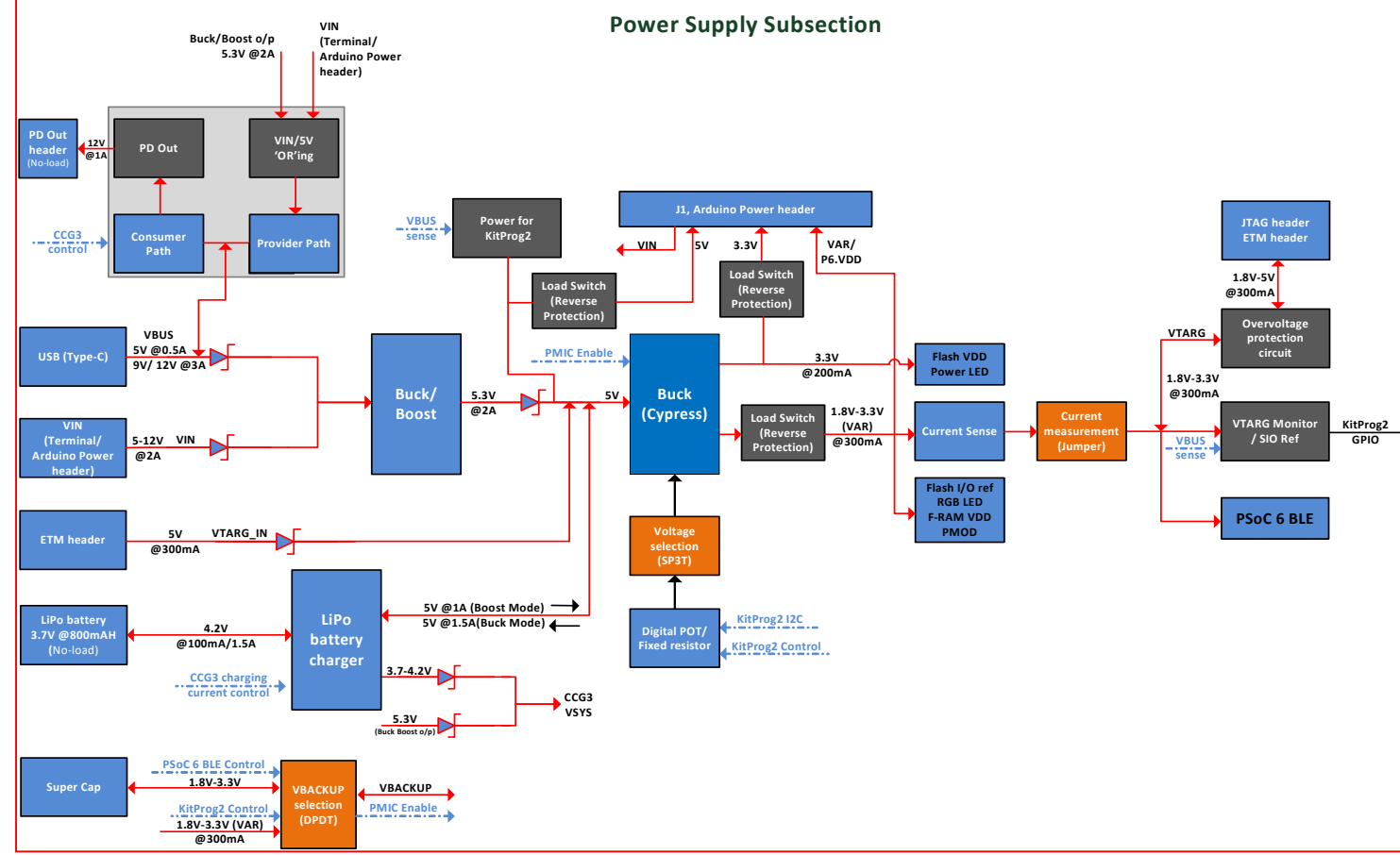
SCH Title : CY8CKIT-062-BLE PSoC 6 BLE Pioneer Board

Page Title : Title & Table of Contents

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Power Supply Subsection





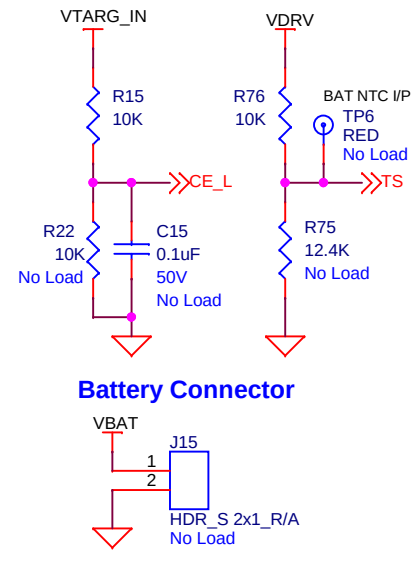
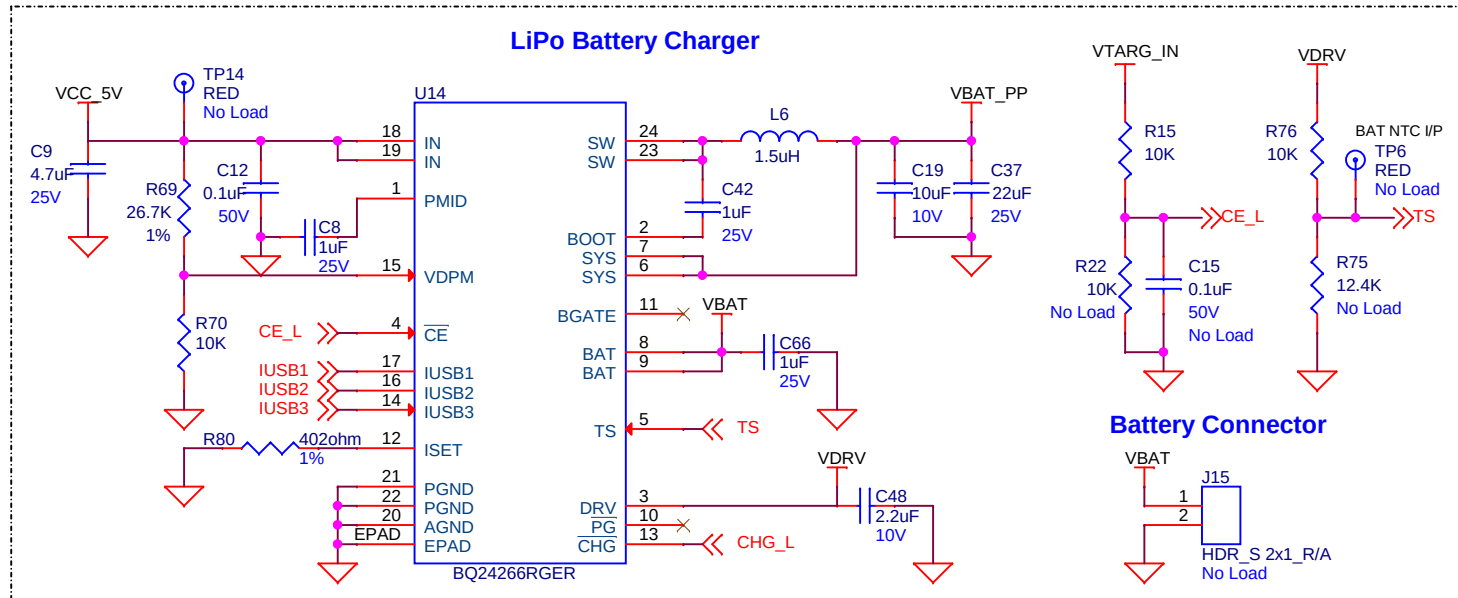
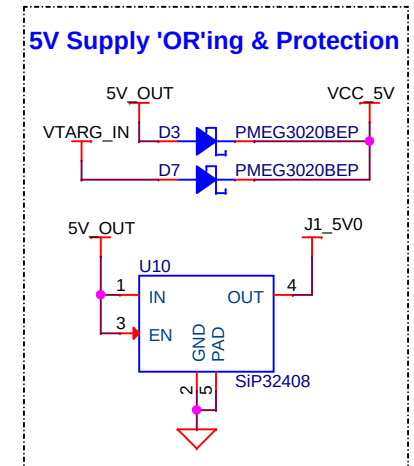
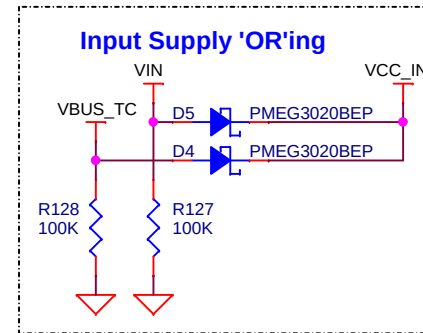
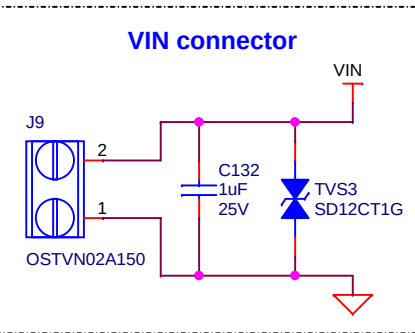
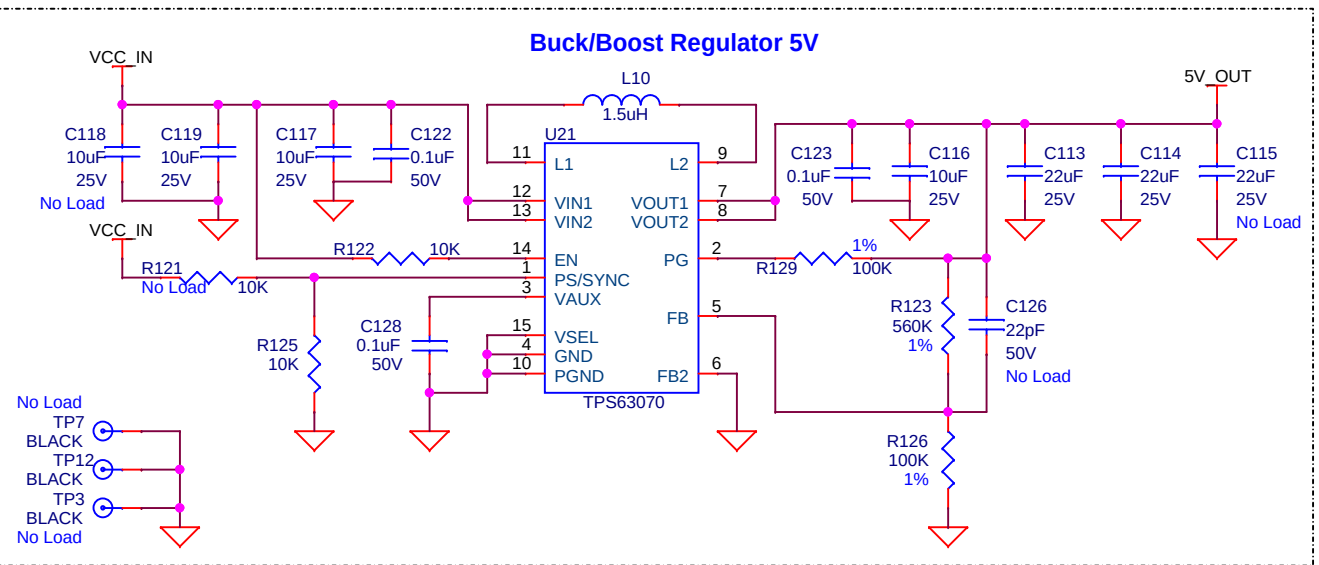
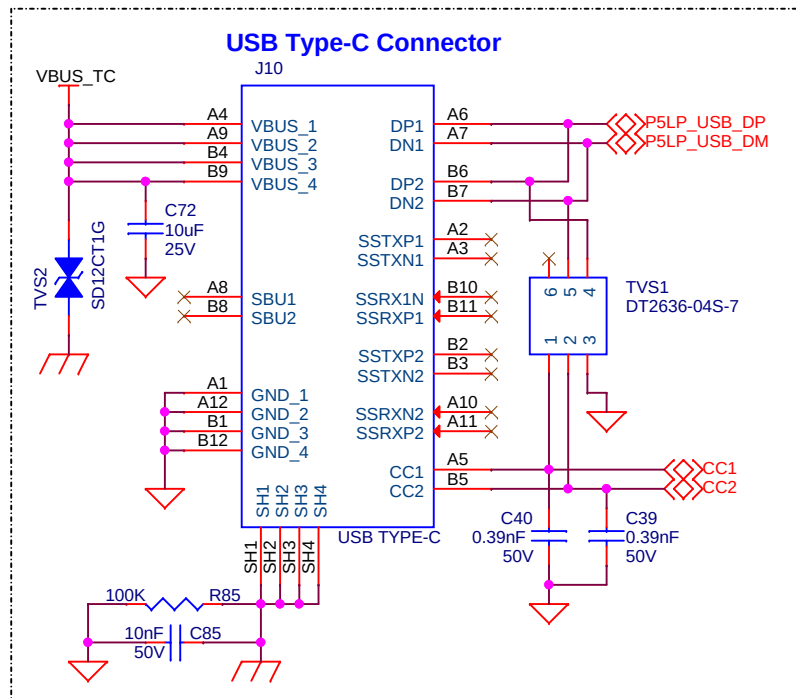
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Page Title : Block Diagram

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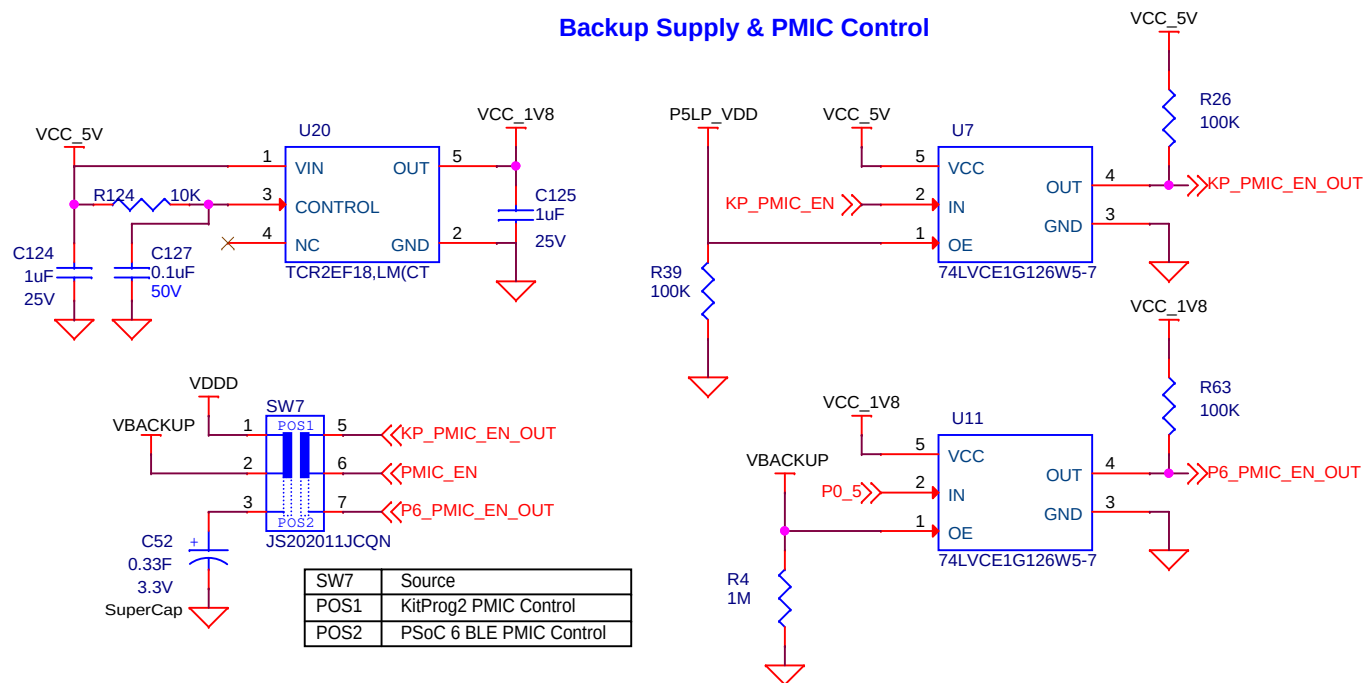
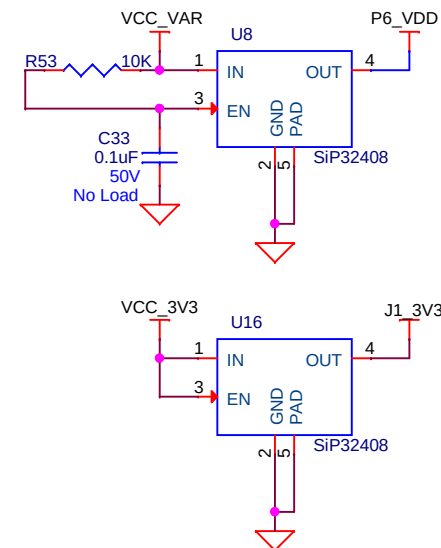
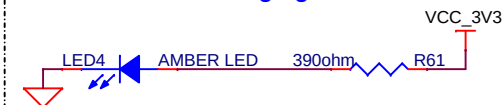
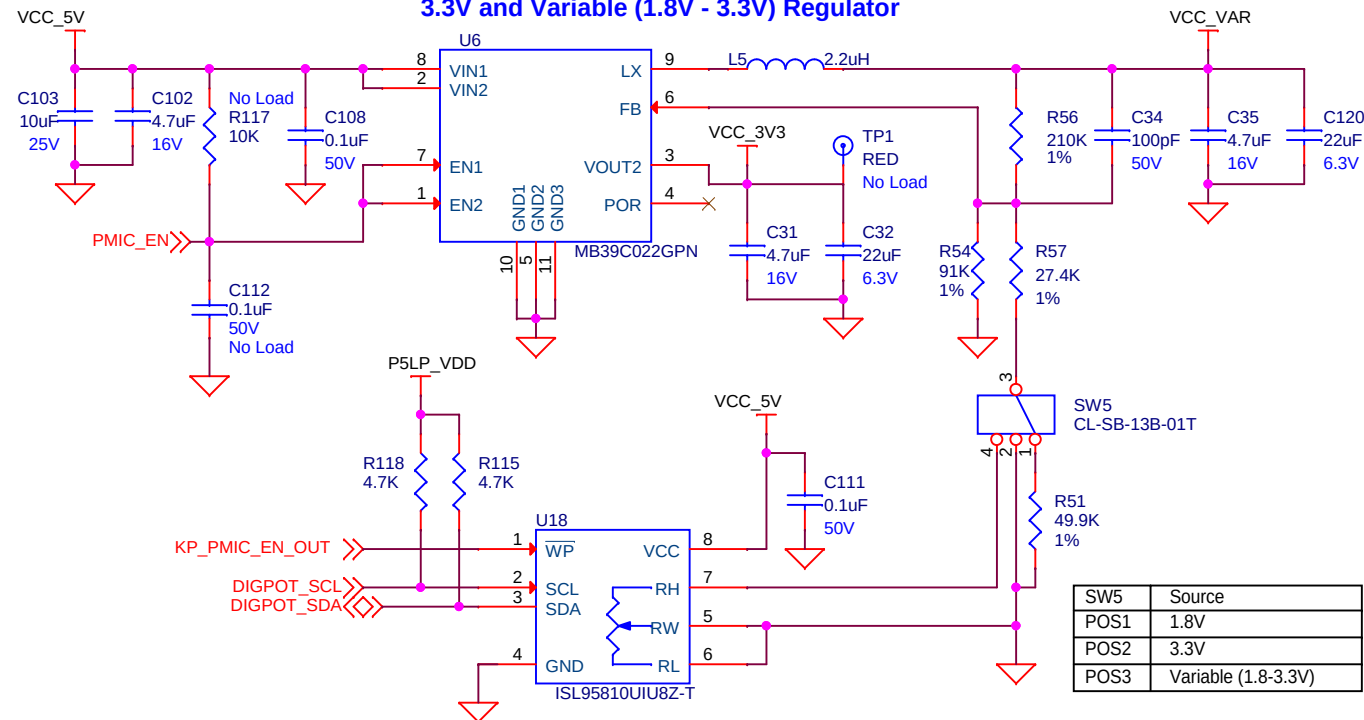
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Page Title : Input Regulators

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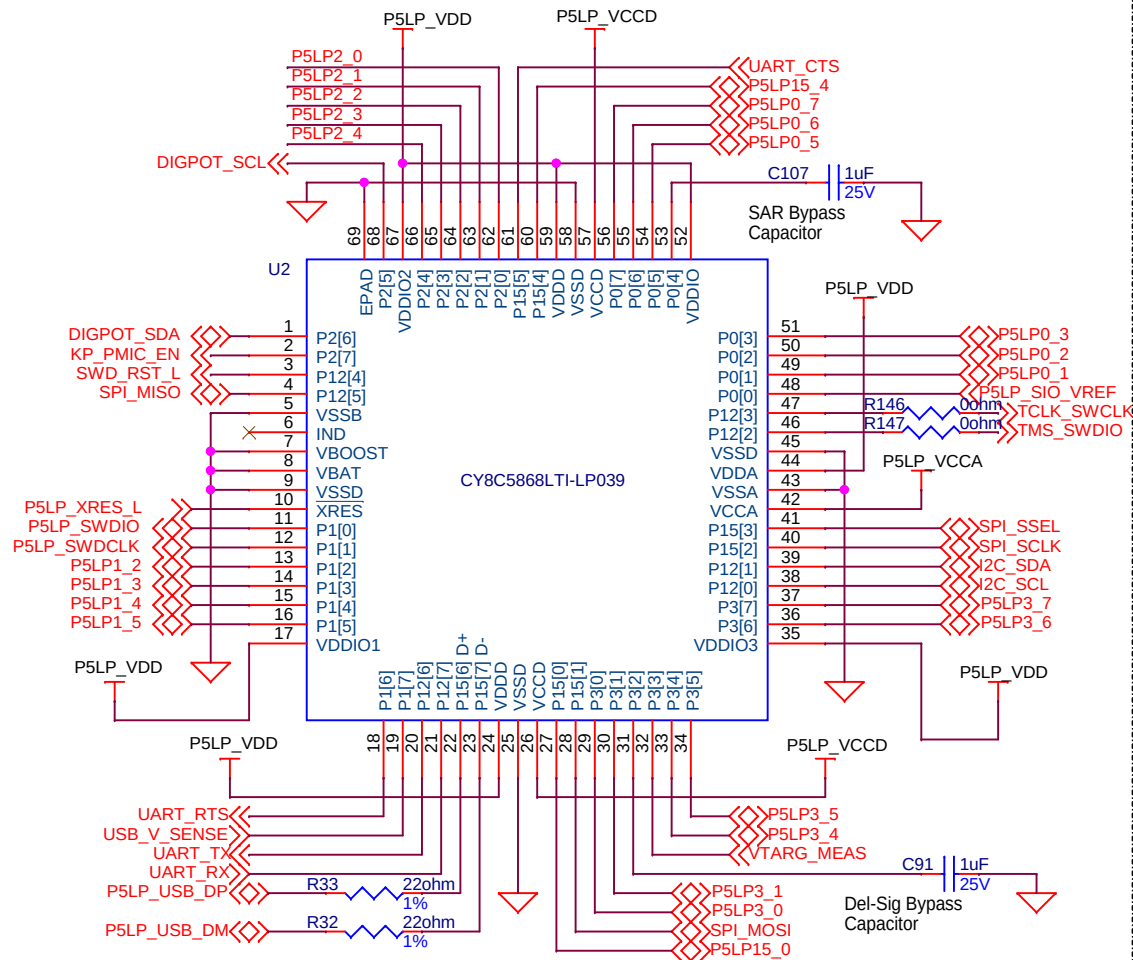
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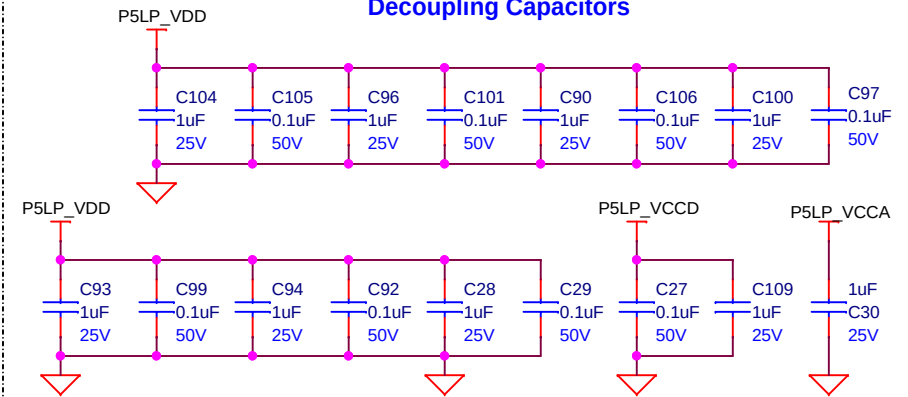
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PSoC 5LP based KitProg2



Decoupling Capacitors



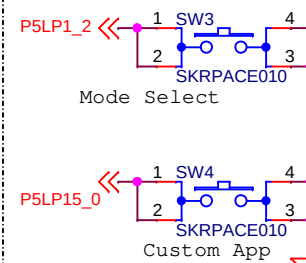
KitProg2 HW Revision

P5LP2_0 Bit 0
P5LP2_1 Bit 1
P5LP2_2 Bit 2
P5LP2_3 Bit 3
P5LP2_4 Bit 4

ID = 0x02

Note: GND is read as binary "1" and floating as "0"

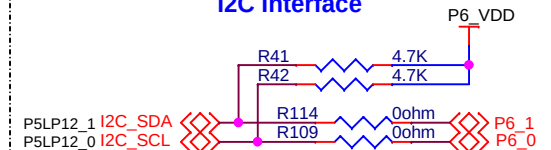
PSoC 5LP User Switches



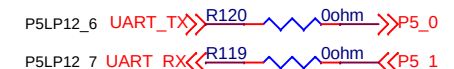
SWD Interface



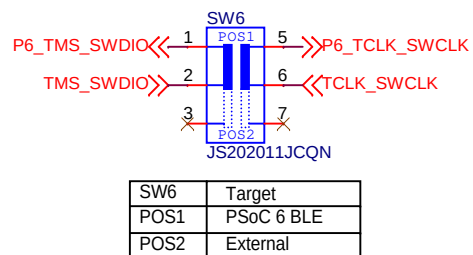
I2C Interface



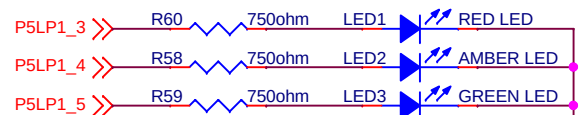
UART Interface



SWD Target Select



PSoC 5LP Status LEDs



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Target PSoC Program/Debug Header

VTARG_REF

C133
1uF
25V

TVS4
ESD3V3D5-TP

J11

1 2 3 4 5 6 7 8 9 10

HDR_S 5x2

TMS_SWDIO

TCLK_SWCLK

TDO_SWO

TDI

SWD_RST_L

Program/Debug Overvoltage Protection

The diagram illustrates a Program/Debug Overvoltage Protection circuit. It includes a P6_VDD input, a VTARG_REF input, and a No Load output. The circuit features several components: NTR4171PT1G (MOSFET), PMV48XP,215 (MOSFET), R152 (0ohm), R151 (15K), R153 (10K), Q3, Q4, D9 (BZT52C3V9-7-F), and DMP3098L-7 (Diode).

Voltage Monitoring

The schematic diagram illustrates the Voltage Monitoring circuit. The main circuit features an operational amplifier (U19, SIP32401ADNP) configured as a voltage follower. The non-inverting input (IN, pin 3) is connected to P5LP_VDD through a 0.1uF capacitor (C110). The inverting input (EN, pin 4) is connected to P6_VDD through a 0.1uF capacitor (C121). The output (OUT, pin 1) is connected to VTARG_MON. The op-amp's GND PAD (pin 5) is connected to ground.

Below the main circuit, three detailed sub-circuits are shown:

- P5LP_VDD:** A voltage divider consisting of resistors R94 (15K) and R95 (30K) connected to P5LP_VDD and ground. The midpoint is labeled USB_V_SENSE.
- VTARG_MON:** A voltage divider consisting of resistors R30 (15K) and R36 (30K) connected to VTARG_MON and ground. The midpoint is labeled VTARG_MEAS.
- VTARG_MON:** A voltage divider consisting of resistors R55 (49.9K, 1% tolerance) and R52 (49.9K, 1% tolerance, No Load) connected to VTARG_MON and ground. The midpoint is labeled P5LP_SIO_VREF.

Level Translator for SPI and UART flow control

The diagram illustrates a level translator circuit for SPI and UART flow control, centered around the FXMA108BQX IC (U13). The IC is configured as follows:

- Power Supply:**
 - VCCB (Pin 20) is connected to P5LP_VDD.
 - VCCA (Pin 1) is connected to P6_VDD.
 - Both P5LP_VDD and P6_VDD are decoupled to ground with 1μF/25V capacitors (C38 and C41).
 - DAP (Pin 21) is connected to ground.
- Signal Connections:**
 - SPI Signals:**
 - SPI_MOSI (Pin 19) to B0
 - SPI_SCLK (Pin 18) to B1
 - SPI_MISO (Pin 17) to B2
 - SPI_SSEL (Pin 16) to B3
 - UART_RTS (Pin 15) to B4
 - UART_CTS (Pin 14) to B5
 - UART Signals:**
 - Pin 13 (B6) and Pin 12 (B7) are marked with 'X', indicating no connection.
 - Output Signals:**
 - A0 (Pin 2) to P12_0
 - A1 (Pin 3) to P12_2
 - A2 (Pin 4) to P12_1
 - A3 (Pin 5) to P5LP_SSEL_P12_4
 - A4 (Pin 6) to P5_3
 - A5 (Pin 7) to P5_2
 - Pin 8 (A6) and Pin 9 (A7) are marked with 'X', indicating no connection.
 - Control and Status:**
 - OE (Pin 11) is connected to P6_VDD through a 10K resistor (R78) and is labeled "No Load".
 - Pin 10 (GND) is connected to ground.

PSoc 5LP GPIO Expansion Header

The diagram illustrates the pin configuration for the PSoc 5LP GPIO Expansion Header (J6). The header is a 16-pin connector with the following connections:

- Pin 1:** P5LP_VDD
- Pin 3:** P5LP15_1 SPI_MOSI
- Pin 5:** P5LP15_2 SPI_SCLK
- Pin 7:** P5LP15_3 SPI_SSEL
- Pin 9:** P5LP12_5 SPI_MISO
- Pin 11:** CUSTOM P5LP3_4
- Pin 13:** P5LP12_7 UART_RX
- Pin 15:** CUSTOM P5LP3_6
- Pin 2:** P5LP0_1 CUSTOM
- Pin 4:** I2C_SCL P5LP12_0
- Pin 6:** P5LP3_0 CUSTOM
- Pin 8:** I2C_SDA P5LP12_1
- Pin 10:** P5LP3_5 CUSTOM
- Pin 12:** CUSTOM
- Pin 14:** UART_TX P5LP12_6
- Pin 16:** CUSTOM

The header is labeled **J6** and **CON 8x2 No Load**.

PSoC 5LP Custom Application Header

Diagram illustrating the PSoC 5LP Custom Application Header (J7) connections:

- Pin 1:** CUSTOM P5LP0_2
- Pin 3:** CUSTOM P5LP0_3
- Pin 5:** CUSTOM P5LP0_7
- Pin 7:** CUSTOM UART_RTS
- Pin 9:** CUSTOM P5LP15_4
- Pin 2:** P5LP_VDD
- Pin 4:** P5LP_XRES_L
- Pin 6:** P5LP_SWDCCLK
- Pin 8:** P5LP_SWDCCLK
- Pin 10:** P5LP_SWDIO

Connector: CON 5x2 No Load

Supply for PSoC 5LP

The diagram illustrates the power supply circuit for the PSoC 5LP. It features a voltage divider network that takes input from VBUS_TC. This network includes a 120K resistor (R89) in series with a parallel combination of a 75K resistor (R86) and a 0.1uF capacitor (C84) connected to ground. The output of this divider is connected to the EN (enable) pin (pin 4) of the SIP32401ADNP voltage regulator (U15). The regulator's input (IN, pin 3) is connected to VCC_5V through a 0.1uF capacitor (C89). The regulator's output (OUT, pin 1) provides power to P5LP_VDD. The GND PAD (pin 2) is connected to ground. The title "Supply for PSoC 5LP" is shown in blue text at the top of the diagram.



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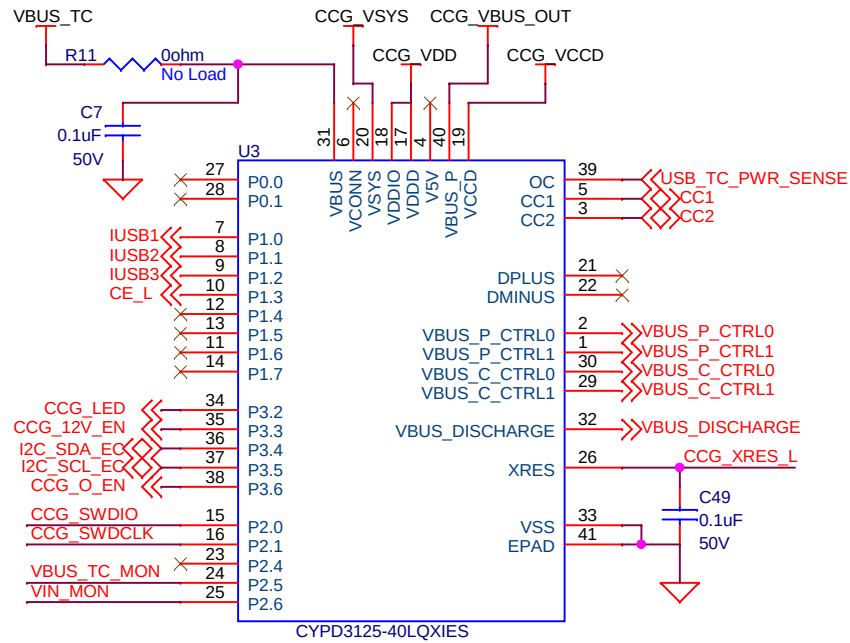
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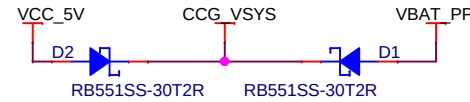
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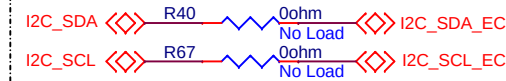
CCG3, USB Type-C and Power Delivery



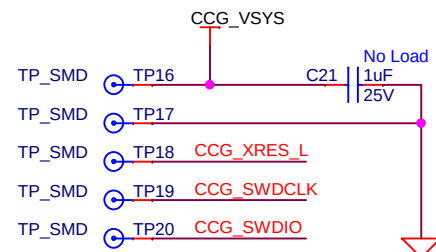
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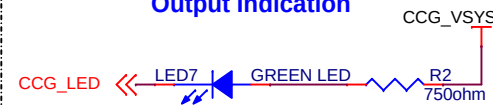
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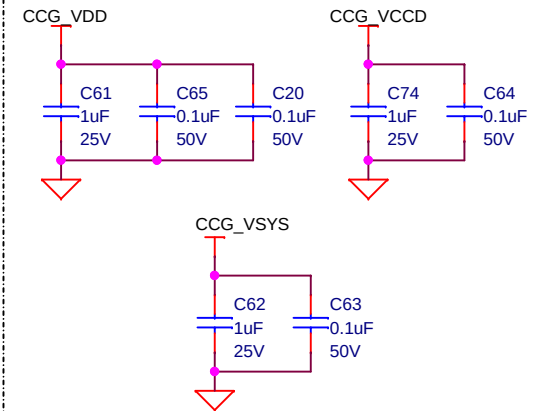
CCG3 Programming



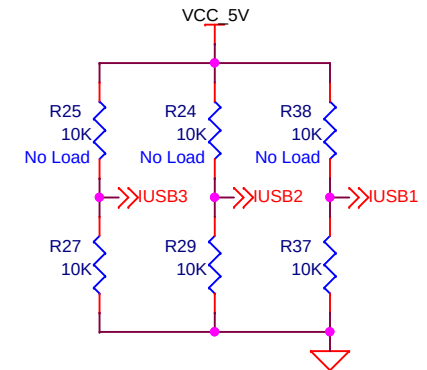
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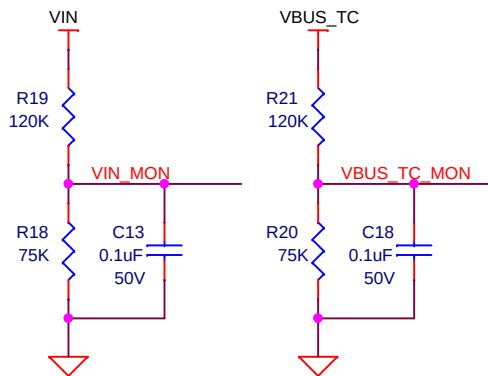
Decoupling Capacitors



LiPo battery charger pull-up



VBUS and VIN voltage monitoring



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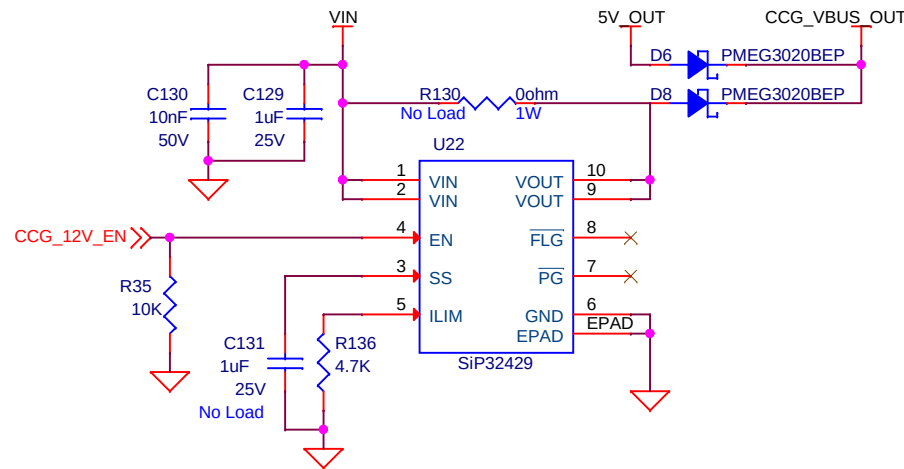
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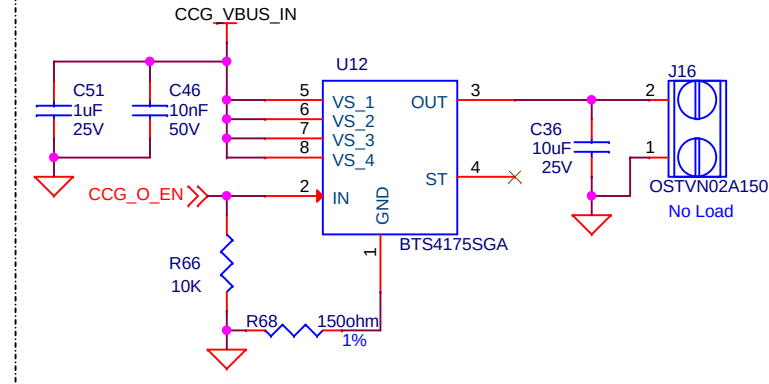
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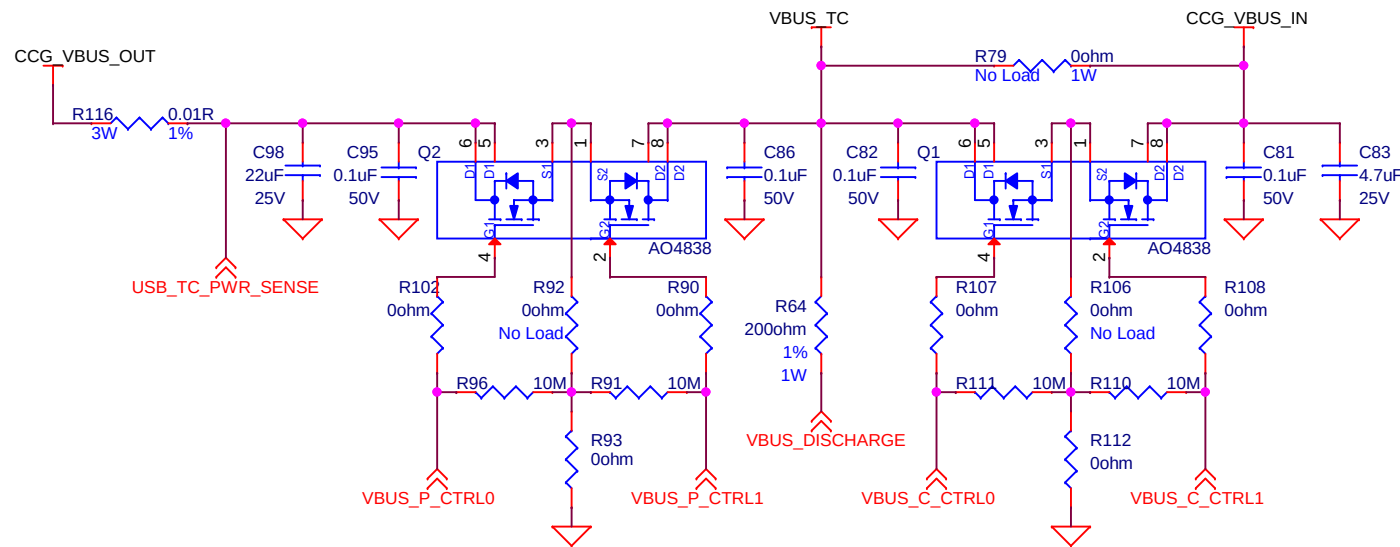
CCG3 Provider path 'OR'ing



CCG3 12V @1A Output



VBUS Provider/Consumer Path



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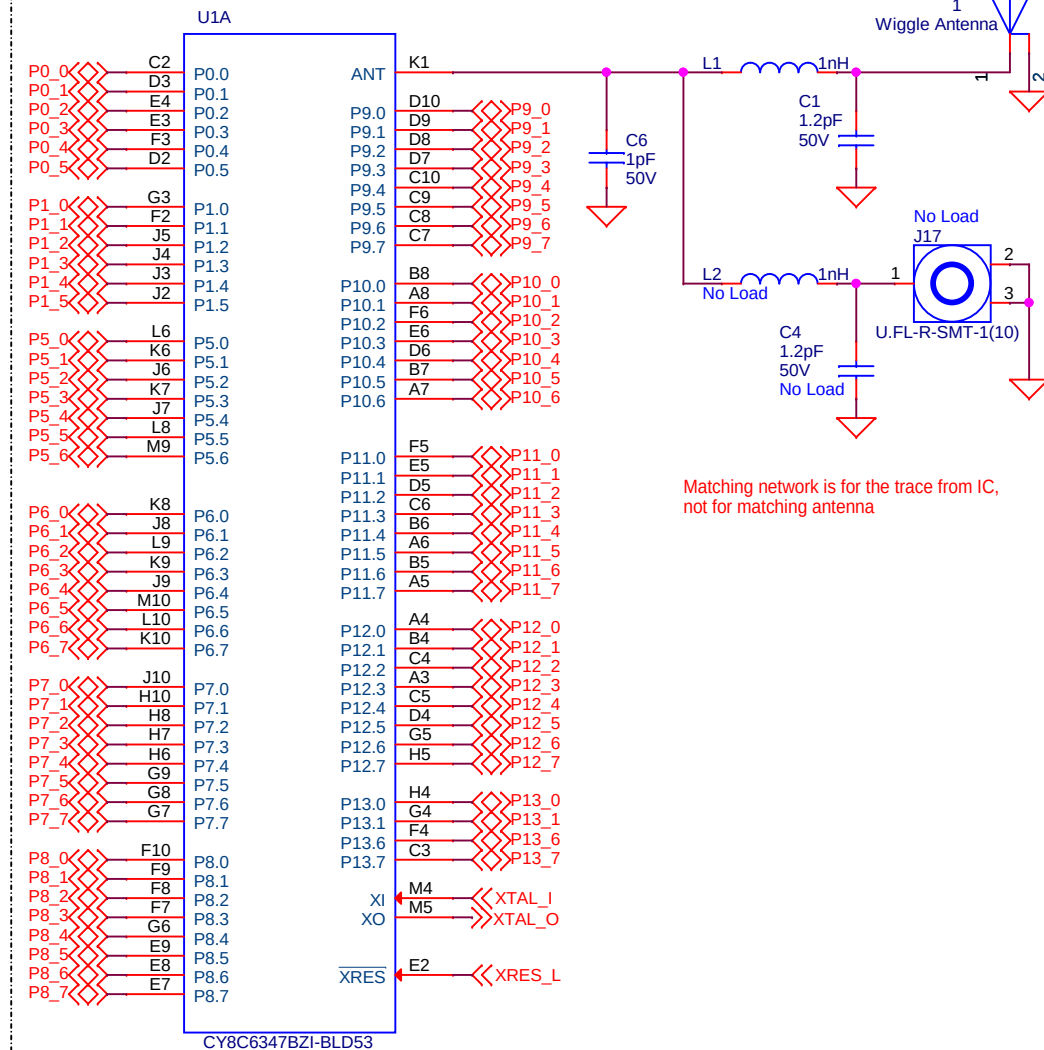
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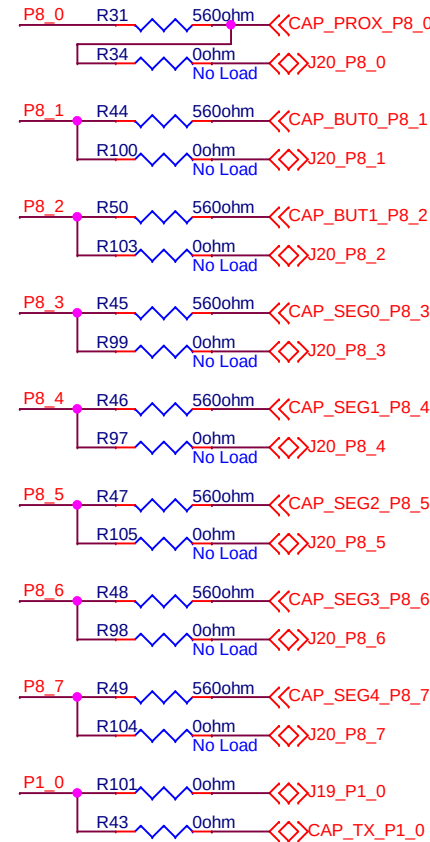
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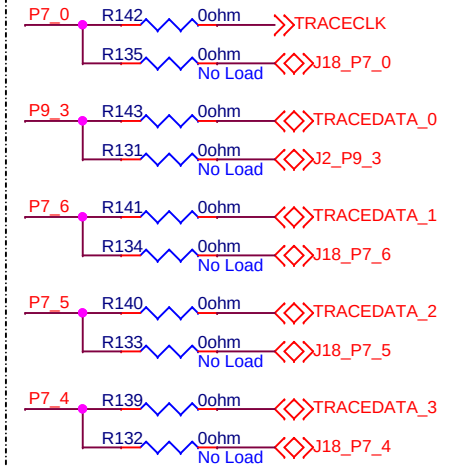
PSoC 6 BLE



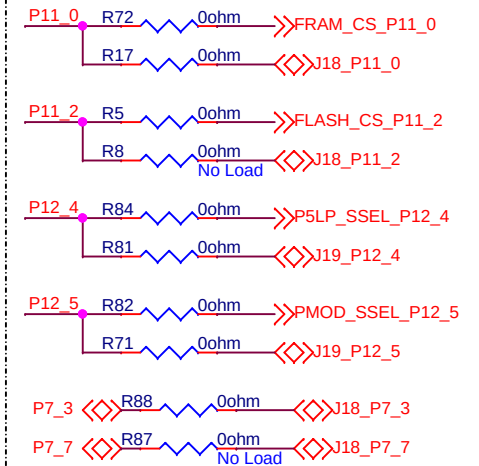
CapSense Multiplexed pins



TRACE Multiplexed pins



Additional Multiplexed pins



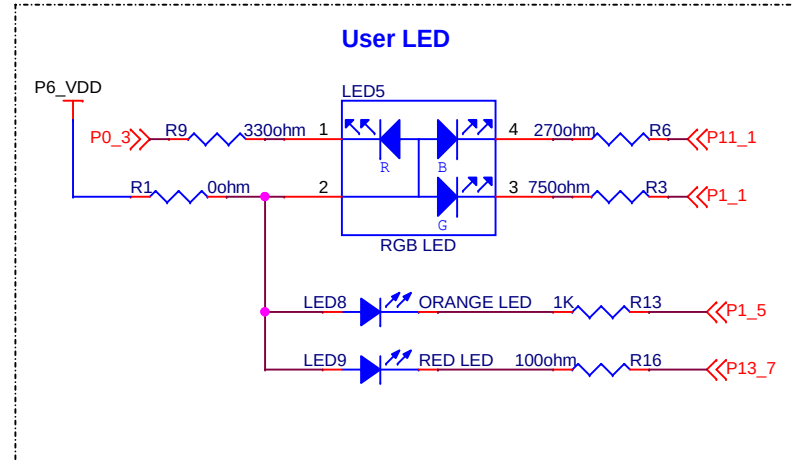
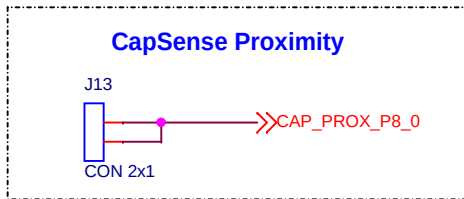
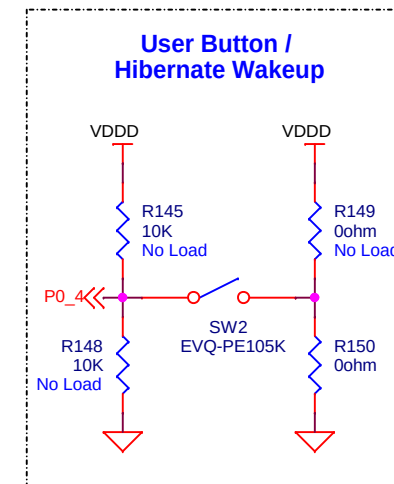
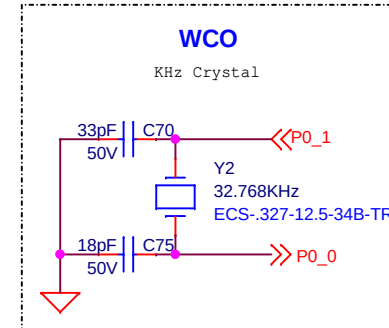
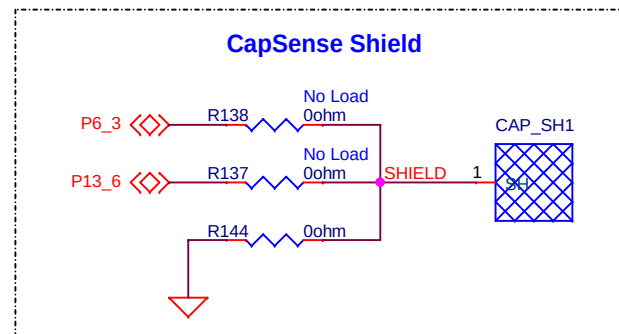
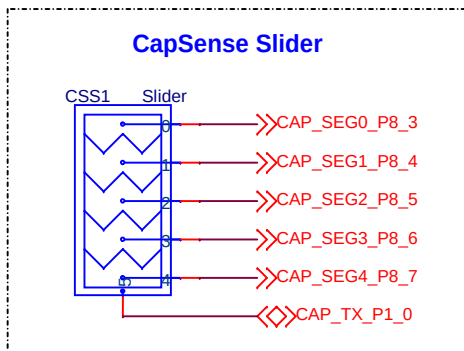
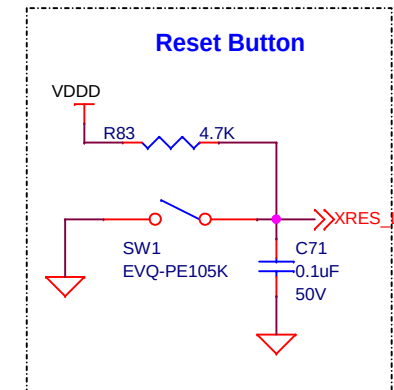
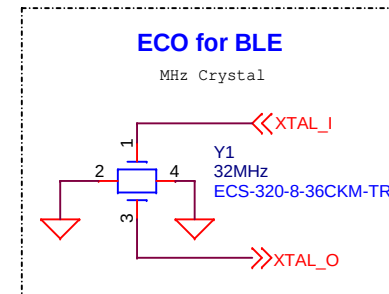
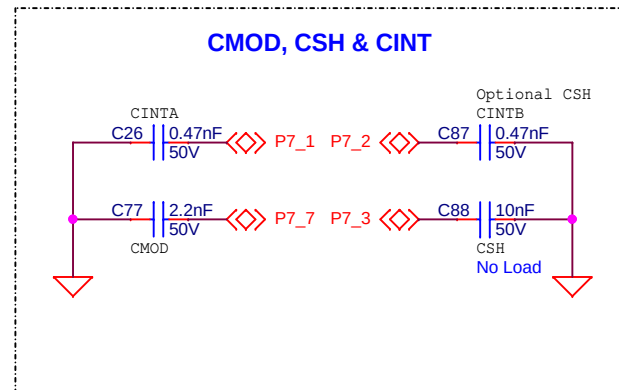
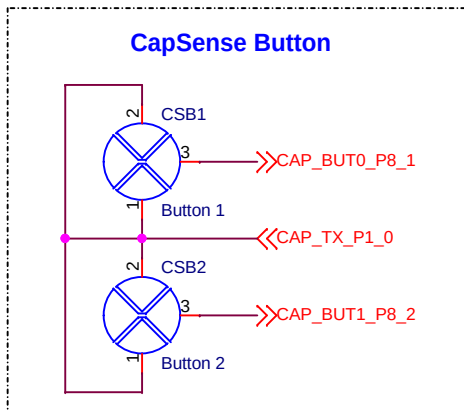
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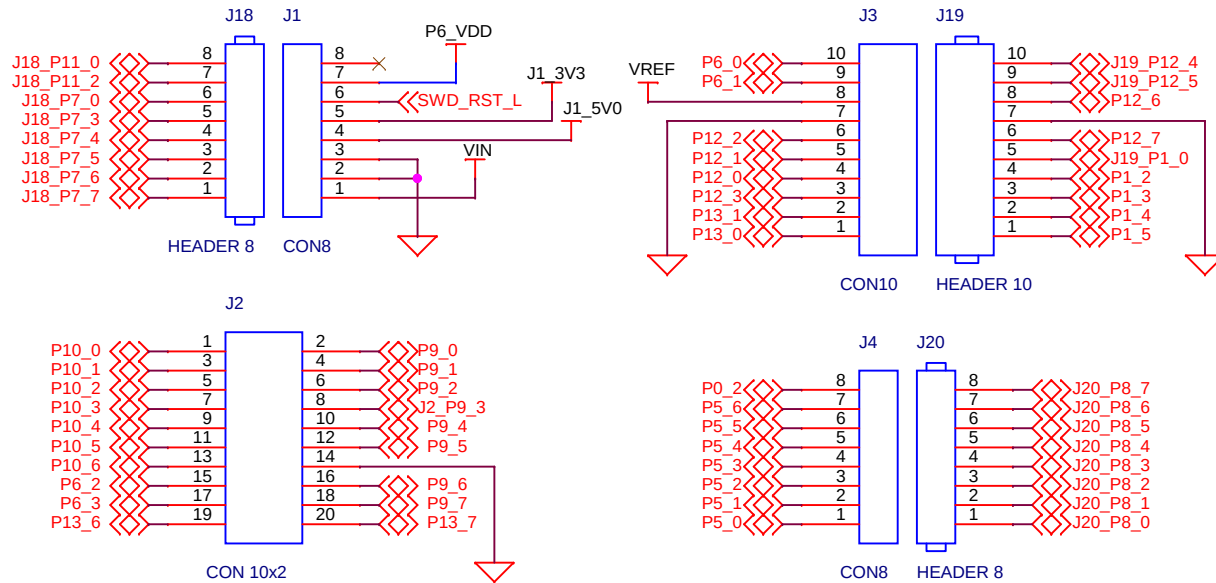
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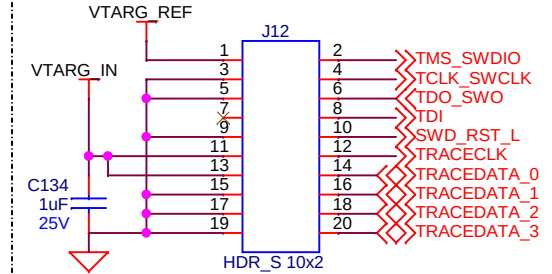
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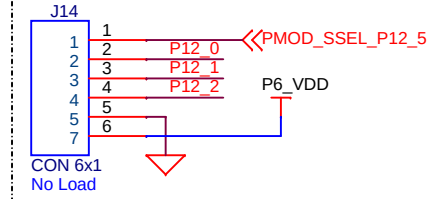
Arduino Headers



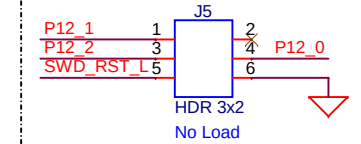
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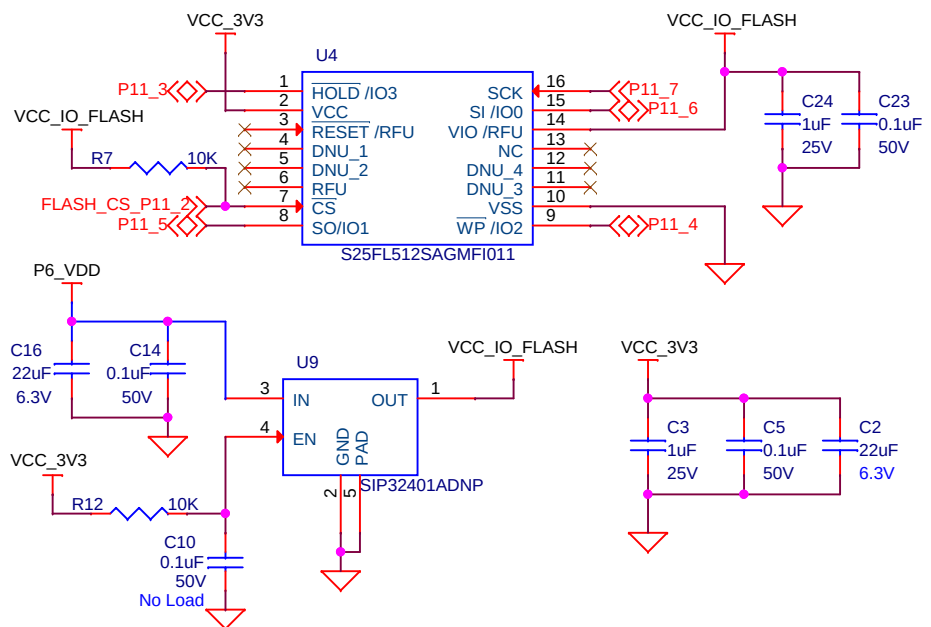
Pmod Header



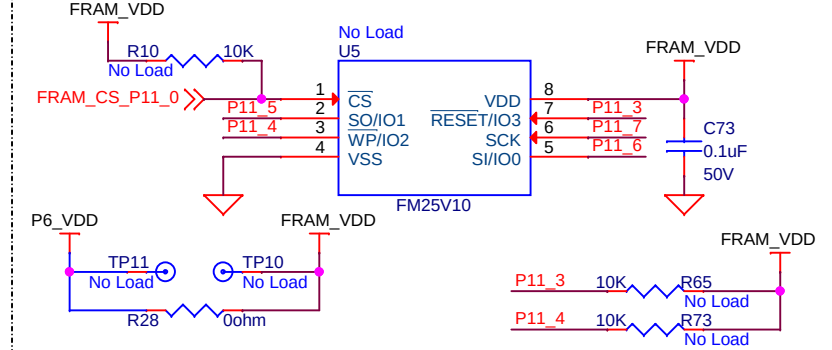
ICSP Header



QSPI Flash (SMIF)



F-RAM



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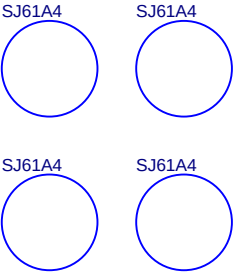
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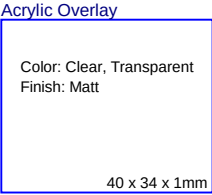
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Accessories

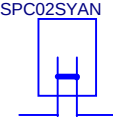
Cylindrical Bumper



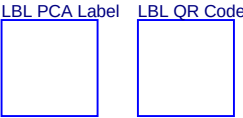
Acrylic Overlay



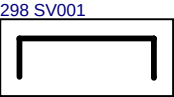
Jumper Shunt



PCBA label



USB connector bracket



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Revision History

Rev	Description	Date
01	Initial internal release	08/29/2016
02	Internal release	10/03/2016
03	Internal release	11/25/2016
04	Initial external release under NDA	01/19/2017
05	3.3V protection diode changed to load SW (U59) Added PMIC control section (U58, U56, U57 and passives) Removed series resistor for SPI and UART HW flow control Voltage Monitoring domain and Protection Circuit o/p changed to P6_VDD Changed trace data line connection (to 9.3, 7.6, 7.5, 7.4) C22 Cap on VRF changed to 10uF Removed SW8 and connected CINT directly, CMOD connection changed to 7.7 Shield # changed to 13.6/6.3 Added additional LED on pin 13.7 and 1.5 Added option to change logic for user SW and added pull-up/down Back annotated from layout	5/2/2017



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Page Title : **Revision History**

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