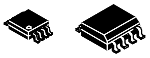


HIGH-VOLTAGE, LOW-DISTORTION, CURRENT-FEEDBACK OPERATIONAL AMPLIFIERS

FEATURES

- Low Distortion
  - – 77 dBc HD2 at 10 MHz, R_L = 1 kΩ
  - – 69 dBc HD3 at 10 MHz, R_L = 1 kΩ
- Low Noise
  - – 14 pA/$\sqrt{Hz}$ Noninverting Current Noise
  - – 17 pA/$\sqrt{Hz}$ Inverting Current Noise
  - – 2 nV/$\sqrt{Hz}$ Voltage Noise
- High Slew Rate: 7300 V/µs (G = 5, V_O = 20 V_{PP})
- Wide Bandwidth: 210 MHz (G = 2, R_L = 100 Ω)
- High Output Current Drive: ±250 mA
- Wide Supply Range: ±5 V to ±15 V
- Power-Down Feature: (THS3095 Only)

APPLICATIONS

- High-Voltage Arbitrary Waveform
- Power FET Driver
- Pin Driver
- VDSL Line Driver

DESCRIPTION

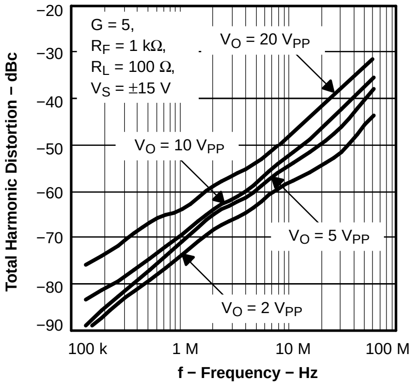
The THS3091 and THS3095 are high-voltage, low-distortion, high-speed, current-feedback amplifiers designed to operate over a wide supply range of ±5 V to ±15 V for applications requiring large, linear output signals such as Pin, Power FET, and VDSL line drivers.

The THS3095 features a power-down pin (PD) that puts the amplifier in low power standby mode, and lowers the quiescent current from 9.5 mA to 500 µA.

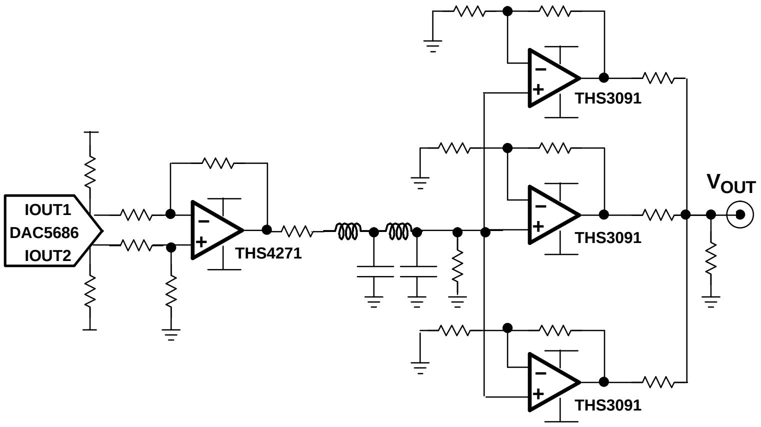
The wide supply range combined with total harmonic distortion as low as -69 dBc at 10 MHz, in addition, to the high slew rate of 7300 V/µs makes the THS3091/5 ideally suited for high-voltage arbitrary waveform driver applications. Moreover, having the ability to handle large voltage swings driving into high-resistance and high-capacitance loads while maintaining good settling time performance makes the devices ideal for Pin driver and PowerFET driver applications.

The THS3091 and THS3095 are offered in an 8-pin SOIC (D), and the 8-pin SOIC (DDA) packages with PowerPAD™.

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

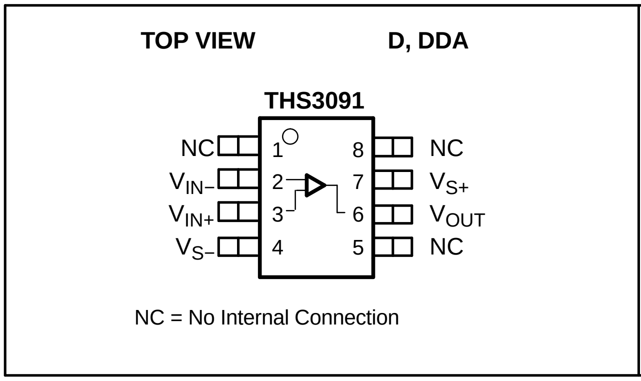


TYPICAL ARBITARY WAVEFORM GENERATOR OUTPUT DRIVE CIRCUIT

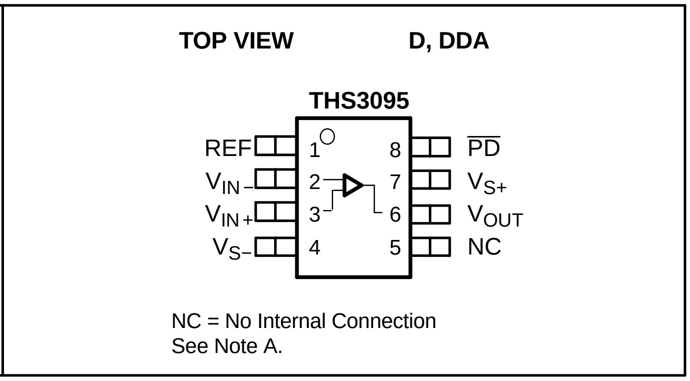


PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



NC = No Internal Connection



NC = No Internal Connection
See Note A.

Note A: The devices with the power−down option defaults to the ON state if no signal is applied to the $\overline{PD}$ pin. Additionallly, the REF pin functional range is from V_{S-} to (V_{S+} − 4 V).

ODERING INFORMATION

PART NUMBER	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS3091D	SOIC-8	Rails, 75
THS3091DR		Tape and Reel, 2500
THS3091DDA	SOIC-8-PP(1)	Rails, 75
THS3091DDAR		Tape and Reel, 2500
Power-down		
THS3095D	SOIC-8	Rails, 75
THS3095DR		Tape and Reel, 2500
THS3095DDA	SOIC-8-PP(1)	Rails, 75
THS3095DDAR		Tape and Reel, 2500

(1) The PowerPAD is electrically isolated from all other pins.

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)(1)	POWER RATING (2) T_J = 125°C	
			T_A = 25°C	T_A = 85°C
D-8	38.3	97.5	1.02 W	410 mW
DDA-8(3)	9.2	45.8	2.18 W	873 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.
(3) The THS3091 and THS3095 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage	Dual supply	±5	±15	V
	Single supply	10	30	
T_A	Operating free-air temperature	-40	85	°C

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

			UNIT
V_{S-} to V_{S+}	Supply voltage		33 V
V_I	Input voltage		± V_S
V_{ID}	Differential input voltage		± 4 V
I_O	Output current		350 mA
	Continuous power dissipation		See Dissipation Ratings Table
T_J	Maximum junction temperature,		150°C
T_J(2)	Maximum junction temperature, continuous operation, long-term reliability		125°C
T_{stg}	Storage temperature		-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
	ESD ratings	HBM	2000
		CDM	1500
		MM	150

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, R_F = 1.21 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/MAX
AC PERFORMANCE								
Small-signal bandwidth, -3 dB	G = 1, R_F = 1.78 kΩ, V_O = 200 mV_{PP}		235				MHz	TYP
	G = 2, R_F = 1.21 kΩ, V_O = 200 mV_{PP}		210					
	G = 5, R_F = 1 kΩ, V_O = 200 mV_{PP}		190					
	G = 10, R_F = 866 Ω, V_O = 200 mV_{PP}		180					
0.1-dB bandwidth flatness	G = 2, R_F = 1.21 kΩ, V_O = 200 mV_{PP}		95					
Large-signal bandwidth	G = 5, R_F = 1 kΩ , V_O = 4 V_{PP}		135					
Slew rate (25% to 75% level)	G = 2, V_O = 10-V step, R_F = 1.21 kΩ		5000				V/µs	TYP
	G = 5, V_O = 20-V step, R_F = 1 kΩ		7300					
Rise and fall time	G = 2, V_O = 5-V_{PP}, R_F = 1.21 kΩ		5				ns	TYP
Settling time to 0.1%	G = -2, V_O = 2 V_{PP} step		42				ns	TYP
Settling time to 0.01%	G = -2, V_O = 2 V_{PP} step		72					
Harmonic distortion								
2nd Harmonic distortion	G = 2, R_F = 1.21 kΩ, V_O = 2 V_{PP}, f = 10 MHz	R_L = 100Ω	66				dBc	TYP
		R_L = 1 kΩ	77					
3rd Harmonic distortion		R_L = 100 Ω	74					
		R_L = 1 kΩ	69					
Input voltage noise	f > 10 kHz		2				nV / $\sqrt{Hz}$	TYP
Noninverting input current noise	f > 10 kHz		14				pA / $\sqrt{Hz}$	TYP
Inverting input current noise	f > 10 kHz		17				pA / $\sqrt{Hz}$	TYP
Differential gain	G = 2, R_L = 150 Ω, R_F = 1.21 kΩ	NTSC	0.013%					TYP
		PAL	0.011%					
Differential phase		NTSC	0.020°					
		PAL	0.026°					
DC PERFORMANCE								
Transimpedance	V_O = ±7.5 V, Gain = 1		850	350	300	300	kΩ	MIN
Input offset voltage	V_{CM} = 0 V		0.9	3	4	4	mV	MAX
Average offset voltage drift					±10	±10	µV/°C	TYP
Noninverting input bias current	V_{CM} = 0 V		4	15	20	20	µA	MAX
Average bias current drift					±20	±20	nA/°C	TYP
Inverting input bias current	V_{CM} = 0 V		3.5	15	20	20	µA	MAX
Average bias current drift					±20	±20	nA/°C	TYP
Input offset current	V_{CM} = 0 V		1.7	10	15	15	µA	MAX
Average offset current drift					±20	±20	nA/°C	TYP
INPUT CHARACTERISTICS								
Common-mode input range			±13.6	±13.3	±13	±13	V	MIN
Common-mode rejection ratio	V_{CM} = ±10 V		78	68	65	65	dB	MIN
Noninverting input resistance			1.3				MΩ	TYP
Noninverting input capacitance			0.1				pF	TYP
Inverting input resistance			30				Ω	TYP
Inverting input capacitance			1.4				pF	TYP

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/ MAX
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 1 kΩ	±13.2	±12.8	±12.5	±12.5	V	MIN
	R_L = 100 Ω	±12.5	±12.1	±11.8	±11.8		
Output current (sourcing)	R_L = 40 Ω	280	225	200	200	mA	MIN
Output current (sinking)	R_L = 40 Ω	250	200	175	175	mA	MIN
Output impedance	f = 1 MHz, Closed loop	0.06				Ω	TYP
POWER SUPPLY							
Specified operating voltage		±15	±16	±16	±16	V	MAX
Maximum quiescent current		9.5	10.5	11	11	mA	MAX
Minimum quiescent current		9.5	8.5	8	8	mA	MIN
Power supply rejection (+PSRR)	V_{S+} = 15.5 V to 14.5 V, V_{S-} = 15 V	75	70	65	65	dB	MIN
Power supply rejection (-PSRR)	V_{S+} = 15 V, V_{S-} = -15.5 V to -14.5 V	73	68	65	65	dB	MIN
POWER-DOWN CHARACTERISTICS (THS3095 ONLY)							
Power-down voltage level	Enable, REF = 0 V	≤				V	MAX
	Power-down , REF = 0 V	≥ 2					
Power-down quiescent current	$\overline{PD}$ = 0V	500	700	800	800	µA	MAX
V_{PD} quiescent current	V_{PD} = 0 V, REF = 0 V,	11	15	20	20	µA	MAX
	V_{PD} = 3.3 V, REF = 0 V	11	15	20	20		
Turnon time delay	90% of final value	60				µs	TYP
Turnoff time delay	10% of final value	150					

ELECTRICAL CHARACTERISTICS

V_S = ±5 V, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/ MAX
AC PERFORMANCE								
Small-signal bandwidth, -3 dB	G = 1, R_F = 1.78 kΩ, V_O = 200 mV_{PP}		190				MHz	TYP
	G = 2, R_F = 1.15 kΩ, V_O = 200 mV_{PP}		180					
	G = 5, R_F = 1 kΩ, V_O = 200 mV_{PP}		160					
	G = 10, R_F = 866 Ω, V_O = 200 mV_{PP}		150					
0.1-dB bandwidth flatness	G = 2, R_F = 1.15 kΩ, V_O = 200 mV_{PP}		65					
Large-signal bandwidth	G = 2, R_F = 1.15 kΩ , V_O = 4 V_{PP}		160					
Slew rate (25% to 75% level)	G = 2, V_O= 5-V step, R_F = 1.21 kΩ		1400				V/µs	TYP
	G = 5, V_O= 5-V step, R_F = 1 kΩ		1900					
Rise and fall time	G = 2, V_O = 5-V step, R_F = 1.21 kΩ		5				ns	TYP
Settling time to 0.1%	G = -2, V_O = 2 V_{PP} step		35				ns	TYP
Settling time to 0.01%	G = -2, V_O = 2 V_{PP} step		73					
Harmonic distortion								
2nd Harmonic distortion	G = 2, R_F = 1.15 kΩ, V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω	77				dBc	TYP
		R_L = 1 kΩ	73					
3rd Harmonic distortion		R_L = 100 Ω	70					
		R_L = 1 kΩ	68					
Input voltage noise	f > 10 kHz		2				nV / √Hz	TYP
Noninverting input current noise	f > 10 kHz		14				pA / √Hz	TYP
Inverting input current noise	f > 10 kHz		17				pA / √Hz	TYP
Differential gain	G = 2, R_L = 150 Ω, R_F = 1.15 kΩ	NTSC	0.027%					TYP
		PAL	0.025%					
Differential phase		NTSC	0.04°					
		PAL	0.05°					
DC PERFORMANCE								
Transimpedance	V_O = ±2.5 V, Gain = 1		700	250	200	200	kΩ	MIN
Input offset voltage	V_{CM} = 0 V		0.3	2	3	3	mV	MAX
Average offset voltage drift					±10	±10	µV/°C	TYP
Noninverting input bias current	V_{CM} = 0 V		2	15	20	20	µA	MAX
Average bias current drift					±20	±20	nA/°C	TYP
Inverting input bias current	V_{CM} = 0 V		5	15	20	20	µA	MAX
Average bias current drift					±20	±20	nA/°C	TYP
Input offset current	V_{CM} = 0 V		1	10	15	15	µA	MAX
Average offset current drift					±20	±20	nA/°C	TYP
INPUT CHARACTERISTICS								
Common-mode input range			±3.6	±3.3	±3	±3	V	MIN
Common-mode rejection ratio	V_{CM} = ±2.0 V, V_O = 0 V		66	60	57	57	dB	MIN
Noninverting input resistance			1.1				MΩ	TYP
Noninverting input capacitance			1.2				pF	TYP
Inverting input resistance			32				Ω	TYP
Inverting input capacitance			1.5				pF	TYP

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/ MAX
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 1 kΩ	±3.4	±3.1	±2.8	±2.8	V	MIN
	R_L = 100 Ω	±3.1	±2.7	±2.5	±2.5		
Output current (sourcing)	R_L = 40 Ω	200	160	140	140	mA	MIN
Output current (sinking)	R_L = 40 Ω	180	150	125	125	mA	MIN
Output impedance	f = 1 MHz, Closed loop	0.09				Ω	TYP
POWER SUPPLY							
Specified operating voltage		±5	±4.5	±4.5	±4.5	V	MAX
Maximum quiescent current		8.2	9	9.5	9.5	mA	MAX
Minimum quiescent current		8.2	7	6.5	6.5	mA	MIN
Power supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 5 V	73	68	63	63	dB	MIN
Power supply rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = –4.5 V to -5.5 V	71	65	60	60	dB	MIN
POWER-DOWN CHARACTERISTICS (THS3095 ONLY)							
Power-down voltage level	Enable, REF = 0 V	≤0.8				V	MAX
	Power-down , REF = 0 V	≥ 2					
Power-down quiescent current	$\overline{PD}$ = 0V	300	500	600	600	µA	MAX
V_{PD} quiescent current	V_{PD} = 0 V, REF = 0 V,	11	15	20	20	µA	MAX
	V_{PD} = 3.3 V, REF = 0 V	11	15	20	20		
Turnon time delay	90% of final value	60				µs	TYP
Turnoff time delay	10% of final value	150					

TYPICAL CHARACTERISTICS

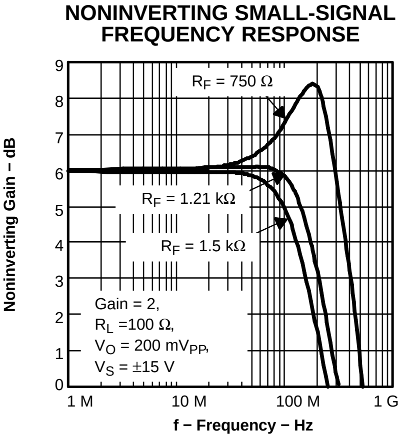
TABLE OF GRAPHS

±15-V GRAPHS		**FIGURE**
Noninverting small-signal frequency response		1, 2
Inverting small-signal frequency response		3
0.1-dB gain flatness frequency response		4
Noninverting large-signal frequency response		5
Inverting large-signal frequency response		6
Capacitive load frequency response		7
Recommended R_{ISO}	vs Capacitive load	8
2nd Harmonic distortion	vs Frequency	9, 11
3rd Harmonic distortion	vs Frequency	10, 12
2nd Harmonic distortion	vs Frequency	13
3rd Harmonic distortion	vs Frequency	14
Harmonic distortion	vs Output voltage swing	15, 16
Slew rate	vs Output voltage step	17, 18, 19
Noise	vs Frequency	20
Settling time		21, 22
Quiescent current	vs Supply voltage	23
Quiescent current	vs Frequency	24
Output voltage	vs Load resistance	25
Input bias and offset current	vs Case temperature	26
Input offset voltage	vs Case temperature	27
Transimpedance	vs Frequency	28
Rejection ratio	vs Frequency	29
Noninverting small-signal transient response		30
Inverting large-signal transient response		31, 32
Overdrive recovery time		33
Differential gain	vs Number of loads	34
Differential phase	vs Number of loads	35
Closed-loop output impedance	vs Frequency	36
Power-down quiescent current	vs Supply voltage	37
Turnon and turnoff time delay		38

TABLE OF GRAPHS

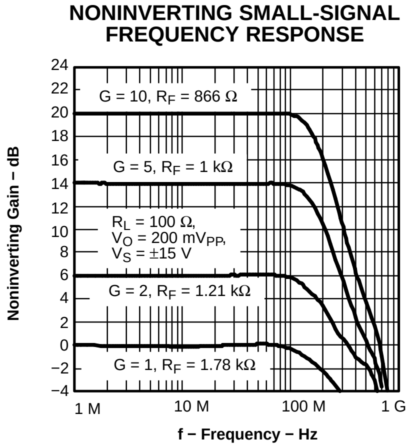
±5-V GRAPHS		**FIGURE**
Noninverting small-signal frequency response		39
Inverting small-signal frequency response		40
0.1-dB gain flatness frequency response		41
Noninverting large-signal frequency response		42
Inverting large-signal frequency response		43
Settling time		44
2nd Harmonic distortion	vs Frequency	45, 47
3rd Harmonic distortion	vs Frequency	46, 48
Harmonic distortion	vs Output voltage swing	49, 50
Slew rate	vs Output voltage step	51, 52, 53
Quiescent current	vs Frequency	54
Output voltage	vs Load resistance	55
Input bias and offset current	vs Case temperature	56
Overdrive recovery time		57
Rejection ratio	vs Frequency	58

TYPICAL CHARACTERISTICS (±15 V)



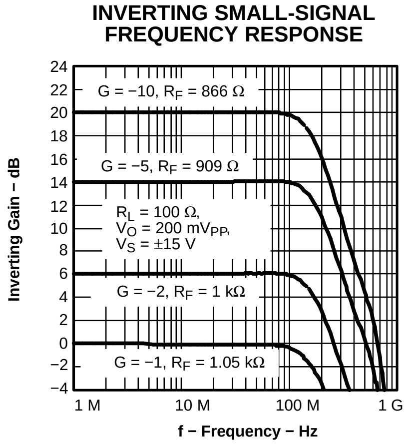
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

Figure 1.



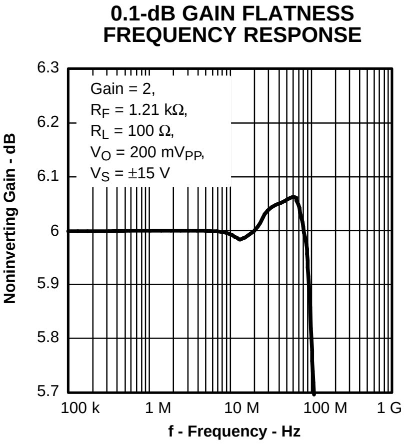
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

Figure 2.



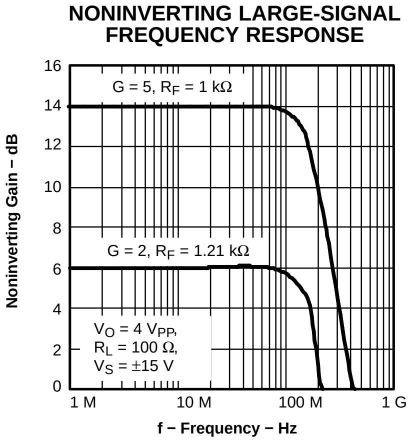
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

Figure 3.



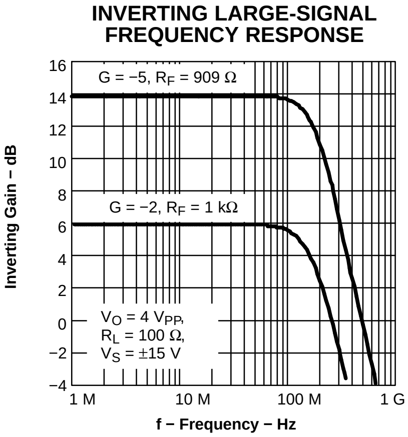
0.1-dB GAIN FLATNESS FREQUENCY RESPONSE

Figure 4.



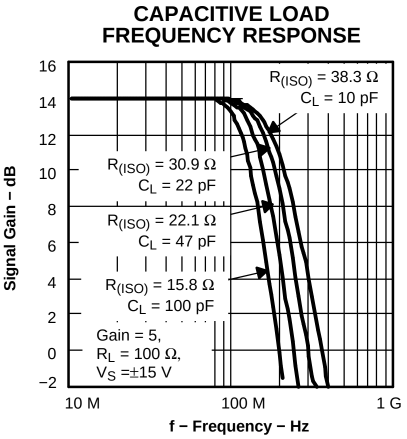
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

Figure 5.



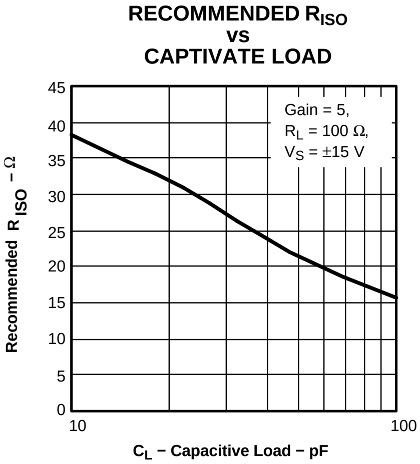
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

Figure 6.



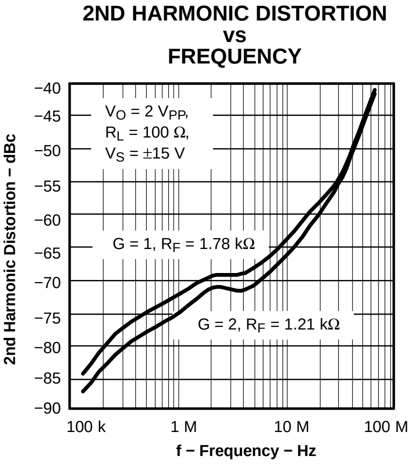
CAPACITIVE LOAD FREQUENCY RESPONSE

Figure 7.



RECOMMENDED R_{ISO} vs CAPTIVATE LOAD

Figure 8.



2ND HARMONIC DISTORTION vs FREQUENCY

Figure 9.

TYPICAL CHARACTERISTICS (±15 V) (continued)

3RD HARMONIC DISTORTION vs FREQUENCY

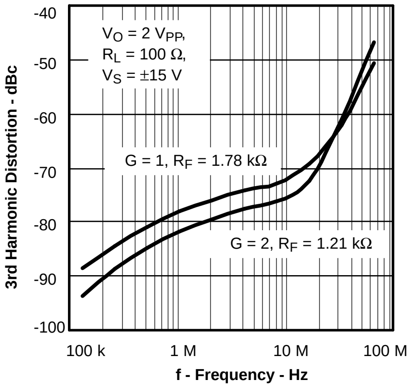


Figure 10.

2ND HARMONIC DISTORTION vs FREQUENCY

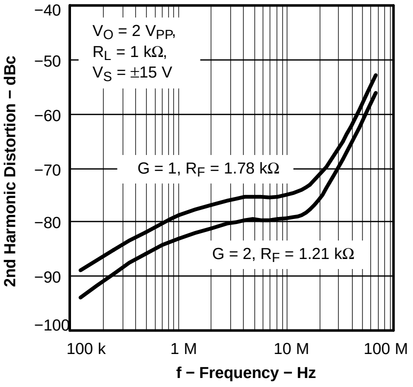


Figure 11.

3RD HARMONIC DISTORTION vs FREQUENCY

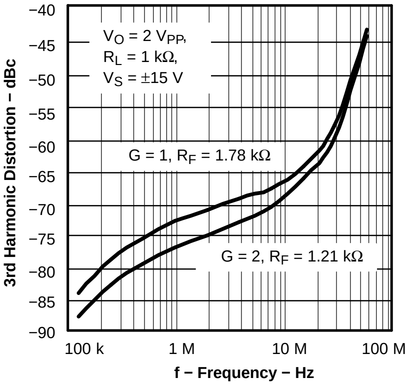


Figure 12.

2ND HARMONIC DISTORTION vs FREQUENCY

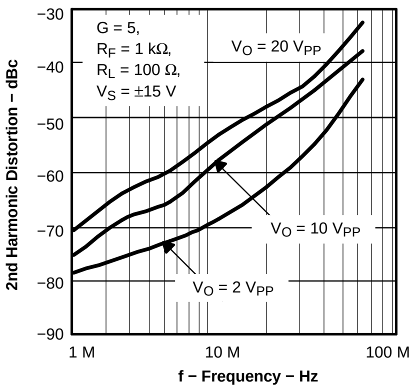


Figure 13.

3RD HARMONIC DISTORTION vs FREQUENCY

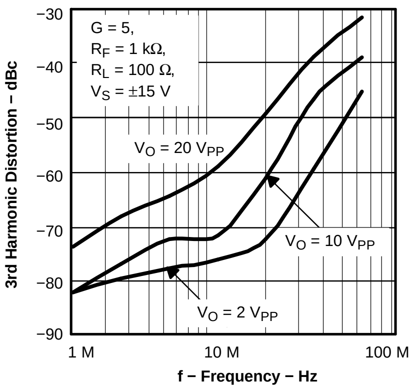


Figure 14.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

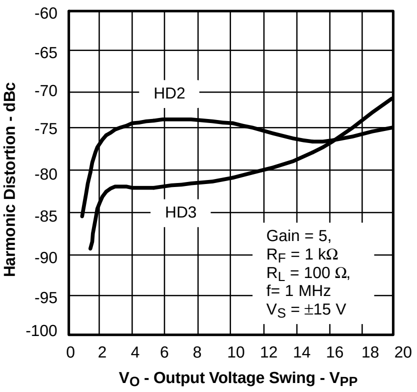


Figure 15.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

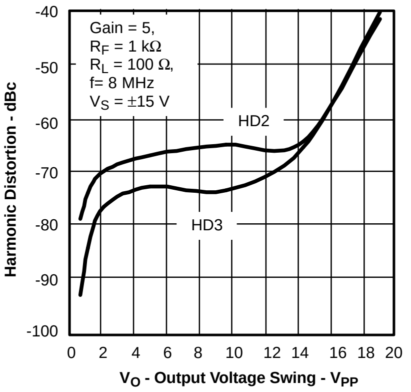


Figure 16.

SLEW RATE vs OUTPUT VOLTAGE STEP

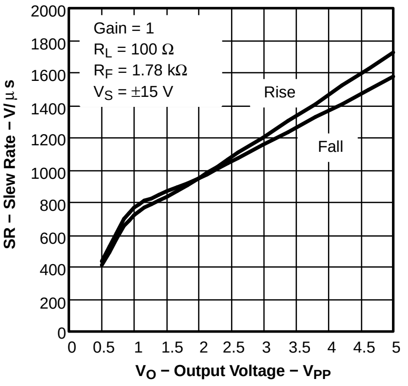


Figure 17.

SLEW RATE vs OUTPUT VOLTAGE STEP

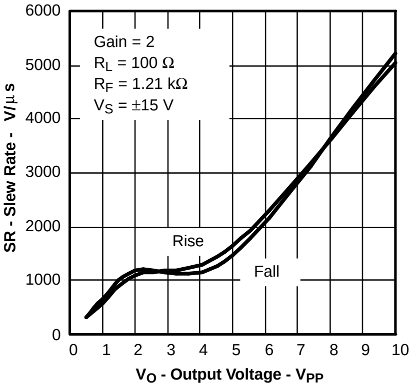


Figure 18.

TYPICAL CHARACTERISTICS (±15 V) (continued)

SLEW RATE
vs
OUTPUT VOLTAGE STEP

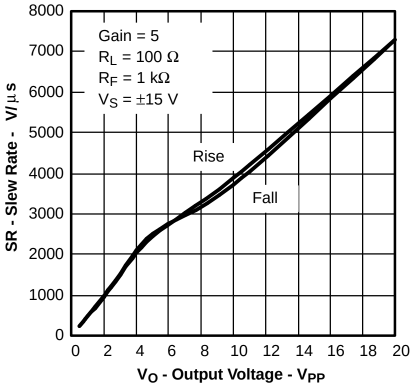


Figure 19.

NOISE
vs
FREQUENCY

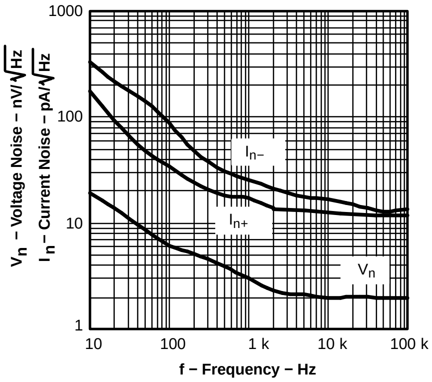


Figure 20.

SETTLING TIME

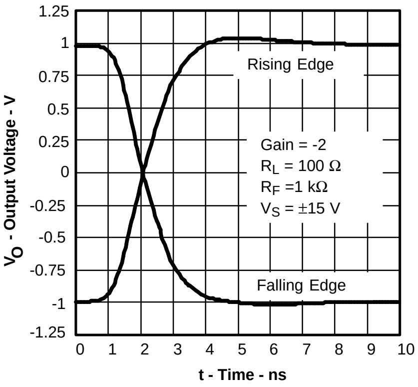


Figure 21.

SETTLING TIME

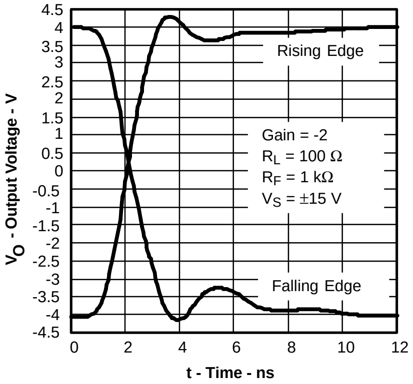


Figure 22.

QUIESCENT CURRENT
vs
SUPPLY VOLTAGE

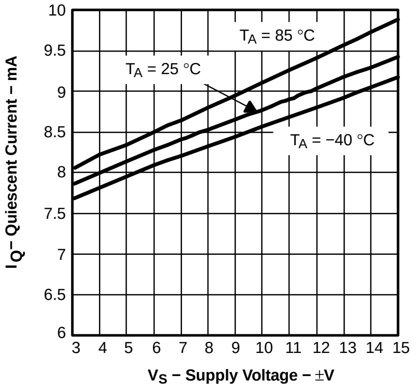


Figure 23.

QUIESCENT CURRENT
vs
FREQUENCY

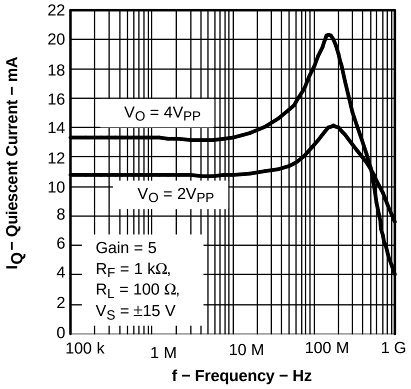


Figure 24.

OUTPUT VOLTAGE
vs
LOAD RESISTANCE

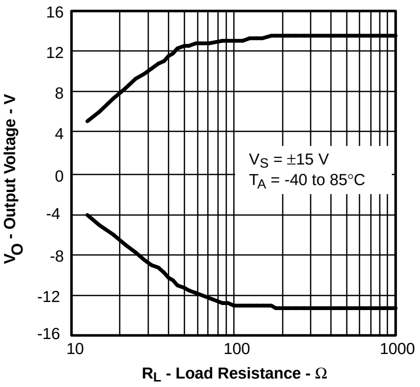


Figure 25.

INPUT BIAS AND
OFFSET CURRENT
vs
CASE TEMPERATURE

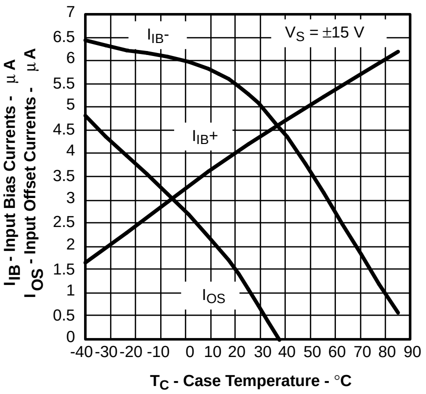


Figure 26.

INPUT OFFSET VOLTAGE
vs
CASE TEMPERATURE

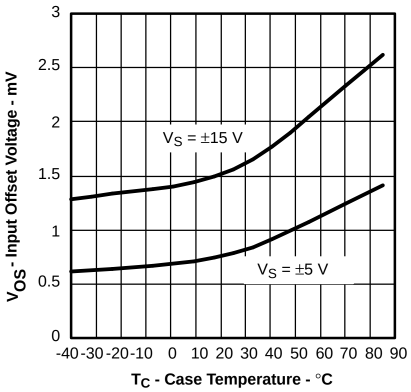


Figure 27.

TYPICAL CHARACTERISTICS (±15 V) (continued)

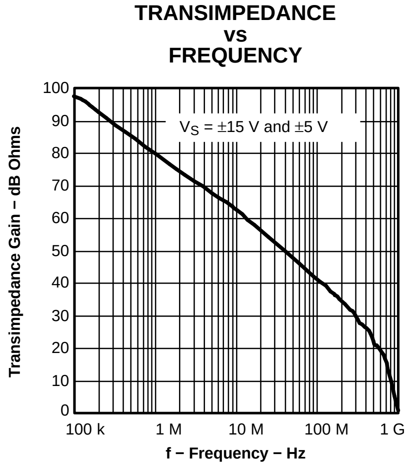


Figure 28.

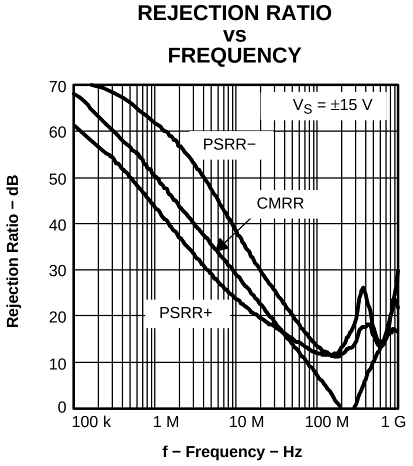


Figure 29.

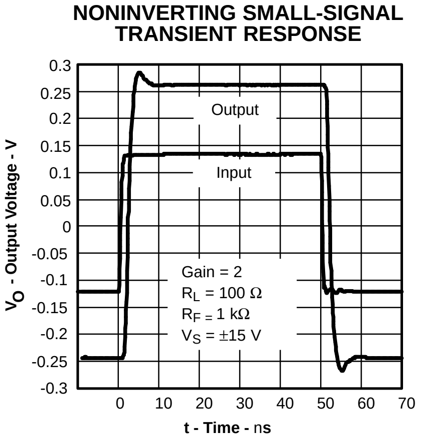


Figure 30.

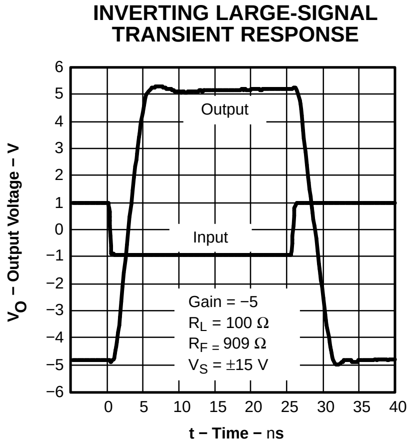


Figure 31.

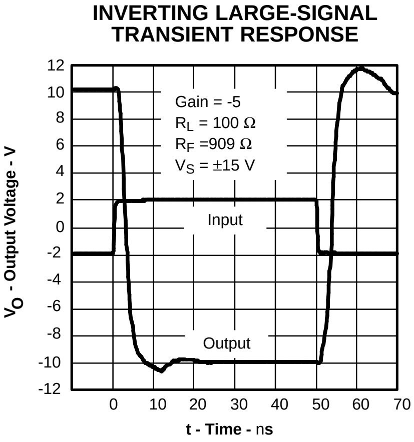


Figure 32.

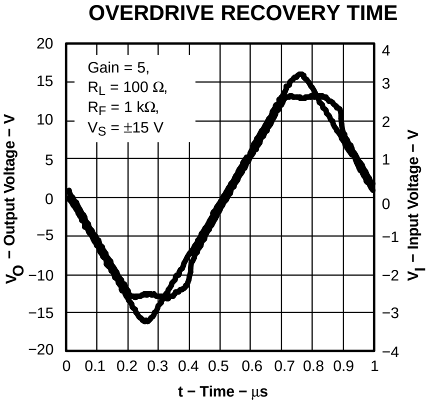


Figure 33.

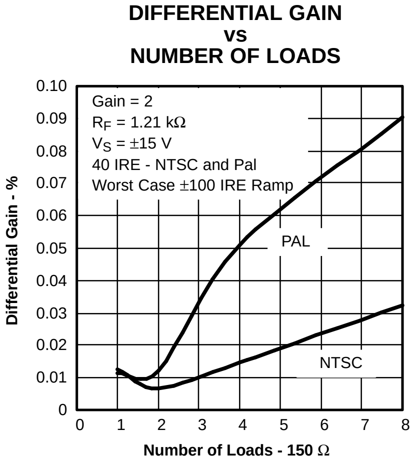


Figure 34.

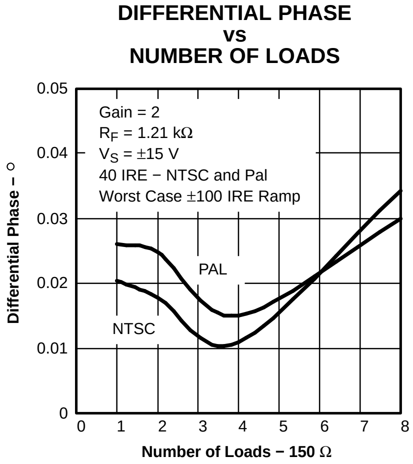


Figure 35.

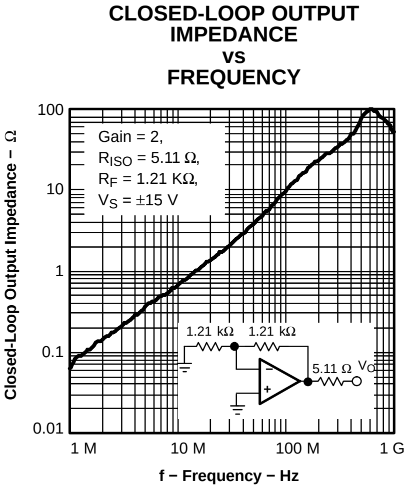


Figure 36.

TYPICAL CHARACTERISTICS (±15 V) (continued)

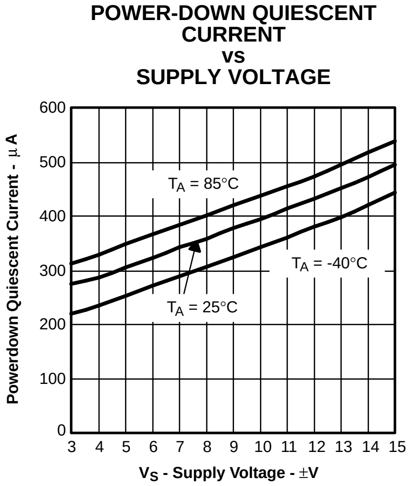


Figure 37.

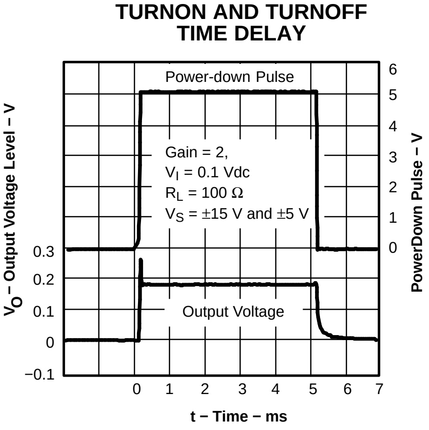


Figure 38.

TYPICAL CHARACTERISTICS (±5 V)

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

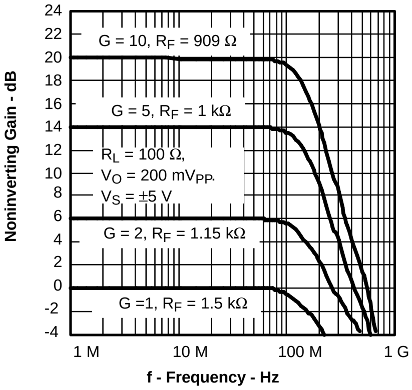


Figure 39.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

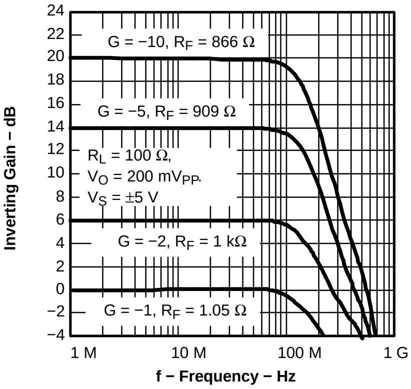


Figure 40.

0.1-dB GAIN FLATNESS FREQUENCY RESPONSE

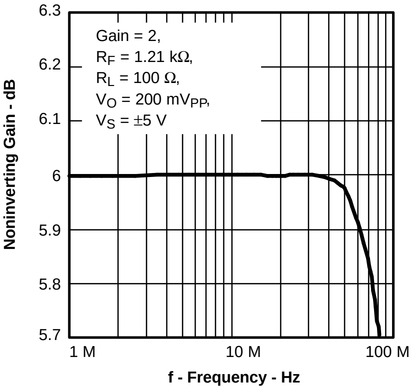


Figure 41.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

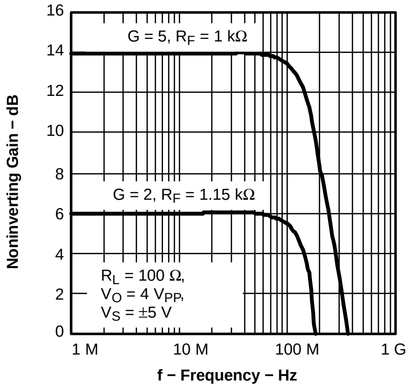


Figure 42.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

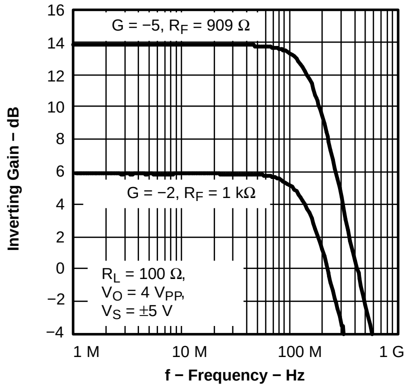


Figure 43.

SETTLING TIME

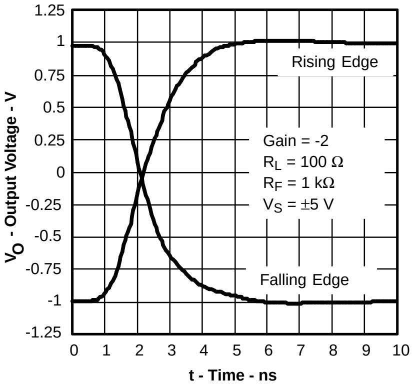


Figure 44.

2ND HARMONIC DISTORTION vs FREQUENCY

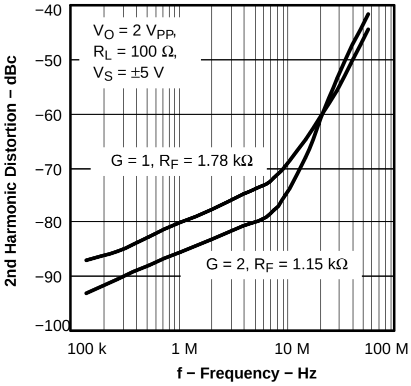


Figure 45.

3RD HARMONIC DISTORTION vs FREQUENCY

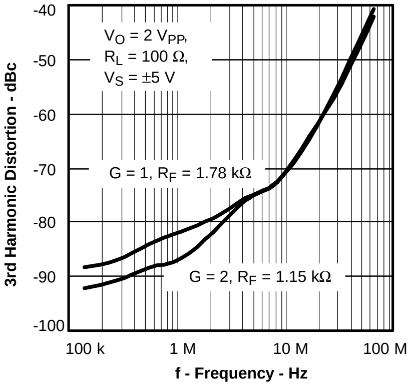


Figure 46.

2ND HARMONIC DISTORTION vs FREQUENCY

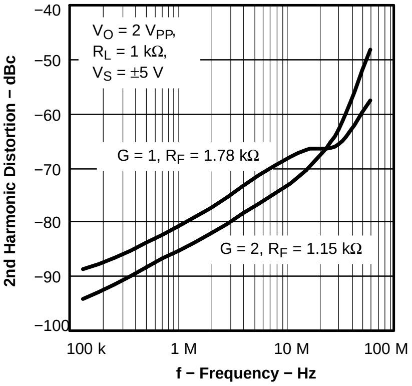


Figure 47.

TYPICAL CHARACTERISTICS (±5 V) (continued)

3RD HARMONIC DISTORTION vs FREQUENCY

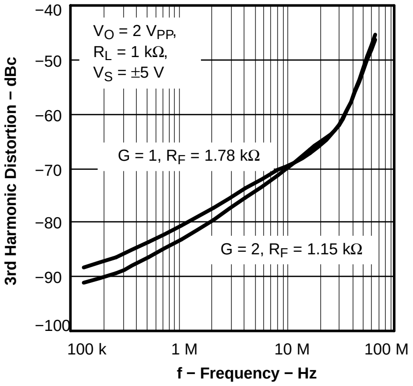


Figure 48.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

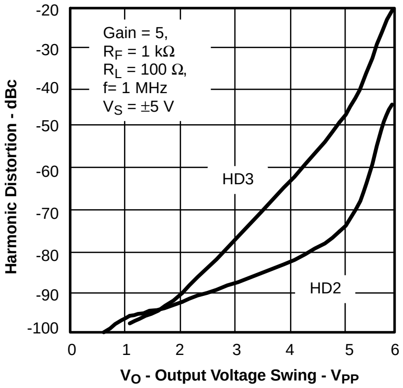


Figure 49.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

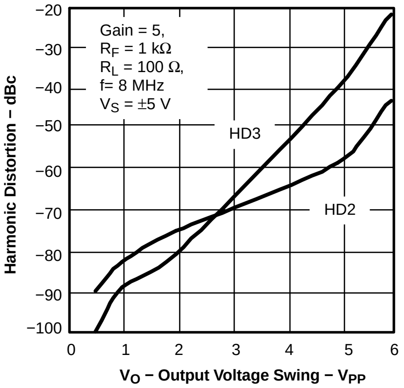


Figure 50.

SLEW RATE vs OUTPUT VOLTAGE STEP

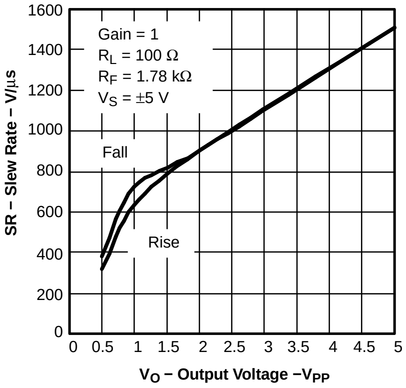


Figure 51.

SLEW RATE vs OUTPUT VOLTAGE STEP

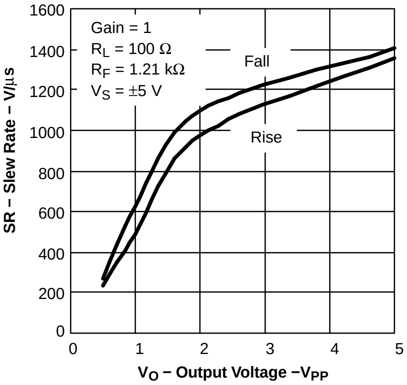


Figure 52.

SLEW RATE vs OUTPUT VOLTAGE STEP

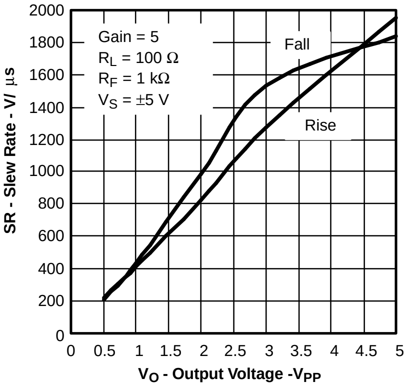


Figure 53.

QUIESCENT CURRENT vs FREQUENCY

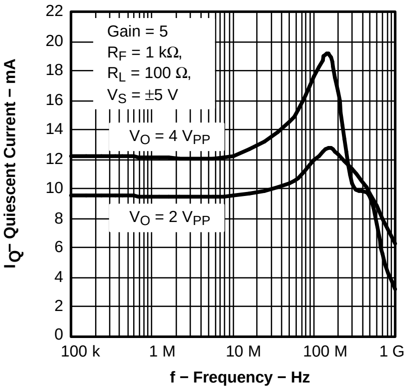


Figure 54.

OUTPUT VOLTAGE vs LOAD RESISTANCE

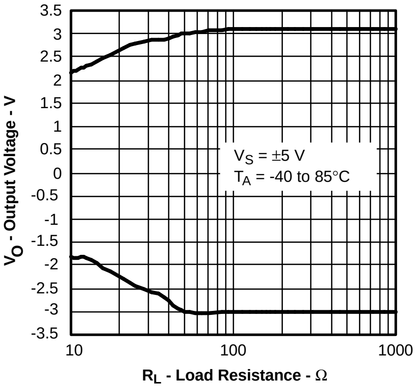


Figure 55.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

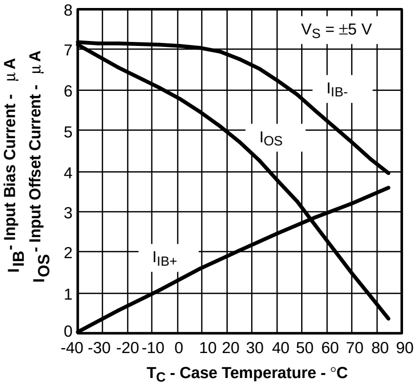


Figure 56.

TYPICAL CHARACTERISTICS (±5 V) (continued)

OVERDRIVE RECOVERY TIME

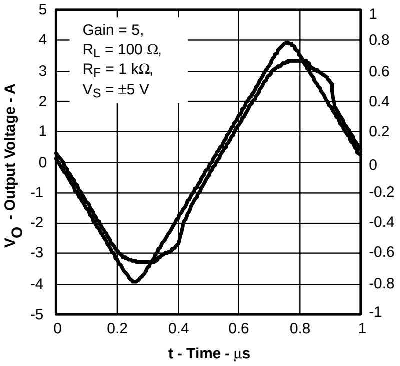


Figure 57.

REJECTION RATIO vs FREQUENCY

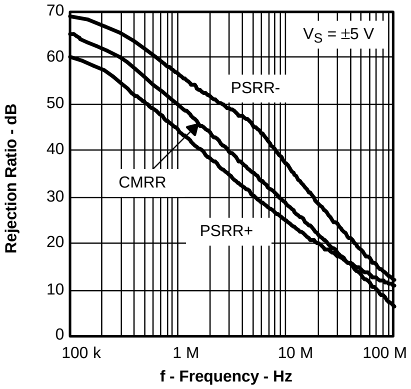


Figure 58.

APPLICATION INFORMATION

WIDEBAND, NONINVERTING OPERATION

The THS3091/5 are unity gain stable 235-MHz current-feedback operational amplifiers, designed to operate from a ±5-V to ±15-V power supply.

Figure 59 shows the THS3091 in a noninverting gain of 2-V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance.

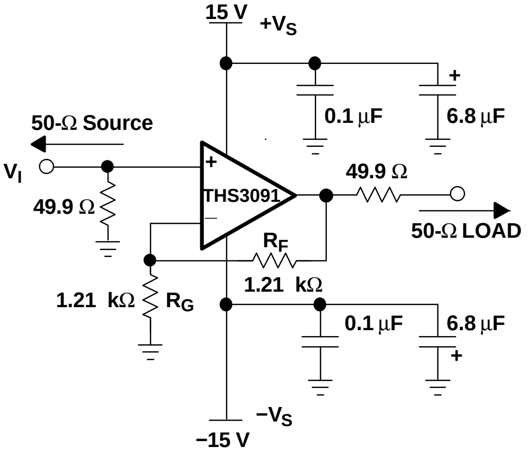


Figure 59. Wideband, Noninverting Gain Configuration

Current-feedback amplifiers are highly dependent on the feedback resistor R_F for maximum performance and stability. Table 1 shows the optimal gain-setting resistors R_F and R_G at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for R_F. Conversely, increasing R_F decreases the bandwidth, but stability is improved.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3091 and THS3095 R_F and R_G values for minimal peaking with R_L = 100 Ω			
GAIN (V/V)	**SUPPLY VOLTAGE (V)**	**R_G (Ω)**	**R_F (Ω)**
1	±15	–	1.78 k
	±5	–	1.78 k
2	±15	1.21 k	1.21 k
	±5	1.15 k	1.15 k
5	±15	249	1 k
	±5	249	1 k
10	±15	95.3	866
	±5	95.3	866
–1	±15 and ±5	1.05 k	1.05 k
–2	±15 and ±5	499	1 k
–5	±15 and ±5	182	909
–10	±15 and ±5	86.6	866

WIDEBAND, INVERTING OPERATION

Figure 60 shows the THS3091 in a typical inverting gain configuration where the input and output impedances and signal gain from Figure 59 are retained in an inverting circuit configuration.

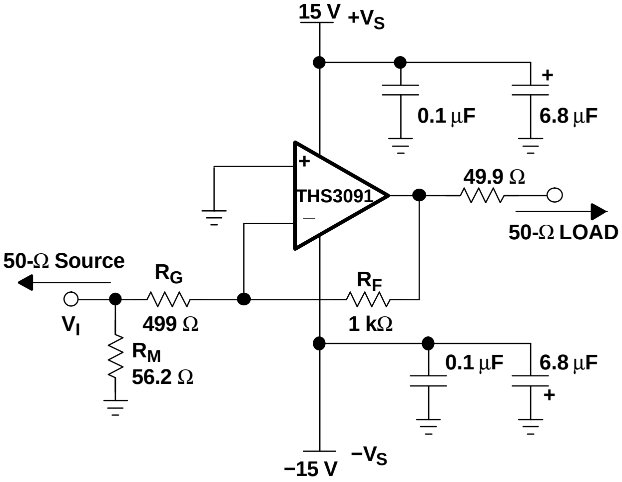


Figure 60. Wideband, Inverting Gain Configuration

SINGLE-SUPPLY OPERATION

The THS3091/5 have the capability to operate from a single-supply voltage ranging from 10 V to 30 V. When operating from a single power supply, biasing the input and output at mid-supply allows for the maximum output voltage swing. The circuits shown in Figure 61 show inverting and noninverting amplifiers configured for single-supply operations.

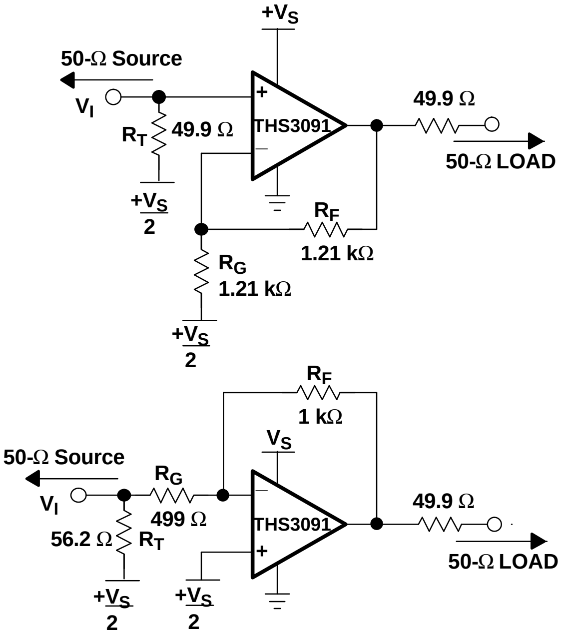


Figure 61. DC-Coupled, Single-Supply Operation

Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS3091/5 matches the demands for video distribution for delivering video signals down multiple cables. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal, and supports component video and RGB video signals that require fast transition times and fast settling times for high signal quality.

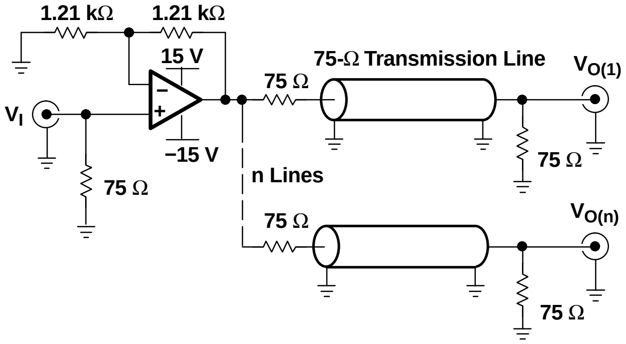


Figure 62. Video Distribution Amplifier Application

Driving Capacitive Loads

Applications such as FET line drivers can be highly capacitive and cause stability problems for high-speed amplifiers.

Figure 63 through Figure 68 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier's feedback path. See Figure 63 for recommended resistor values versus capacitive load.

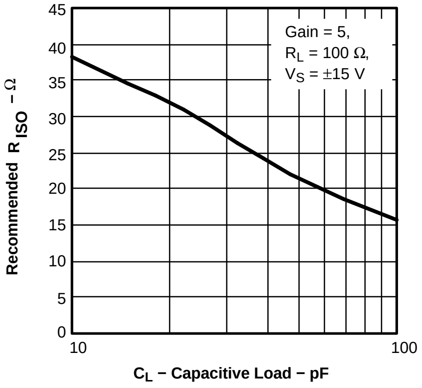


Figure 63. Recommended R_{ISO} vs Capacitive Load

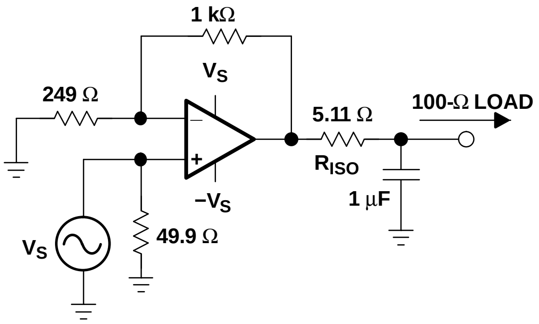


Figure 64.

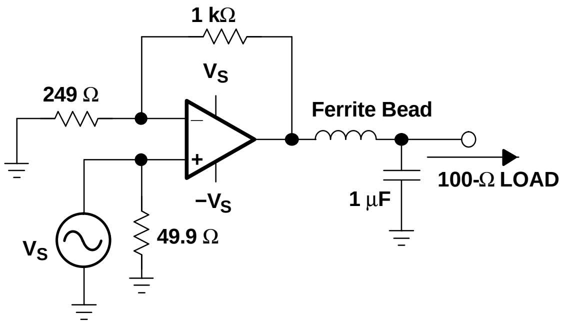


Figure 65.

Placing a small series resistor, R_{ISO}, between the amplifier's output and the capacitive load, as shown in Figure 64, is an easy way of isolating the load capacitance.

Using a ferrite chip in place of R_{ISO}, as shown in Figure 65, is another approach of isolating the output of the amplifier. The ferrite's impedance characteristic versus frequency is useful to maintain the low-frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. Use a ferrite with similar impedance to R_{ISO}, 20 Ω - 50 Ω, at 100 MHz and low impedance at dc.

Figure 66 shows another method used to maintain the low-frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. At low frequency, feedback is mainly from the load side of R_{ISO}. At high frequency, the feedback is mainly via the 27-pF capacitor. The resistor R_{IN} in series with the negative input is used to stabilize the amplifier and should be equal to the recommended value of R_F at unity gain. Replacing R_{IN} with a ferrite of similar impedance at about 100 MHz as shown in Figure 67 gives similar results with reduced dc offset and low-frequency noise. (See the *ADDITIONAL REFERENCE MATERIAL* section for expanding the usability of current-feedback amplifiers.)

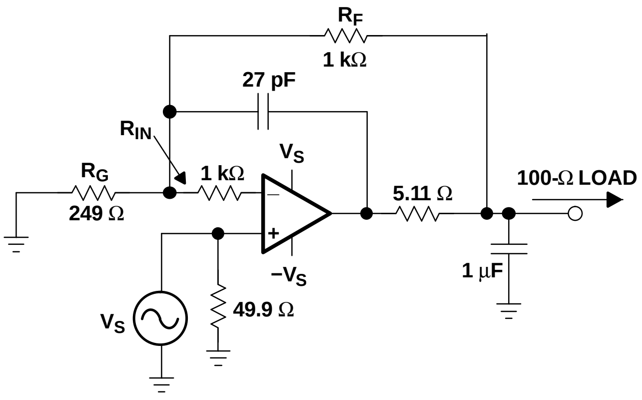


Figure 66.

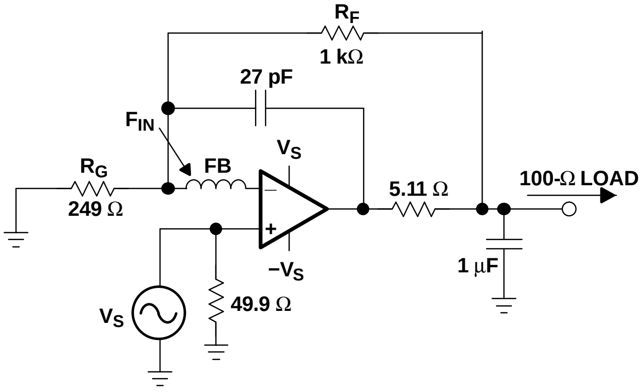


Figure 67.

Figure 68 is shown using two amplifiers in parallel to double the output drive current to larger capacitive loads. This technique is used when more output current is needed to charge and discharge the load faster like when driving large FET transistors.

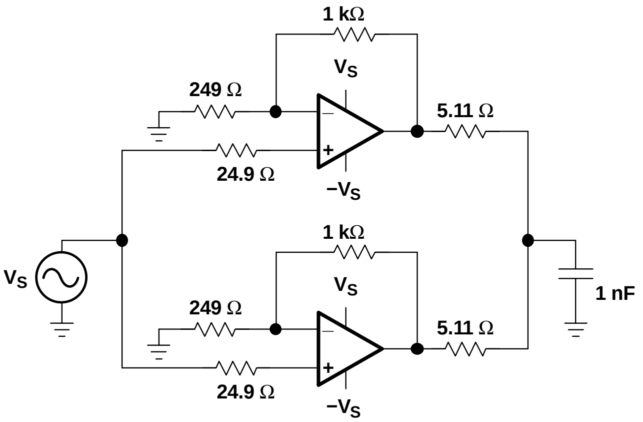


Figure 68.

Figure 69 shows a push-pull FET driver circuit typical of ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.

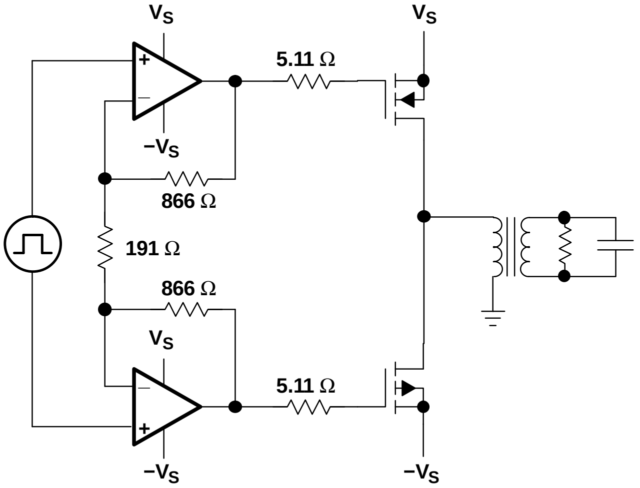


Figure 69. PowerFET Drive Circuit

SAVING POWER WITH POWER-DOWN FUNCTIONALITY AND SETTING THRESHOLD LEVELS WITH THE REFERENCE PIN

The THS3095 features a power-down pin (PD) which lowers the quiescent current from 9.5 mA down to 500 µA, ideal for reducing system power.

The power-down pin of the amplifier defaults to the negative supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the positive rail. The threshold voltages for power-on and power-down are relative to the supply rails and are given in the specification tables. Below the *Enable Threshold Voltage*, the device is on. Above the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

Figure 70 shows the total system output impedance which includes the amplifier output impedance in parallel with the feedback plus gain resistors, which cumulate to 2380 Ω. Figure 59 shows this circuit configuration for reference.

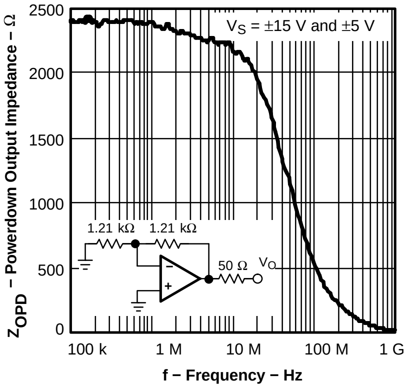


Figure 70. Power-down Output Impedance vs Frequency

As with most current feedback amplifiers, the internal architecture places some limitations on the system when in power-down mode. Most notably is the fact that the amplifier actually turns *ON* if there is a ±0.7 V or greater difference between the two input nodes (V+ and V-) of the amplifier. If this difference exceeds ±0.7 V, the output of the amplifier creates an output voltage equal to approximately [(V+ - V-) -0.7 V]×Gain. This also implies that if a voltage is applied to the output while in power-down mode, the V- node voltage is equal to $V_{O(applied)} \times R_G/(R_F + R_G)$. For low gain configurations and a large applied voltage at the output, the amplifier may actually turn *ON* due to the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach either 10% or 90% of the final output voltage. The time delays are in the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

POWER-DOWN REFERENCE PIN OPERATION

In addition to the power-down pin, the THS3095 features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. In most split-supply applications, the reference pin is connected to ground. In either case, the user needs to be aware of voltage-level thresholds that apply to the power-down pin. The usable range at the REF pin is from V_{S-} to (V_{S+} - 4 V).

PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with a high-frequency amplifier, like the THS3091/5, requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25 in.) from the power supply pins to high-frequency 0.1-µF and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 µF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
- Careful selection and placement of external components preserve the high-frequency performance of the THS3091/5. Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wirebound type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2 kΩ, this parasitic capacitance can add a pole and/or a zero that can effect circuit operation. Keep resistor values as low as possible, consistent with load-driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or

through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S because the THS3091/5 are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an RS are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3091/5 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

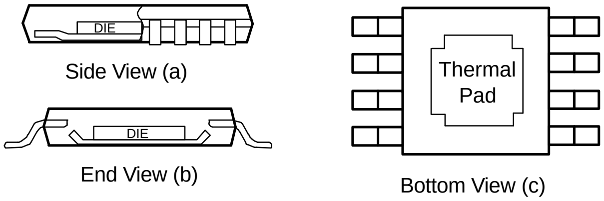
- Socketing a high-speed part like the THS3091/5 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3091/5 parts directly onto the board.

PowerPAD™ DESIGN CONSIDERATIONS

The THS3091/5 are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe on which the die is mounted [see Figure 71(a) and Figure 71(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 71(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that devices such as the THS3091/5 have no electrical connection between the PowerPAD and the die.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



Side View (a)
End View (b)
Bottom View (c)

Figure 71. Views of Thermal Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

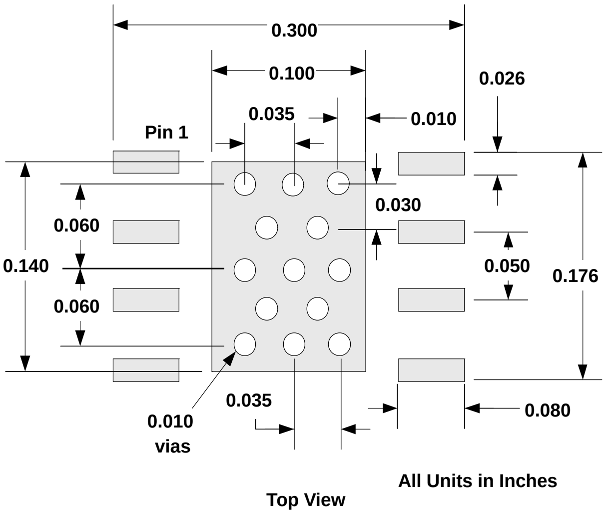


Figure 72. DDA PowerPAD PCB Etch and Via Pattern

PowerPAD™ LAYOUT CONSIDERATIONS

1. PCB with a top-side etch pattern is shown in Figure 72. There should be etch for the leads as well as etch for the thermal pad.
2. Place 13 holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS3091/5 IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane. Note that the PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage such as V_{S-} is acceptable as there is no electrical connection to the silicon.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3091/5 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its 13 holes exposed. The bottom-side solder mask should cover the 13 holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The THS3091/5 incorporates automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately 160°C. When the junction temperature reduces to approximately 140°C, the amplifier turns on again. But, for maximum performance and reliability, the designer must ensure that the design does not exeed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).

T_{max} is the absolute maximum junction temperature (°C).

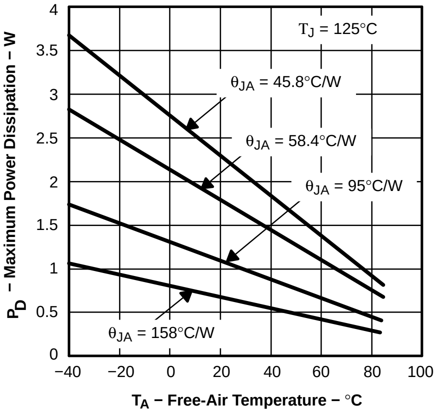
T_A is the ambient temperature (°C).

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).

θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS3091 and THS3095 are offered in an 8-pin SOIC (DDA) with PowerPAD package. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note (literature number SLMA002). The following graph also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3”x 3”
θJ_A = 45.8°C/W for 8-Pin SOIC w/PowerPAD (DDA)
θJ_A = 58.4°C/W for 8-Pin MSOP w/PowerPAD (DGN)
θJ_A = 95°C/W for 8-Pin SOIC High−K Test PCB (D)
θJ_A = 158°C/W for 8-Pin MSOP w/PowerPAD w/o Solder

Figure 73. Maximum Power Distribution vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Evaluation Fixtures, Spice Models, and Application Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, an evaluation board has been developed for the THS3091/5 operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments Web site, www.ti.com, or through your local Texas Instruments sales representative.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS3091/5 is available through the Texas Instruments Web site (www.ti.com). The Product Information Center (PIC) is also available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

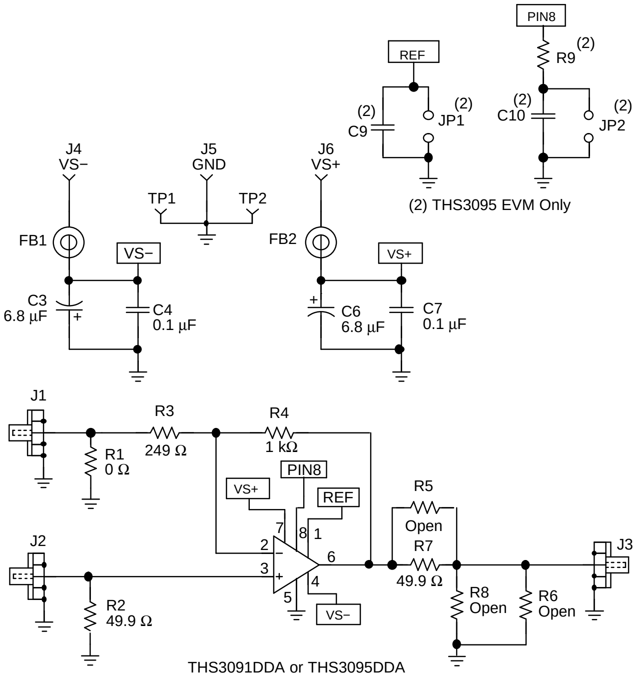


Figure 74. THS3091 EVM Circuit Configuration

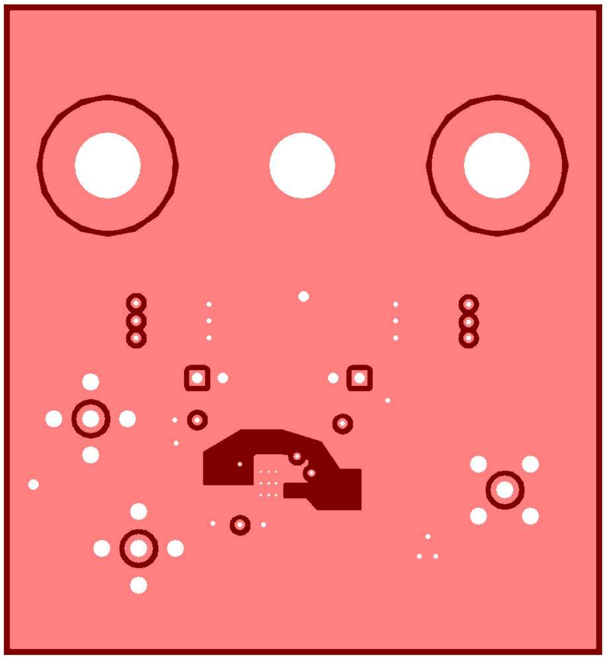


Figure 76. THS3091 EVM Board Layout (Second and Third Layers)

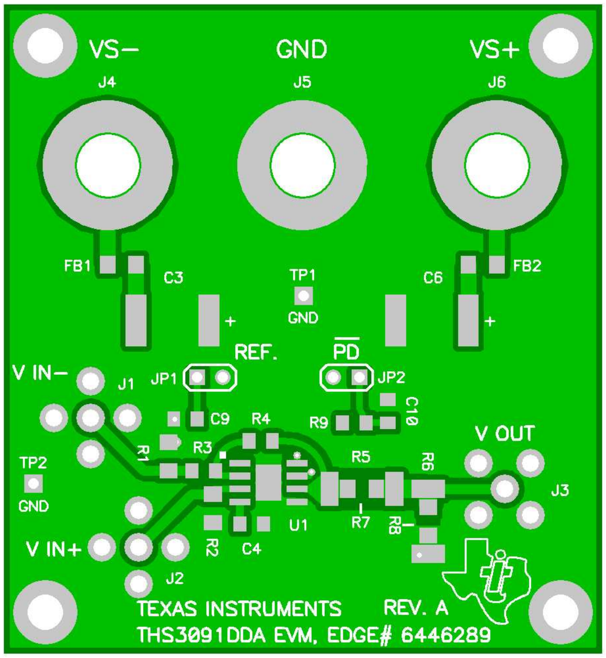


Figure 75. THS3091 EVM Board Layout (Top Layer)

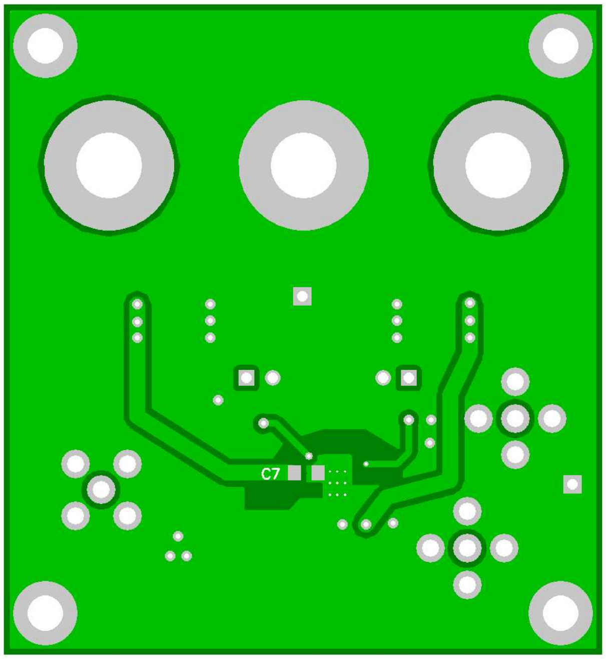


Figure 77. THS3091 EVM Board Layout (Bottom Layer)

Table 2. Bill of Materials

THS3091DDA and THS3095DDA EVM(1)						
ITEM	**DESCRIPTION**	**SMD SIZE**	**REFERENCE DESIGNATOR**	**PCB QTY**	**MANUFACTURER'S PART NUMBER**	**DISTRIBUTOR'S PART NUMBER**
1	Bead, Ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi-Key) 240-1010-1-ND
2	Cap, 6.8 µF, Tanatalum, 50 V, 10%	D	C3, C6	2	(AVX) TAJD685K050R	(Garrett) TAJD685K050R
3	Cap, 0.1 µF, ceramic, X7R, 50 V	0805	C9, C10	2(2)	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
4	Cap, 0.1 µF, ceramic, X7R, 50 V	0805	C4, C7	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
5	Resistor, 0 Ω, 1/8 W, 1%	0805	R9	1(2)	(KOA) RK73Z2ALTD	(Garrett) RK73Z2ALTD
6	Resistor, 249 Ω, 1/8 W, 1%	0805	R3	1	(KOA) RK73H2ALTD2490F	(Garrett) RK73H2ALTD2490F
7	Resistor, 1 kΩ, 1/8 W, 1%	0805	R4	1	(KOA) RK73H2ALTD1001F	(Garrett) RK73H2ALTD1001F
8	Open	1206	R8	1		
9	Resistor, 0 Ω, 1/4 W, 1%	1206	R1	1	(KOA) RK73Z2BLTD	(Garrett) RK73Z2BLTD
10	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R2, R7	2	(KOA) RK73Z2BLTD49R9F	(Garrett) RK73Z2BLTD49R9F
11	Open	2512	R5, R6	2		
12	Header, 0.1-inch centers, 0.025-inch square pins		JP1, JP2	2 (2)	(Sullins) PZC36SAAN	(Digi-Key) S1011-36-ND
13	Connector, SMA PCB Jack		J1, J2, J3	3	(Amphenol) 901-144-8RFX	(Newark) 01F2208
14	Jack, banana receptacle, 0.25-inch. dia. hole		J4, J5, J6	3	(SPC) 813	(Newark) 39N867
15	Test point, black		TP1, TP2	2	(Keystone) 5001	(Digi-Key) 5001K-ND
16	Standoff, 4-40 hex, 0.625-inch length			4	(Keystone) 1808	(Newark) 89F1934
17	Screw, Phillips, 4-40, 0.25-inch			4	SHR-0440-016-SN	
18	IC, THS3091(3) IC, THS3095(2)		U1	1	(TI) THS3091DDA(3) (TI) THS3095DDA(2)	
19	Board, printed-circuit			1	(TI) EDGE # 6446289 Rev. A(3) (TI) EDGE # 6446290 Rev. A(2)	

(1) All items are designated for both the THS3091DDA and THS3095 EVMs unless otherwise noted.
(2) THS3095 EVM only.
(3) THS3091 EVM only.

ADDITIONAL REFERENCE MATERIAL

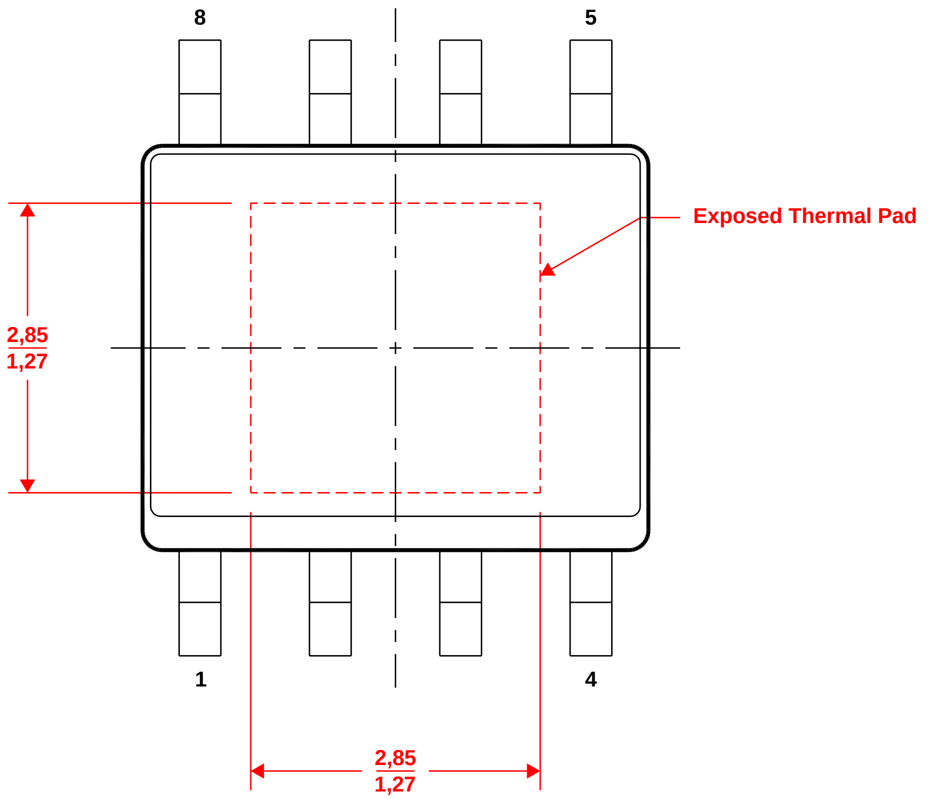
- PowerPAD™ Made Easy, application brief (SLMA004)
- PowerPAD™ Thermally Enhanced Package, technical brief (SLMA002)
- Voltage Feedback vs Current Feedback Amplifiers, (SLVA051)
- Current Feedback Analysis and Compensation (SLOA021)
- Current Feedback Amplifiers: Review, Stability, and Application (SBOA081)
- Effect of Parasitic Capacitance in Op Amp Circuits (SLOA013)
- Expanding the Usability of Current-Feedback Amplifiers, 3Q 2003 Analog Applications Journal (www.ti.com/sc/analogapps).

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



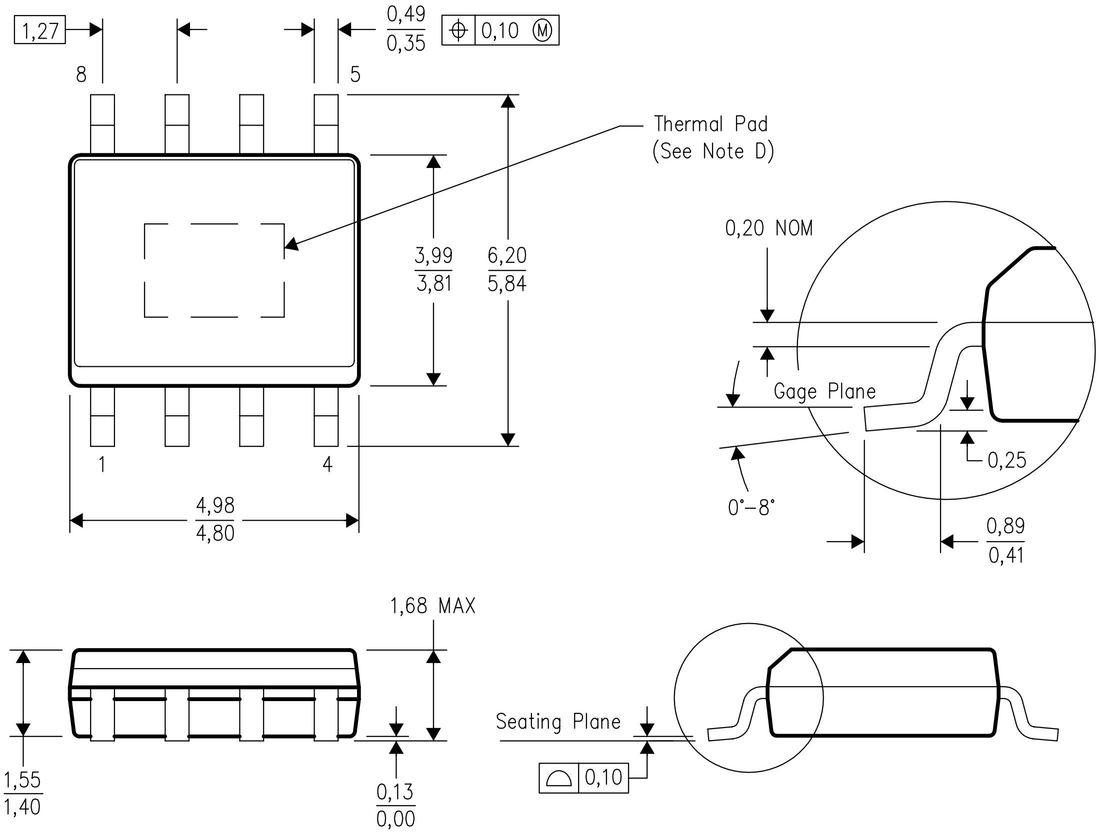
Top View

NOTE: All linear dimensions are in millimeters

PPTD042

Exposed Thermal Pad Dimensions

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

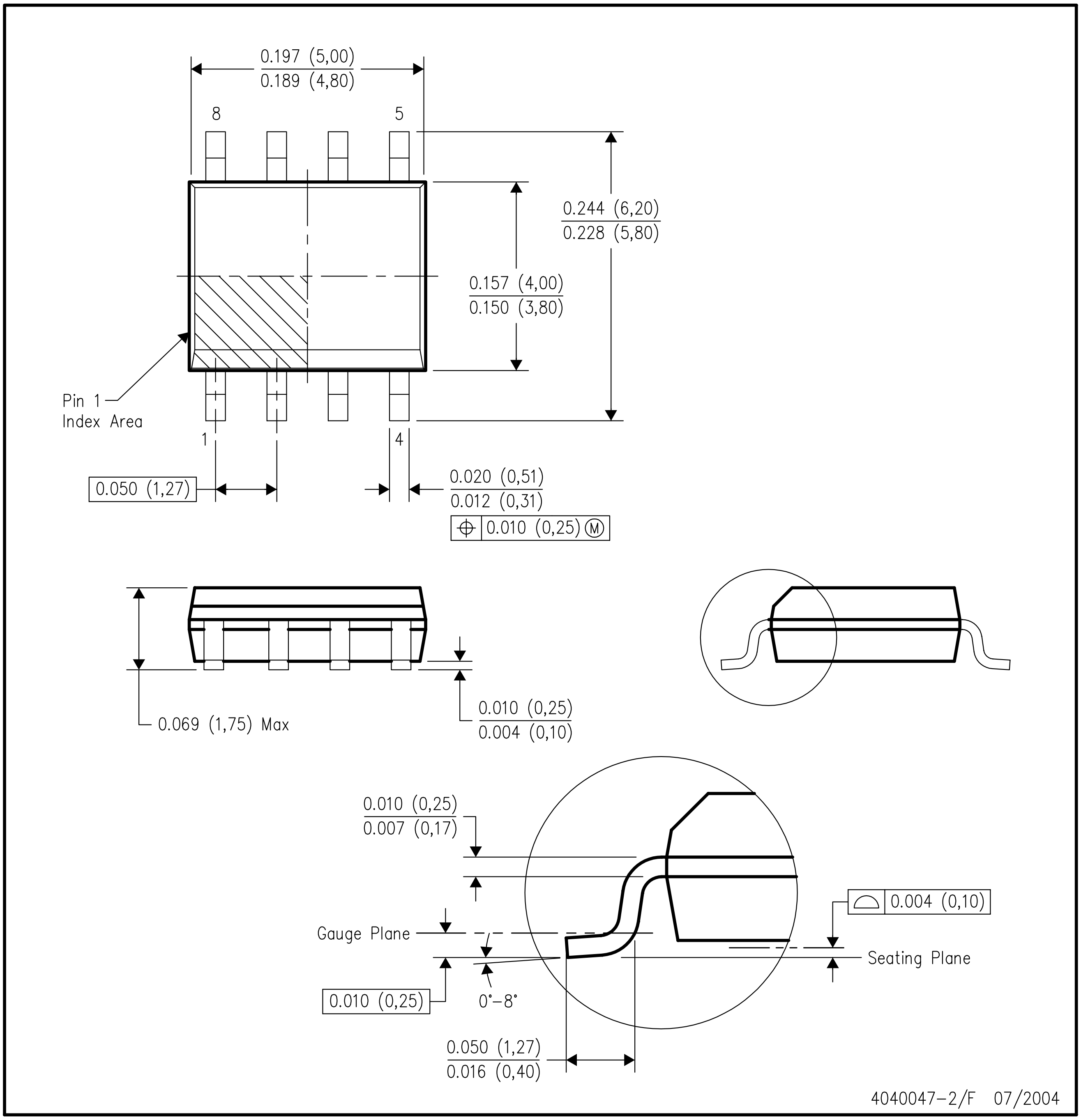


4202561/D 04/04

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.

PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AA.

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