

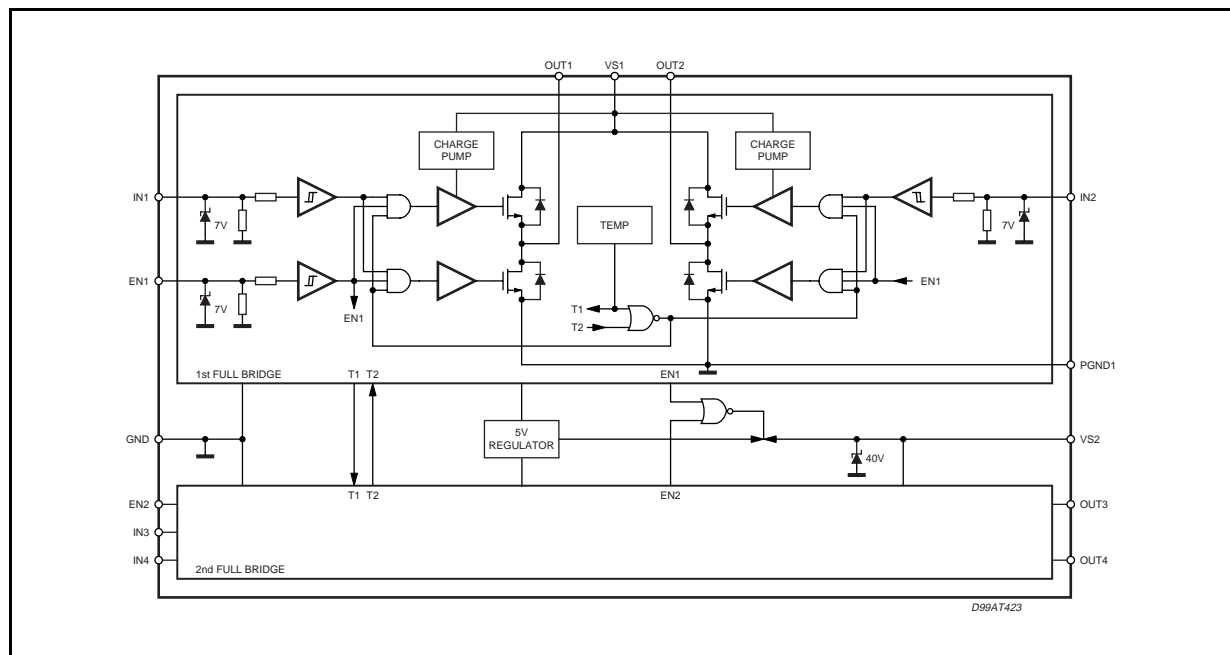
DMOS DUAL FULL BRIDGE DRIVER

- 2 INDEPENDENTLY CONTROLLED H-BRIDGES
- $R_{DS,ON} < 0.9\Omega$ @ $T_{amb} = 25^\circ C$, $V_s = 14V$
- 0.8A DC CURRENT WITHOUT HEAT SINK
- LOW QUIESCENT MODE $I_q < 200\mu A$
- THERMAL PROTECTION
- CROSS CONDUCTION PROTECTION
- SUPPLY VOLTAGE UP TO 40V
- CMOS COMPATIBLE INPUTS
- OUTPUT SHORT-CIRCUIT PROTECTION

DESCRIPTION

The L9925 is a dual full bridge driver for stepper motor applications. Realized in BCD (Bipolar, CMOS & DOS) technology, logic circuits, precise linear blocks and power transistors are combined to optimize circuit performance and minimize off chip components. Schmitt triggers are used for all input stages and are fully compatible with 5V CMOS logic levels. When both enable signals are low, the IC is commanded to a low quiescent current state and will draw less than 200 μA from the battery.

BLOCK DIAGRAM



The charge pump is integrated on chip; no external components are required. Full performance is maintained for $9V < V_s < 16V$. Extended ranges of $6V < V_s < 9V$ and $16V < V_s < 40V$ yields full functionality but with relaxed performance. Over temperature protection and ESD protection to all pins ensures reliability and reduces system integration failures.

ABSOLUTE MAXIMUM RATINGS

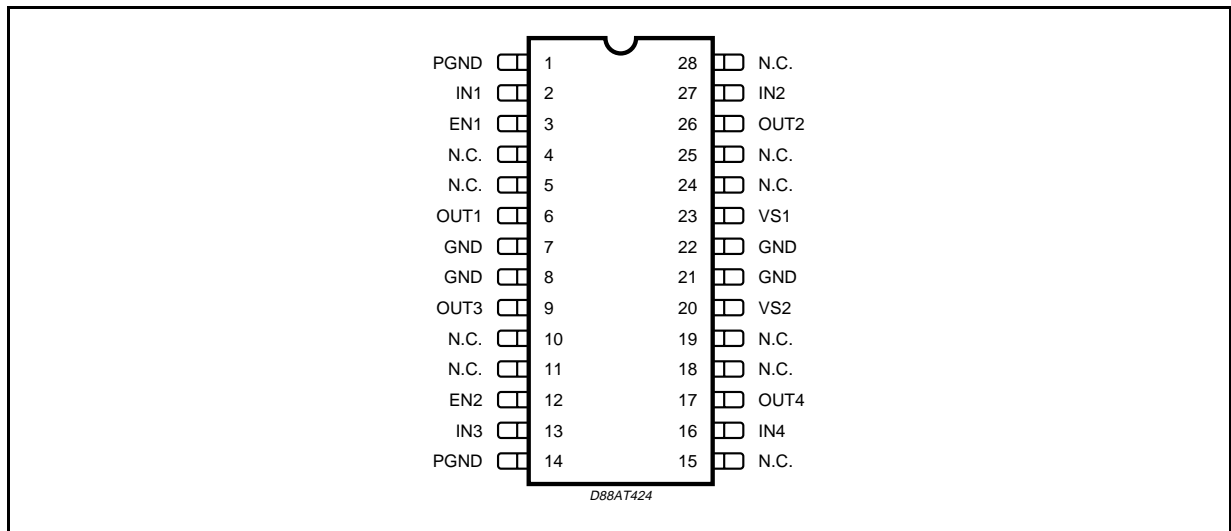
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition isn't implied.

For voltages and currents applied externally to the device:

| Symbol | Parameter | Value | Unit |
|-----------------------------------|--|----------------|-------------|
| V _{VSDC} | Dc Supply Voltage | -0.3 to 26 | V |
| V _{VSP} | Supply Voltage Pulse (T ≤ 400ms) ⁽¹⁾ | 40 | V |
| I _{OUT} | DC Output Load Current | ±1.2 | A |
| I _{OUT MAX} | DC Output Current: for V _{OUT} > V _{VS} + 0.3V or V _{OUT} < -0.3V the internal DMOS reverse and/or substrate diode become conductive and the applied current should not exceed the specified limit. | ±1.8 | A |
| V _{IN1,2} | DC Input Voltage | -0.3 to 7 | V |
| V _{EN} | Enable Input Voltage | -0.3 to 7 | V |
| T _{stg} , T _j | Storage and Junction Temperature | -40 to 150 | °C |
| P _{tot} | Total Power Dissipation (T _{pins} = 80°C) (T _{amb} = 70°C no copper area on PCB) (T _{amb} = 70°C 8cm ² copper area on PCB) | 5 1.23 2 | W W W |

(1) Device may be overstressed if pulsed simultaneous with short circuit at one or more of the outputs will be present.

PIN CONNECTION



THERMAL DATA

| Symbol | Parameter | Value | Unit |
|------------------------|--|-------|------|
| T _{jTS} | Thermal Shut-down junction temperature min. | 150 | °C |
| T _{jTSH} | Thermal Shut-down threshold hysteresis typ. | 25 | °C |
| R _{th j-amb} | Thermal Resistance Junction-ambient ⁽²⁾ | 50 | °C/W |
| R _{th j-pins} | Thermal Resistance Junction-pins | 15 | °C/W |

⁽²⁾ With 6cm² on board heat sink area

PIN FUNCTIONS

| N. | Name | Function |
|--------|-------|--|
| 1 | PGND1 | Ground for DMOS sources in bridge 1 |
| 2 | IN1 | Digital Input from motor controller for bridge 1 |
| 3 | EN1 | Logic enable/disable for bridge 1 (active high) |
| 4, 5 | NC | No connect |
| 6 | OUT1 | Output of one half of bridge 1 |
| 7, 8 | GND | Ground |
| 9 | OUT3 | Output of one half of bridge 2 |
| 10, 11 | NC | No connect |
| 12 | EN2 | Logic enable/disable for bridge 2 (active high) |
| 13 | IN3 | Digital Input from motor controller for bridge 2 |
| 14 | PGND2 | Ground for DMOS sources in bridge 2 |
| 15 | NC | No connect |
| 16 | IN4 | Digital Input from motor controller for bridge 2 |
| 17 | OUT4 | Output of one half of bridge 2 |
| 18, 19 | NC | No connect |
| 20 | VS2 | Supply Voltage for bridge 2 |
| 21, 22 | GND | Ground |
| 23 | VS1 | Supply Voltage for bridge 1 |
| 24, 25 | NC | No connect |
| 26 | OUT2 | Output of one half of bridge 1 |
| 27 | IN2 | Digital Input from motor controller for bridge 1 |
| 28 | NC | No connect |

ELECTRICAL CHARACTERISTICS ($V_s = 9$ to 16V; $T_j = -40$ to 150°C⁽³⁾, unless otherwise specified.)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|-----------------------------------|------------------------------|---|------|------|------|------|
| I _s | Quiescent Current | EN1 = EN2 = 0V; T _j = 85°C | | | 200 | μA |
| | | EN1 = EN2 = 5V; I _{load} = 0A | | 5 | 12 | mA |
| R _{ds} | Switch on Resistance | T _j = 25°C; V _s = 14V; I _o = 300mA | | 0.75 | 0.8 | Ω |
| | | T _j = 125°C; V _s = 6V; I _o = 300mA | | 1.5 | 1.9 | Ω |
| T _{d-on} | Turn-on delay | See Fig 1 | | 10 | 50 | μs |
| T _{d-SB} | Standby setting time | See Fig 1 | | 50 | 200 | μs |
| T _{d-off} | Turn-off delay | See Fig 1 | | 10 | 50 | μs |
| t _{rise} | Output rise time (10 to 90%) | See Fig 1 | 0.5 | 5 | 20 | μs |
| t _{fall} | Output fall time (90 to 10%) | See Fig 1 | 0.5 | 5 | 20 | μs |
| I _{Lo} | Output leakage current | EN = 0V; V _o = V _s or GND | -10 | | 10 | mA |
| IN _x , EN _x | Logic Input Low voltage | | -0.3 | | 1.5 | V |
| | Logic Input High voltage | | 3.5 | | 6 | V |
| | Hysteresis | | 0.5 | 1.0 | 2.0 | V |
| I _{bias} | Input bias current | | -50 | | 300 | μA |

The voltage referred to GND and currents are assumed positive, when the current flows into the pin.

(3) Tested up to 125°C, parameter guaranteed by correlation up to 150°C

Logic Levels

All inputs are positive, non inverting logic

| Logic State | Voltage Range |
|-------------|---------------|
| 0 | -0.3 to 1.5V |
| 1 | 3.5 to 6.0V |

Truth Table

Enable/ Disable

| EN1 | EN0 | Bridge 1 | Bridge 2 | Iq |
|-----|-----|----------|----------|--------|
| 0 | 0 | Disabled | Disabled | <200μA |
| 0 | 1 | Disabled | Enabled | <12mA |
| 1 | 0 | Enabled | Disabled | <12mA |
| 1 | 1 | Enabled | Enabled | <12mA |

General Operation

With the bridge enabled, each input INx, maps directly to the corresponding output OUTx.

The output voltage will be equal to the difference between the supply rail and the product of the load current and the on resistance of the output switch. $V_{out} = V_{supply} - (R_{DS,ON} \cdot I_{LOAD})$.

Sourced load currents are positive.

| IN1 | OUT1 | IN2 | OUT2 | IN3 | OUT3 | IN4 | OUT4 |
|-----|------|-----|------|-----|------|-----|------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | Vs | 1 | Vs | 1 | Vs | 1 | Vs |

Figure 1. Timing Diagram

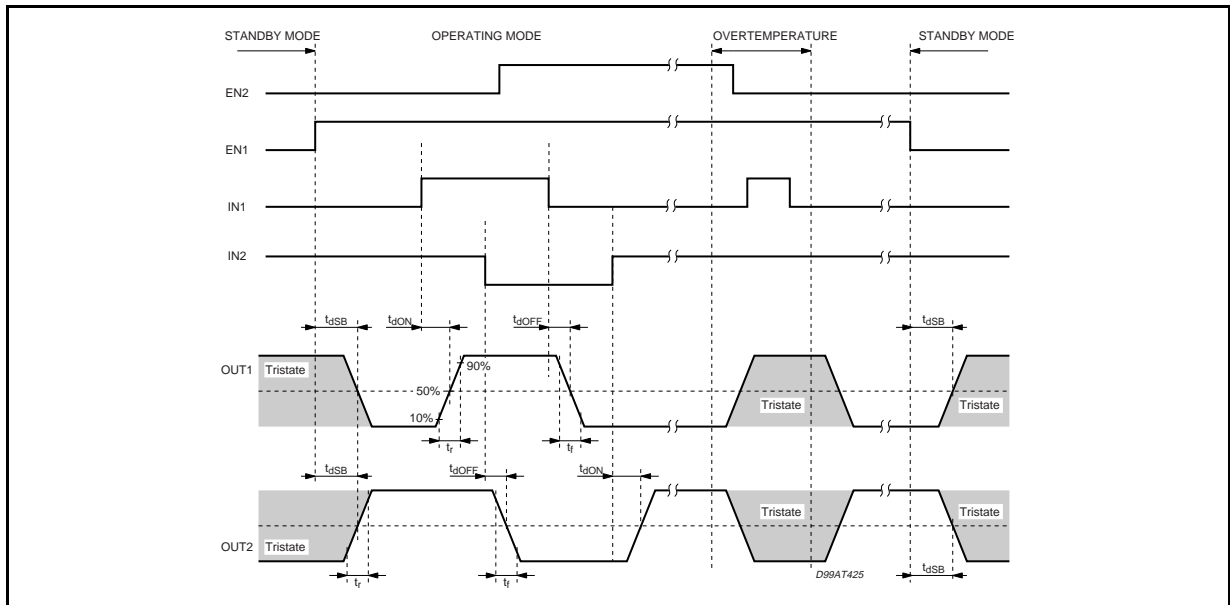


Figure 2. Typical RON - Characteristics of Source and Sink Stage

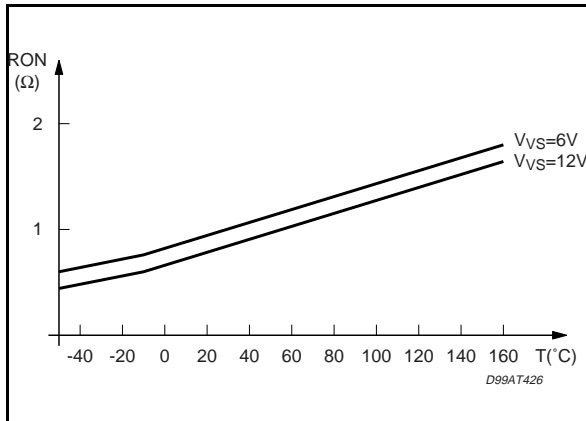


Figure 3. ON - Resistance vs Supply Voltage

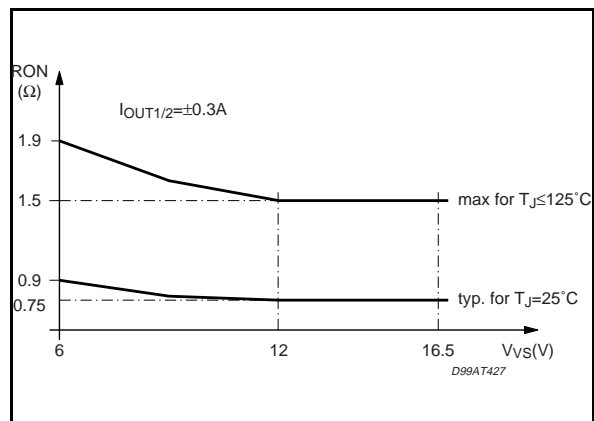


Figure 4. Application Diagram

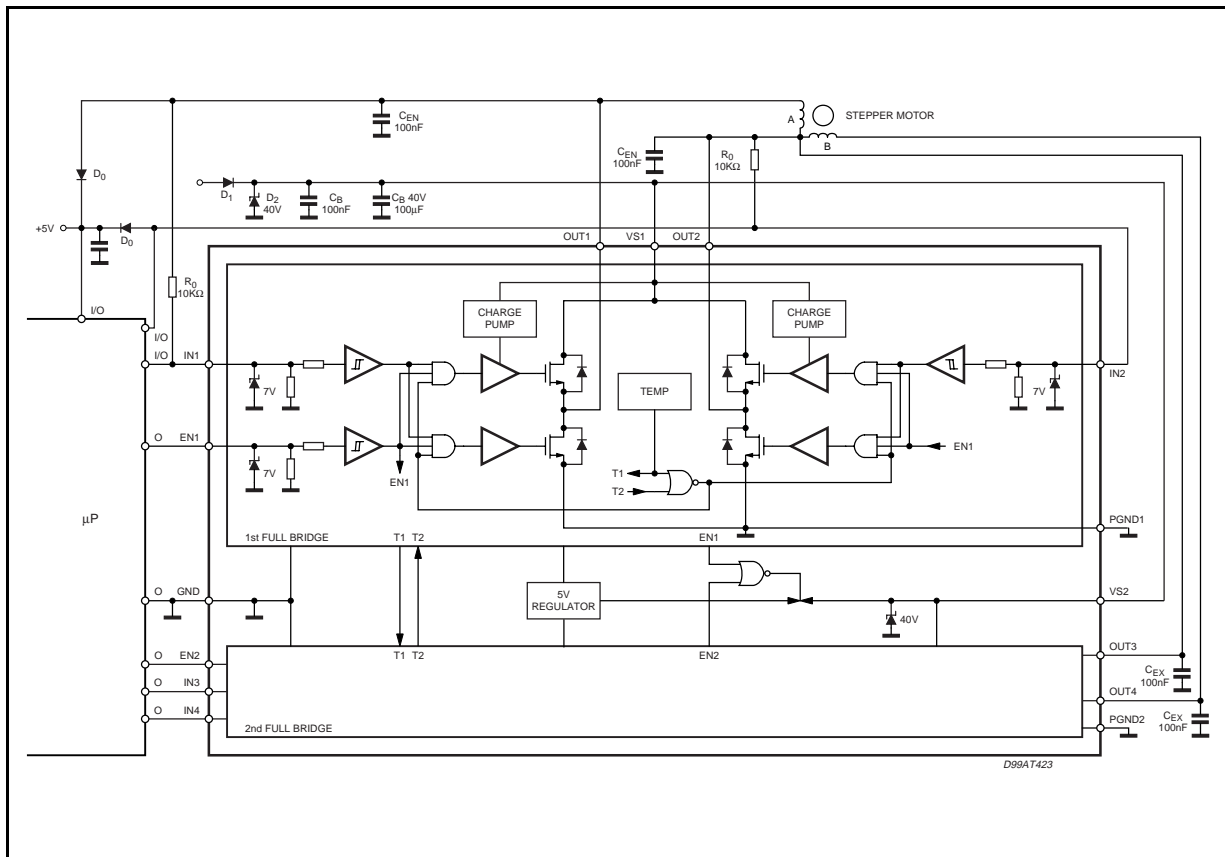


Figure 4 shows a typical application diagram for DC motor driving. To assure the safety of the circuit in the reverse battery condition a reverse protection diode D1 is necessary. The transient protection diode D2 must assure that the maximum supply voltage Vs during the transients at the VBAT line will be limited to a value lower than the absolute maximum ratings for VSP. The capacities CB are used to lower Vs-EMR and its values depend on the driving load.

The resistance feedback loop realized by R0 limited to the µP power supply line by the diode D0 allows open load detection. To protect the device at the outputs against EMI or ESD > 2KV external capacitors Cex may be used.

CIRCUIT DESCRIPTION

L9925 is a dual full bridge IC designed to drive DC motors, stepper motors and other inductive loads. Each bridge has 4 power DMOS transistor with RDSon = 0.75Ω and the relative protection and control circuitry (see fig. 5). The 4 half bridges can be controlled independently by means of the 4 inputs IN1, IN3, IN4 and 2 enable inputs ENABLE1 and ENABLE2.

LOGIC DRIVE (true table for the two full bridges)

| | INPUTS | | OUTPUT MOSFETS |
|---------------|------------------|------------------|---|
| | IN1 IN3 | IN2 IN4 | |
| EN1 = EN2 = H | L L H H | L H L H | Sink 1, Sink2 Sink1, Source2 Source1, Sink2 Source1, Source2 |
| @Tj > 150°C | X | X | All transistors turned OFF |
| EN1 = EN2 = L | X | X | All transistors turned OFF |

L = Low; H = High; X = Don't care

CROSS CONDUCTION

The device guarantees the absence of cross-conduction by watching internal gate-source voltage of the driving power DMOS.

TRANSISTOR OPERATION

ON STATE

When one of POWER DMOS transistors is ON it can be considered as a resistor RDS(ON) = 0.75Ω at a junction temperature of 25°C



In this condition the dissipated power is given by:

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows.

The power dissipation during this period is given by:

$$P_{OFF} = V_S \cdot I_{DSS}$$

Figure 5a. Two phase chopping

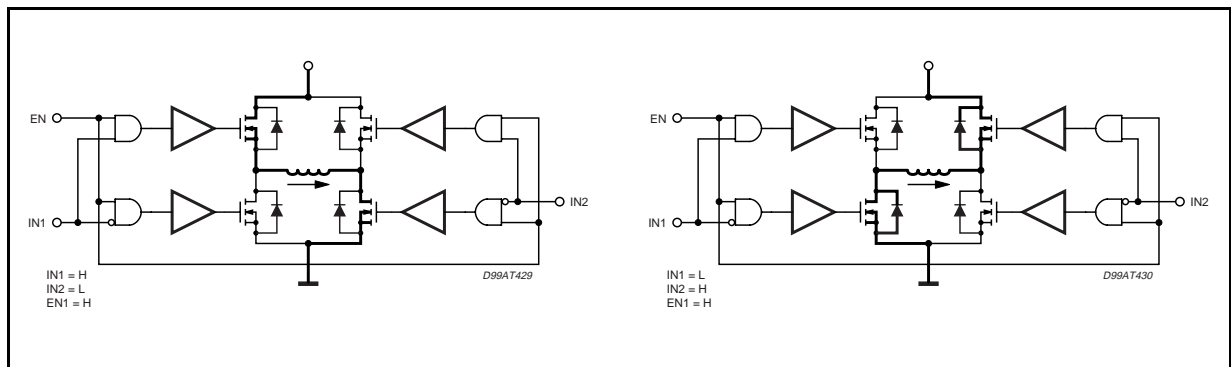


Figure 5b. One phase chopping

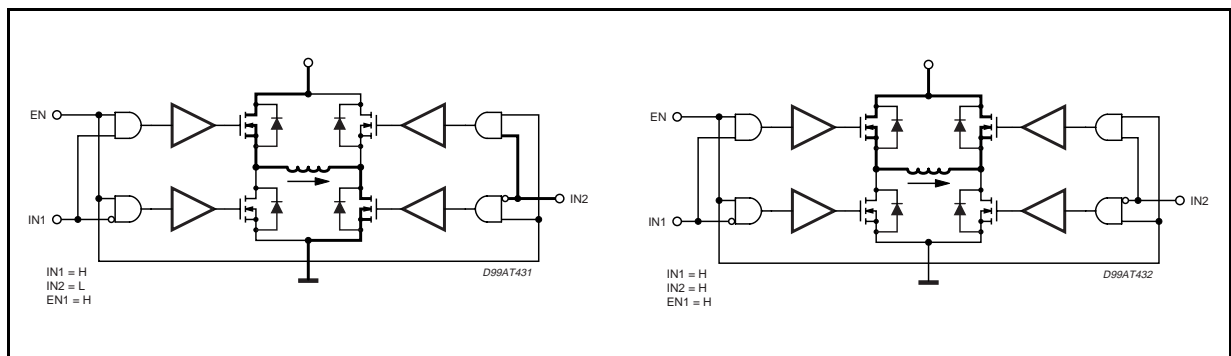
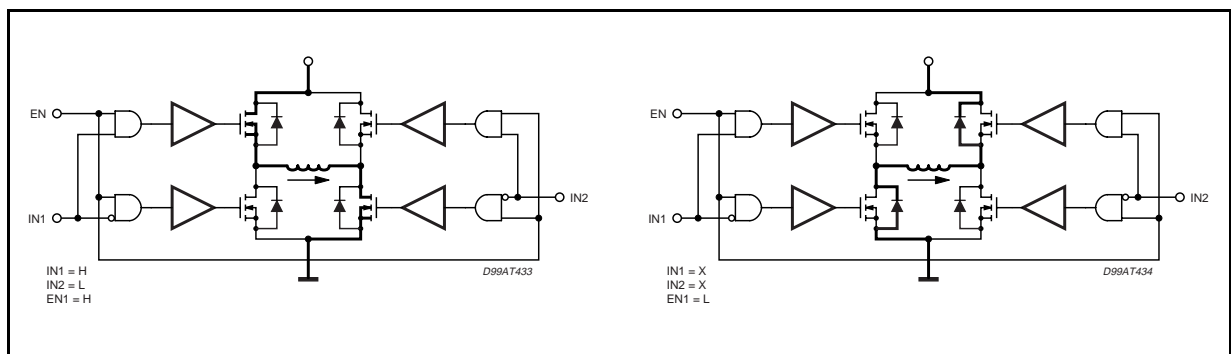


Figure 5c. Enable chopping



TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have an intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode applications. During recirculation with the ENABLE input is low, the POWER MOS is OFF and the diode voltage it is clamped to its characteristics. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans} = I_{DS}(t) \cdot V_{DS}(t)$$

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENALBE input high, the voltage drop across the transistor is $R_{DS(ON)}$ for voltages less than 0.6V and is clamped at a voltages depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction.

POWER DISSIPATION each bridge

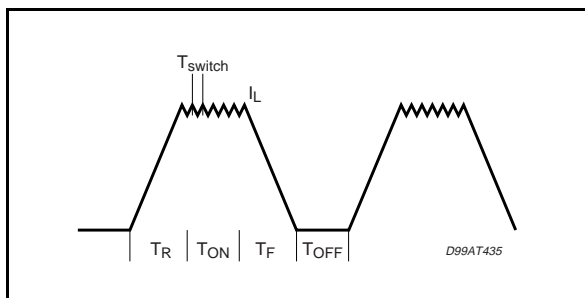
In order to achieve the high performance provided by the L9925 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in Fig. 6 is considered.

RISE TIME T_R

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_R . The dissipated energy $E_{OFF/ON}$.

$$E_{OFF/ON} = [R_{DS(ON)} \cdot I_L^2 \cdot T_R] \cdot \frac{2}{3}$$

Figure 6.



ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the

commutation E_{COM} . As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{CON} = V_S \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;

$T_{COM} = t_{rise} = t_{fall} \leq 20\mu s$

T_{SWITCH} = Chopper frequency

FALL TIME T_F

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{OFF/ON} = [R_{DS(ON)} \cdot I_L^2 \cdot T_F] \cdot \frac{2}{3}$$

QUIESCENT ENERGY

The last contribution of the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_S \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = (2 \cdot E_{OFF/ON} + E_{ON} + E_{COM})_{bridge1} + (2 \cdot E_{OFF/ON} + E_{ON} + E_{COM})_{bridge2} + E_{QUIESCENT}$$

The total power dissipation P_{DIS} is simply:

$$P_{DIS} = \frac{E_{tot}}{T}$$

T_R = Rise time

T_{ON} = ON time

T_F = Fall time

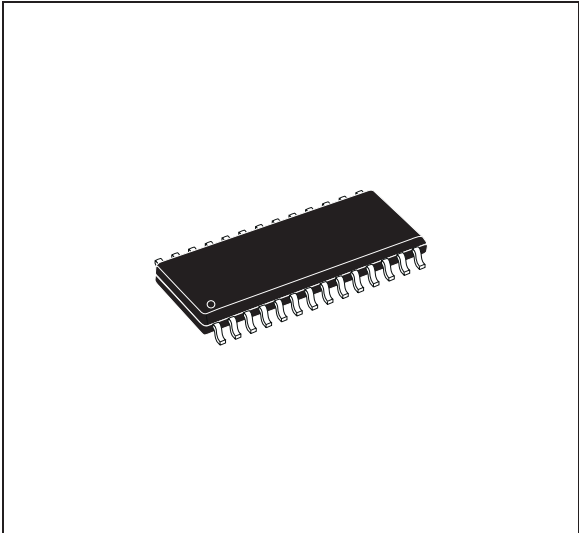
T_{OFF} = OFF time

T = Period

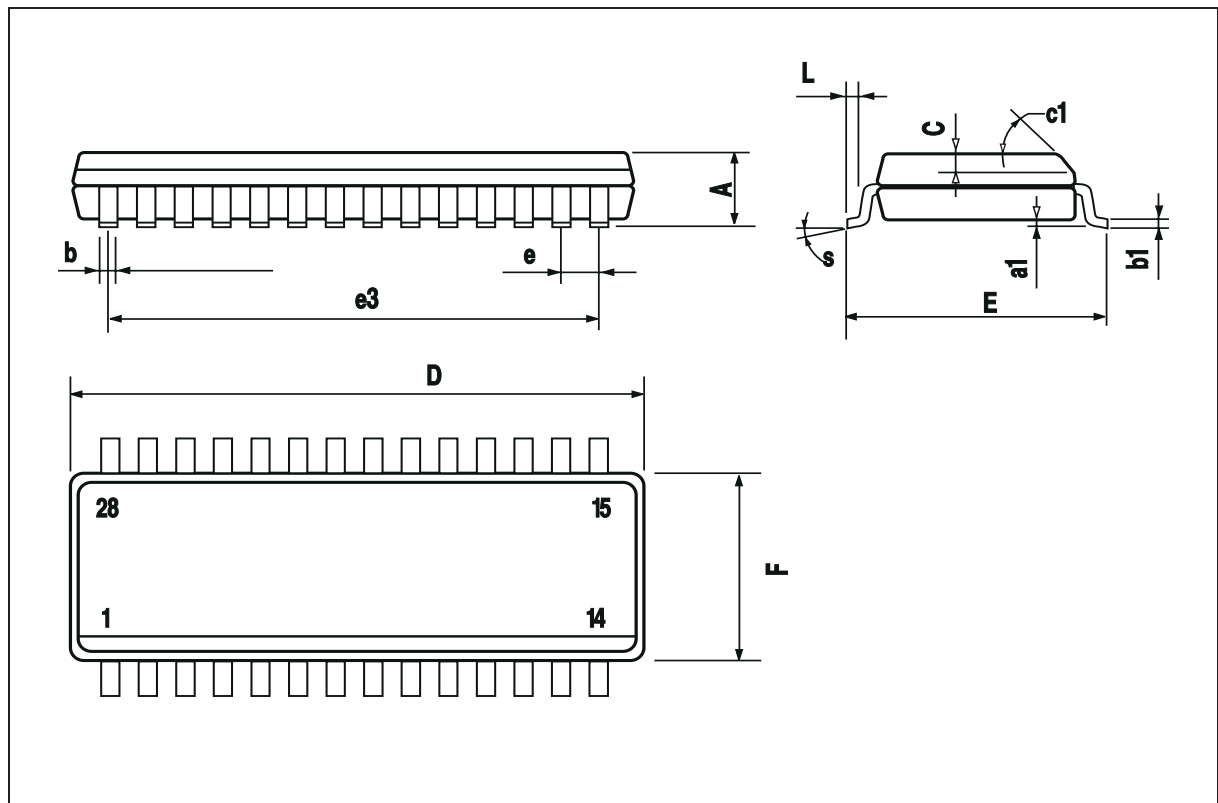
$$T = T_R + T_{ON} + T_F + T_{OFF}$$

| DIM. | mm | | | inch | | |
|------|------------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.3 | 0.004 | | 0.012 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.013 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 17.7 | | 18.1 | 0.697 | | 0.713 |
| E | 10 | | 10.65 | 0.394 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 16.51 | | | 0.65 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.299 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| S | 8° (max.) | | | | | |

OUTLINE AND MECHANICAL DATA



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