DESIGN OF A NEUTRAL POINT CLAMPED POWER INVERTER

by

DAVID BRENT CRITTENDEN, B.S.E.E.

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To properly recognize all of the people responsible for bringing me to this point in my life would take a considerable amount of space. Nevertheless, here is an attempt, mediocre at best, to recognize those individuals responsible for this thesis and master's degree.

Only by the grace of God have I come this far. God's never ending grace and mercy and his ultimate plan for my life have molded me for his desired purpose.

Gena, my wife, has endured long evenings alone, spoiled dinner plans, and a self-centered spouse. What a model of patience and compassion. I have been blessed.

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ABSTRACT

This thesis details the design, construction, and preliminary testing of a Neutral Point Clamped Power Inverter. The inverter is designed for the 100 kilowatt class of inverters and has a three phase output connection and a neutral connection.

The inverter is designed around insulated gate bipolar transistor as the power switching devices. The inverter employs software generation of the gate signals for the power switches and gate driver electronics to ensure reliability and insulation between the high power and low power circuitry.

The inverter produces a true three level line-to-neutral voltage waveform and a true five level line-to-line voltage waveform. The true descriptor indicates that a zero voltage output is not produced by averaging two potentials. Rather, a zero voltage output is produced by connecting the output voltage to a neutral point. To date, the inverter has been tested at 20 kilowatts of continuous power.

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CHAPTER I

INTRODUCTION

Today's electric power utilities employ many sources, distribution schemes, two major frequencies, and countless levels of power quality. An electrically-driven load intended for global use must be able to utilize the available power source regardless of the characteristics of that power source. This gives rise to the need for an interface between a load and the existing power supply or power grid. The universal power supply (UPS) is a solution to this need. The UPS must be tolerant of the characteristics mentioned above concerning electric power sources.

The scope of the project centers on the power supply requirements of a load where the power levels reach the megawatt level. Existing technology for meeting these requirements includes rotating machinery and commercial uninterruptible power supplies. Table 1.1 lists characteristics of some methods for achieving the goals of a UPS.

In general, a UPS will have an input conditioning stage and an output conditioning stage. This thesis considers the output stage of the UPS by investigating the neutral point clamped inverter (NPCI). The objective of the project which this thesis describes is to design, build, and test a scaled prototype of a megawatt level NPCI. The NPCI is a power electronics based

method for converting DC power into AC power. The implementation of this NPCI uses insulated-gate bipolar transistors (IGBTs) as the major power electronic devices, and it also utilizes medium power diodes. A major advantage of the NPCI is its multilevel switching capabilities. The specific NPCI modulation method employed leads to a five voltage level switching scheme in the line-to-line waveforms whereas conventional power electronic methods lead to three voltage levels of switching. The line-to-neutral waveforms have three voltage levels versus two levels in the conventional inverter. These increases in voltage levels reduce the harmonic content in the voltage waveforms.[1]

Table 1.1: Comparison of Universal Power Supply Methods

Legend: Key: ++ Best, + Good, 0 Average, - Poor, --Worst

Performance Item	TTU NPC_Converter	TTU Stair-Step Waveform Converter	Westinghouse DVR Utility Type Inverter	Rotating Machinery,	Commercial UPS, Libert, Toshiba
Size	++	0	--	-	-
Weight	++	0	--	--	-
Power Capability	+	++	++	+	--
Fault Tolerance	+	++	+	--	+
Input Harmonics	0	0	+	++	+
Ruggedness	0	0	0	++	++
Strengths	Compact, Powerful, Neutral Connection without transformer	Very powerful and robust. Can be modularized.	Commercial proven product, good control.	Robust, insensitive to short overload	Commercial proven product, good control.
Weakness	Input harmonics for small size and weight are high, remedies not mature yet.	Relatively heavy due to the need for transformers.	Very big and heavy. Size and weight of a Semi-Trailer.	120 lbs/kW, hard to adapt to different voltages and frequencies.	Heavy, 42 lbs/kW without batteries, and big, 0.62 kW/ft^3
Comments	11kW/ ft^3, 13lb/kW. Input Harmonics can be traded off with weight.	Input Harmonics can be traded off with weight.	PWM based Inverter with excellent control, extreme size and weight.	No harmonics and very rugged, but very heavy and needs gearing to change freq.	Not available for high power, high specific size and weight.

CHAPTER II

REVIEW OF CONVENTIONAL INVERTERS AND PULSE WIDTH MODULATION

Topology of Conventional Inverter

A conventional inverter utilizes six switches and six diodes. The switches can be any power electronic device suitable for operating in a completely on or completely off state on command. Figure 2.1 shows this

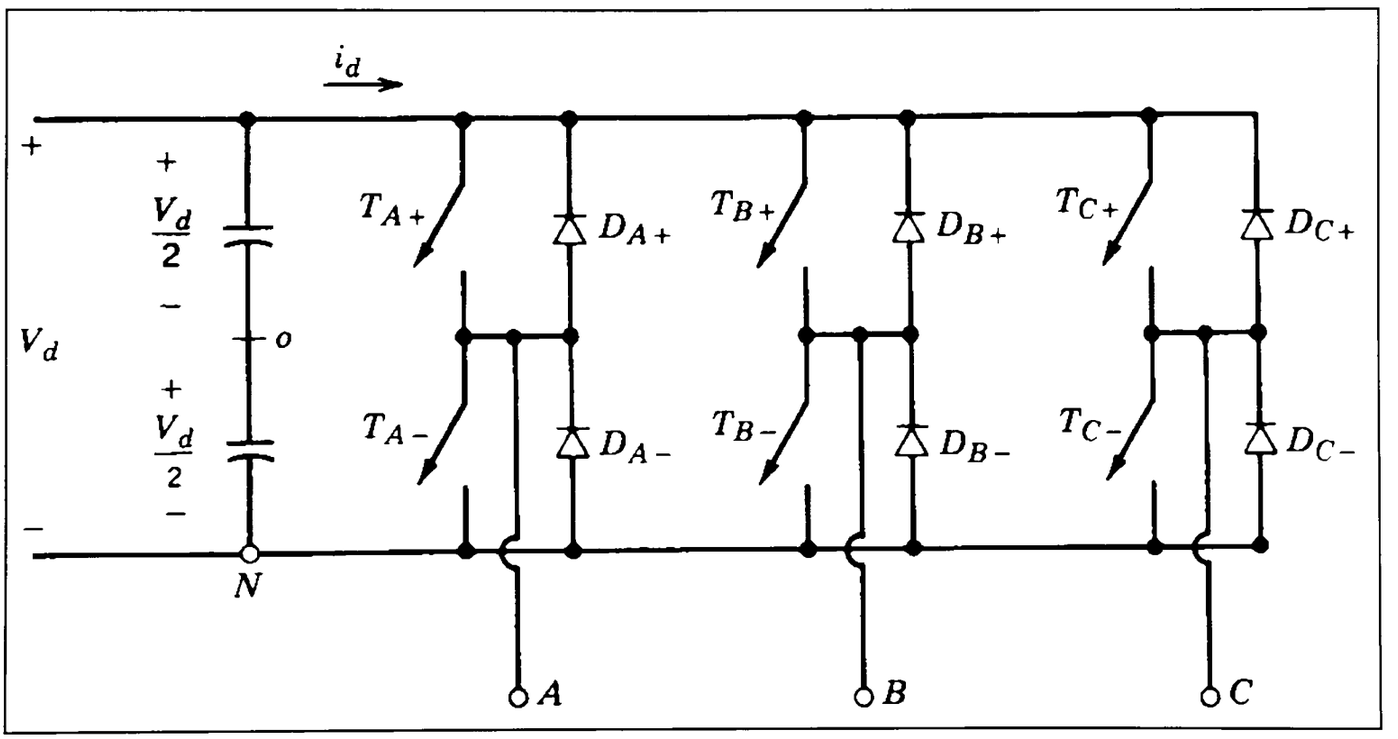


Figure 2.1: Conventional inverter topology.[2]

topology with phase outputs A, B, and C and a bus voltage of V_d. The phase voltages are defined with respect to the neutral point, *o*, and have a value of either V_d or 0. As shown, the phase outputs connect to the DC bus via ideal

switches. The ideal switches are used to facilitate the explanation of the topology and the generation of the control signals. The diodes across each switch are necessary when driving inductive loads. The diodes turn on when the potential across them is above a manufacturer specified level, generally a few volts for power diodes. The diodes carry regenerative currents at times when the current direction in an inductive load and the applied voltage have opposite polarity.

Generation of Pulse Width Modulation Signals

The topology above has a three phase output where the three phase voltages are 120° out of phase. Each phase requires a separate PWM signal, but the method for producing the PWM signal is the same. The difference in the PWM signals come from the control voltage signal, $v_{control}$. The $v_{control}$ signals have a frequency of f_1 and the same phase difference of 120° as the voltages of the phase outputs. The frequency, f_1, is the desired fundamental frequency of the inverter output voltage which will not look like the $v_{control}$ signal and will contain voltage components at harmonic frequencies of f_1. With the similarities between the phases, generation of the pulse width modulation signals is illustrated for only one phase.

A block diagram for the generation of PWM signals is shown in Figure 2.2. The $v_{control}$ input is the desired waveform characteristic to be seen

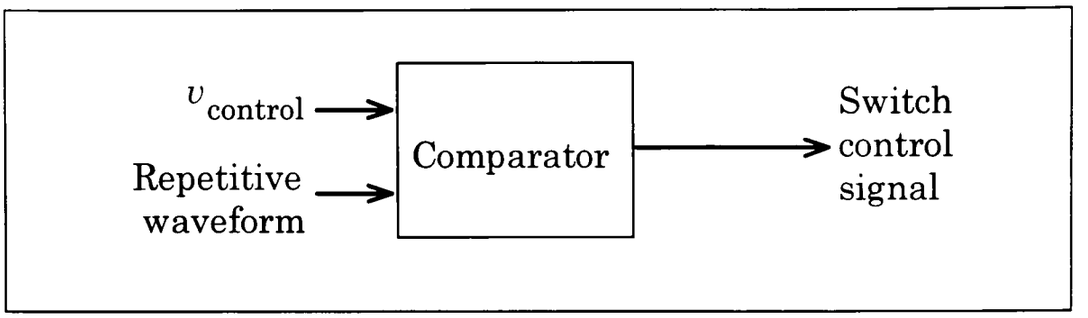


Figure 2.2: Block diagram of PWM signal generation

at the phase output. Usually, this is a sine wave of fixed or variable frequency with a normalized amplitude. The repetitive waveform input is a triangle wave (v_{tri}) with a frequency considerably higher than the frequency of the $v_{control}$ signal. Thus, the triangle wave becomes a carrier frequency for the $v_{control}$ signal. This relationship gives the modulation characteristic of the switch control signal. See Figure 2.3 (a) for an illustration where v_{tri} is the repetitive waveform signal with a frequency f_s.

The comparator operates on two conditions: $v_{control} < v_{tri}$ and $v_{control} > v_{tri}$. For $v_{control} < v_{tri}$, the output of the comparator is a logic high signal and the top switch (T_{A+}) is closed. For $v_{control} > v_{tri}$, the output of the comparator is a logic low signal and the bottom switch (T_{A-}) is closed. These conditions give the results shown in Figure 2.3 (b). Note, the comparator output is not shown in Figure 2.3 (b); Figure 2.3 (b) is the phase voltage. The values of the logic signal from the comparator are such that the devices being driven by the signals are in a completely on or completely off state. When in one of these states, the phase output voltage (v_{Ao} in Figure 2.3 (b)) has a value of

either the positive DC bus or the negative DC bus, resulting in the waveform shown in Figure 2.3 (b).

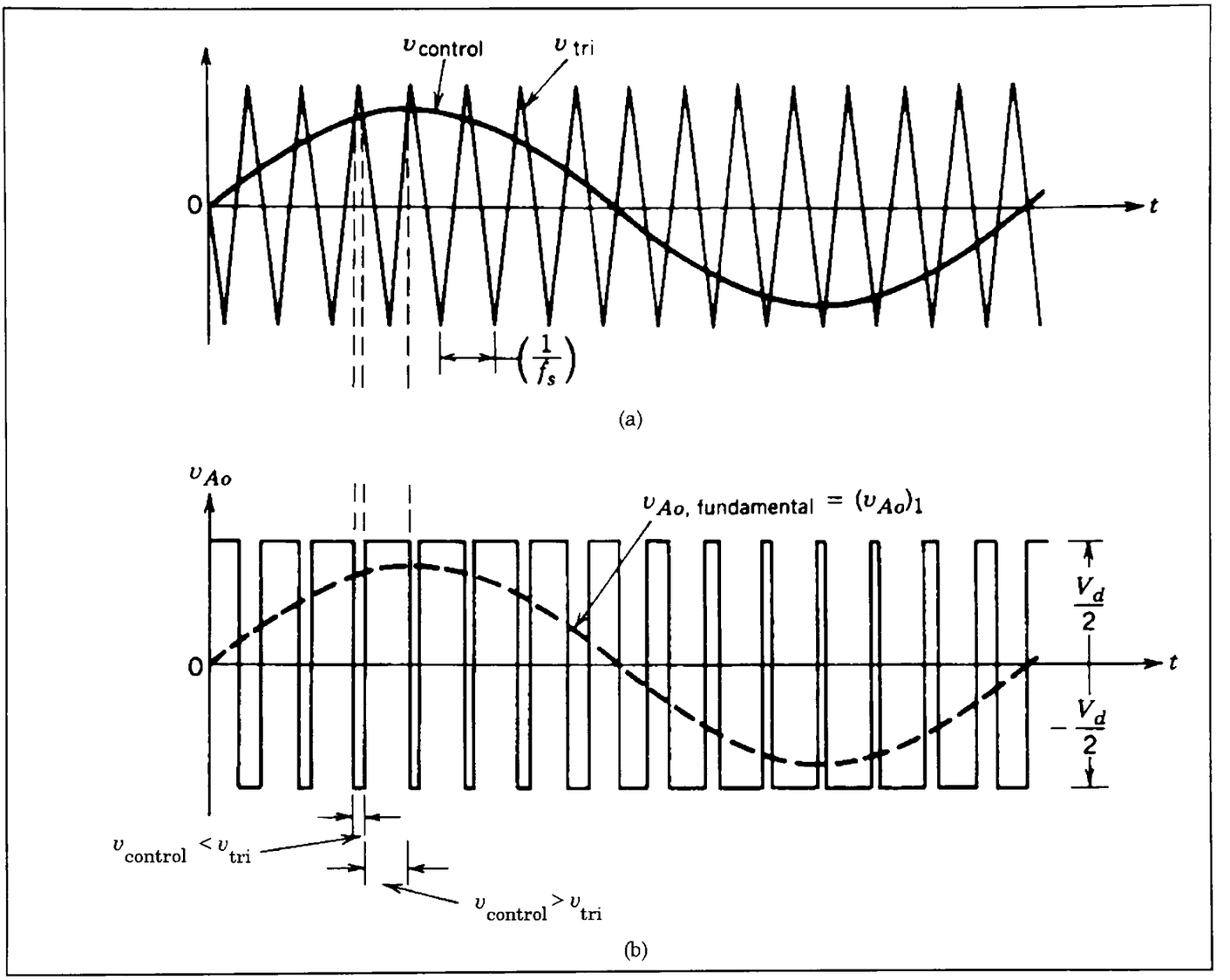


Figure2.3: Illustration of control signals: (a) $v_{control}$ and repetitive wave signals (b) resulting control signal (v_{Ao}) after comparator.[2]

A mathematical representation of the above explanation is as follows. Two additional terms need to be defined. The amplitude modulation ratio is given by

$$m_a = \frac{\hat{V}_{\text{control}}}{\hat{V}_{\text{tri}}} \tag{2.1}$$

where $\hat{V}_{\text{control}}$ is the peak amplitude of the control signal, v_{control}, and $\hat{V}_{\text{tri}}$ is the amplitude of the triangle wave, v_{tri}. The frequency modulation ratio is given by

$$m_f = \frac{f_s}{f_1}. \tag{2.2}$$

In the inverter in Figure 2.1, the switches T_{A+} and T_{A-} are controlled based on the comparison of v_{control} and v_{tri}. The output voltage for each phase is independent of the direction of the current through the switches, i_o, resulting in the relationships:

$$v_{\text{control}} > v_{\text{tri}}, \qquad T_{A+} \text{ is on}, \qquad v_{Ao} = \frac{V_d}{2}$$

$$\text{or} \tag{2.3}$$

$$v_{\text{control}} < v_{\text{tri}}, \qquad T_{A-} \text{ is on}, \qquad v_{Ao} = -\frac{V_d}{2}.$$

These relationships show that the switches are never on simultaneously and the resulting waveform varies between $V_d/2$ and $-V_d/2$ as shown in Figure 2.3 (b). The waveforms in Figure 2.3 (b) are shown for $m_f = 15$ and $m_a = 0.8$. Also shown in Figure 2.3 (b) is the fundamental frequency of the phase voltage v_{Ao} represented by the dashed line. Figure 2.4 shows the harmonics of f_1 from Figure 2.3 (b).

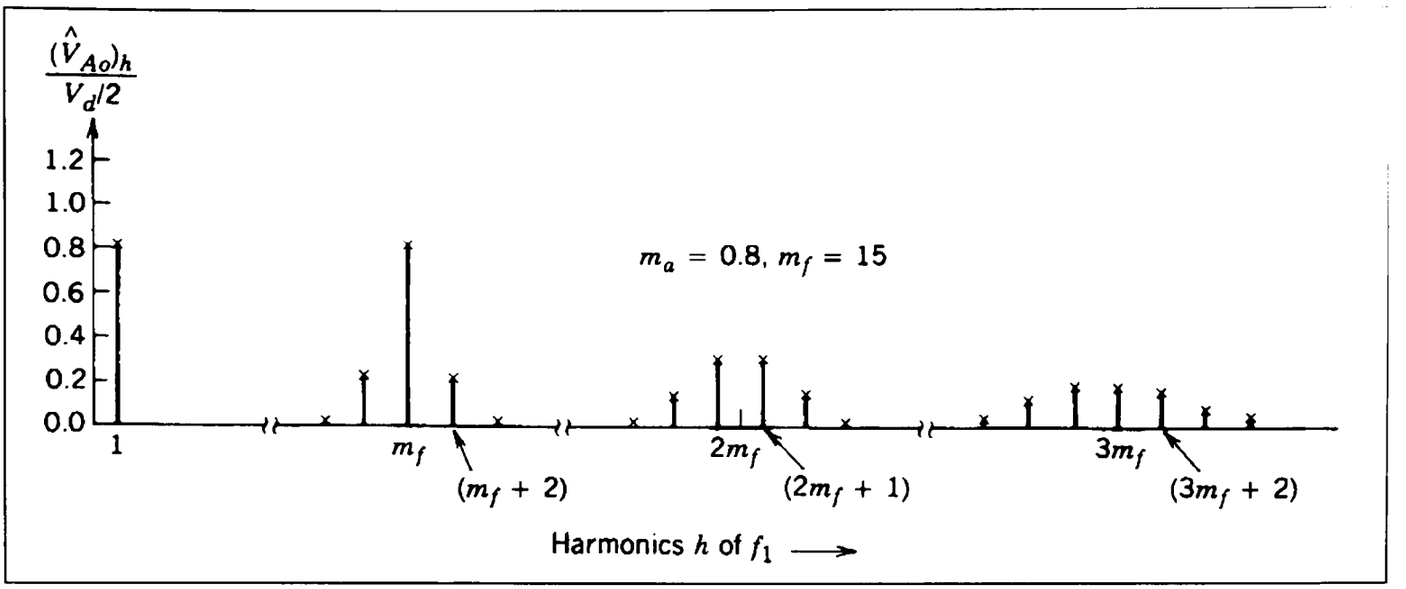


Figure 2.4: Harmonics of f_1 shown in Figure 2.3 (b). [2]

Figure 2.4 shows that the peak amplitude of the fundamental frequency component $(\hat{V}_{Ao})_1$ is m_a times $(V/2)$. If the control voltage varies sinusoidally with a desired output frequency, $f_1 = \omega_1/2\pi$, the control voltage can be represented as:

$$v_{\text{control}} = \hat{V}_{\text{control}} \sin(\omega_1 t) \qquad \text{where } \hat{V}_{\text{control}} \leq \hat{V}_{\text{tri}}. \tag{2.4}$$

The fundamental component of the output voltage then becomes

$$(v_{Ao})_1 = \frac{\hat{V}_{\text{control}}}{\hat{V}_{\text{tri}}} \sin(\omega_1 t) \frac{V_d}{2}$$

$$= m_a \sin(\omega_1 t) \frac{V_d}{2} \quad (\text{for } m_a \leq 1.0). \tag{2.5}$$

Grouping the m_a and the $V_d/2$ terms, the amplitude of the fundamental frequency is linearly dependent on the amplitude-modulation ratio, m_a.

A second observation is the amplitudes of the harmonics that surround the switching frequency. The switching frequency multiples are almost independent of m_f, but m_f defines where the harmonics will occur. In theory, the harmonics will occur by the following relation:

$$f_h = (jm_f \pm k) f_1$$

where h is the harmonic order corresponding to the kth sideband of the j times the frequency-modulation ratio m_f:

$$h = j(m_f) \pm k \tag{2.6}$$

Finally, m_f should be an odd integer. With m_f an odd integer, odd symmetry $[f(-t) = -f(t)]$ as well as half-wave symmetry $[f(t) = -f(t + T_s / 2)]$ with the time origin as shown in Figure 2.3 (b) can be achieved. Recognizing symmetry when finding the Fourier coefficients one finds that the sine series coefficients are finite and the cosine series coefficients are zero.

CHAPTER III

THE NEUTRAL POINT CLAMPED INVERTER

Topology

Figure 3.1 is an NPCI topology that allows for line-to-line waveforms with five voltage levels and line-to-neutral waveforms with three voltage

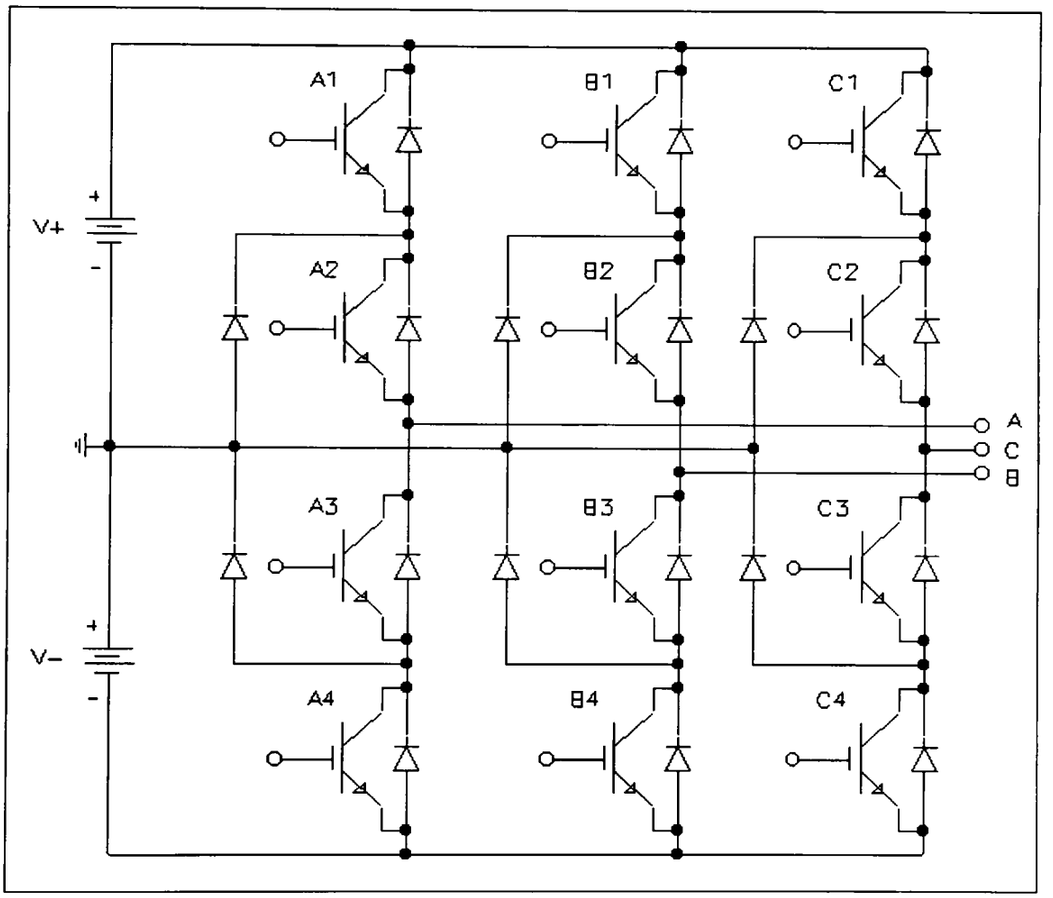


Figure 3.1: Neutral Point Clamped Inverter topology

levels. (See waveforms in later sections.) The phase outputs are the center point of a series connection of four IGBTs , and the DC bus input is connected to the top and bottom row of devices, A1, B1, C1, and A4, B4, C4, respectively. The center point of the DC bus is shown by a ground symbol

and is connected between a pair of series connected diodes in each phase. These six clamping diodes connected to the neutral bus control the voltage distribution among the four IGBTs in each phase leg. A conventional inverter requires the switches to sustain the full voltage drop between the positive and negative DC buses. However, the voltage drop (stress) across each switch of the NPCI is one half of the voltage between the positive and negative bus since the switches on either side of the neutral bus are in series, and an actual neutral point exists. Each IGBT has an individual gate signal that must be referenced between the respective IGBT gate and emitter terminal. The diode shown between the collector and emitter of each IGBT is an internal "body diode" inherent to the IGBT device structure.

The batteries in Figure 3.1 represent a DC bus structure. The DC bus has a positive, negative, and neutral connection with large low frequency filter capacitors and smaller high frequency filter capacitors. The bus structure is discussed in more detail in the physical system section.

Operation

This specific NPCI topology uses 3-level switching instead of 2-level switching used in conventional 3-phase inverters. The three levels correspond to the positive, negative, and neutral buses. Taking leg A of Figure 3.1 as an example, the phase output A is connected to the positive bus

by turning on switches A1 and A2. Turning switches A3 and A4 on connect the phase A output to the negative bus, and turning switches A2 and A3 on connects the phase A output to the neutral bus. The other two phases operate in the same manner, but with phase shifted results with respect to phase A.

The resulting waveforms for the switches in leg A are shown in Figure 3.2 where N covers one cycle of the desired output waveform.

Synopsis of Control Strategy

The control strategy for the NPCI is similar to a conventional converter in that a control voltage signal, a repetitive triangle wave signal, and a comparator function are used to produce the gate signals. The control voltage signal for each phase of the NPCI is the same signal used in the conventional converter, and likewise for the triangle wave. The function for the comparator, however, is the three level signum function as defined by:

$$Sgn(x) = \begin{cases} 1 & \text{if } x > 0 \\ 0 & \text{if } x = 0 \\ -1 & \text{if } x < 0 \end{cases} . \qquad 3.1$$

With four switches per phase, the NPCI gate signals are not as easily produced as the conventional inverter gate signals. The next chapter covers the control strategy in detail.

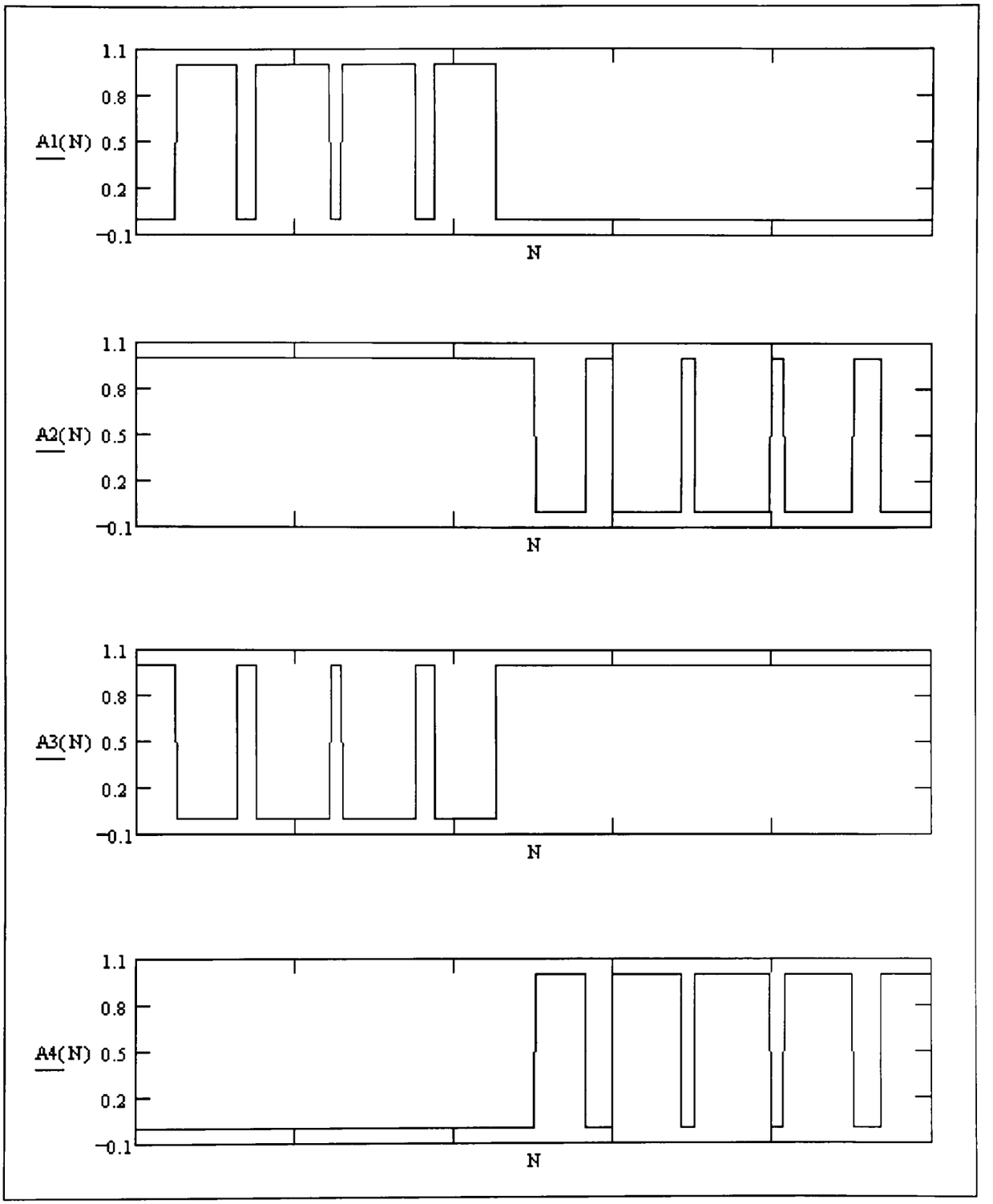


Figure 3.2: Example waveforms for leg A.

CHAPTER IV

NPCI CONTROL STRATEGY AND SIMULATION

The design process concerning the control strategy utilizes both Mathcad® and PSpice® software packages. The Mathcad software is used to generate the gate drive signal patterns that are later burned into EPROMs. The PSpice software allows simulation of the topology and control strategy and returns a good estimation of the behavior of the system.

Available Methods for Generation of Gate Drive Signals

The gate drive signal generation involves both hardware and software. The hardware based drive signals employ data storage devices (ROMs, EPROMS, etc.) or specific analog circuits. The data storage method requires that the drive signals be created and coded off-line for implementation on a specific storage device. Many interactive software programs are capable of generating the drive signals via digital waveform comparisons, and the data can be converted to the required device format. Implementing the data storage approach takes little time to construct and requires only basic external components and integrated circuits to store the data and to extract the data from the storage device. However, this method provides limited flexibility without reprogramming the storage device, and the frequency

response is limited to the frequency response of the storage device and associated circuitry.

The second hardware approach relies solely on electronic circuit design. The control circuit does exactly what the software program in the storage device method does, but in real time. Three major components of the gate drive circuit are the triangle wave generator, reference wave generator, and comparator ladder. This hardware approach is circuit design intensive and somewhat time consuming to construct. The complexity of the circuit is limited by the overall goals of the circuit and the availability of integrated analog circuits. The analog approach enjoys a larger degree of flexibility than the storage device method, and the frequency response is limited only by the delay time from input to output of the circuit (i.e., real time).

The software-based method utilizes microprocessor-generated signals. The microprocessor is programmed with a similar algorithm as used in the hardware method. The algorithm for the microprocessor can be very robust and complex, but, once it is loaded onto a device, reprogramming is required to change the algorithm. Usually, a microprocessor will require an output interface circuit(s) and possibly external program memory. The main advantage of the microprocessor approach is the robustness and flexibility that can be incorporated into the program. Typically, extremely fast microprocessors (digital signal processors [DSPs]) are required to execute the

programs. When a flexible and robust drive circuit is required, the cost of the DSP and related external hardware can be justified.

Control Strategy Used for NPCI

For the period of time that this report covers, the hardware implementation using a data storage device was the best choice. The time constraints were such that a working prototype was needed quickly, and the data storage implementation is the best method for the given constraints. Figure 4.1 is a repeat of Figure 3.1 for reference.

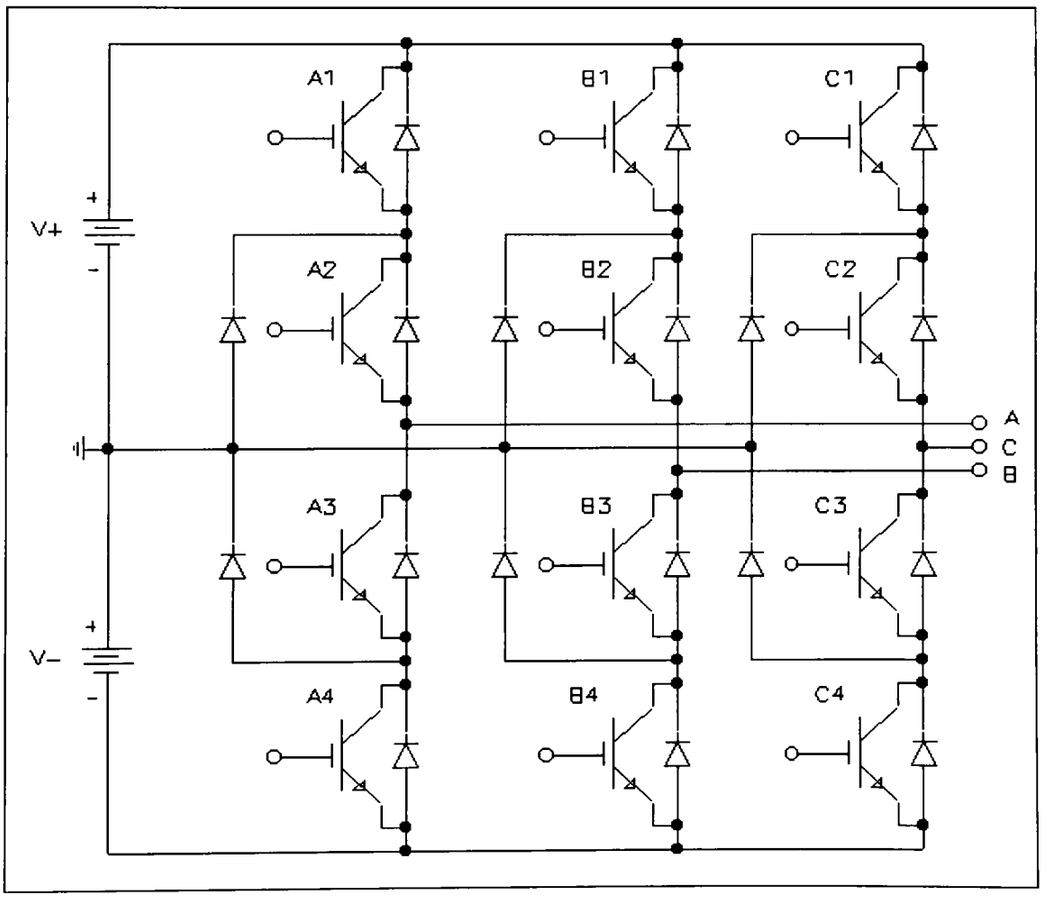


Figure 4.1: Neutral Point Clamped Inverter topology

As in the case of the conventional inverter, each leg (or phase) of the inverter (a vertical, four switch group) has identical gate drive signals except for a 120° phase shift between each leg. Therefore, a description of one leg can be extended to the other two legs keeping in mind the phase shift between legs.

Figure 4.2 shows the classic method for generating pulse-width modulation (PWM) signals as in the case of the conventional inverter of Chapter II. For Figure 4.2, the waveforms have been digitally generated

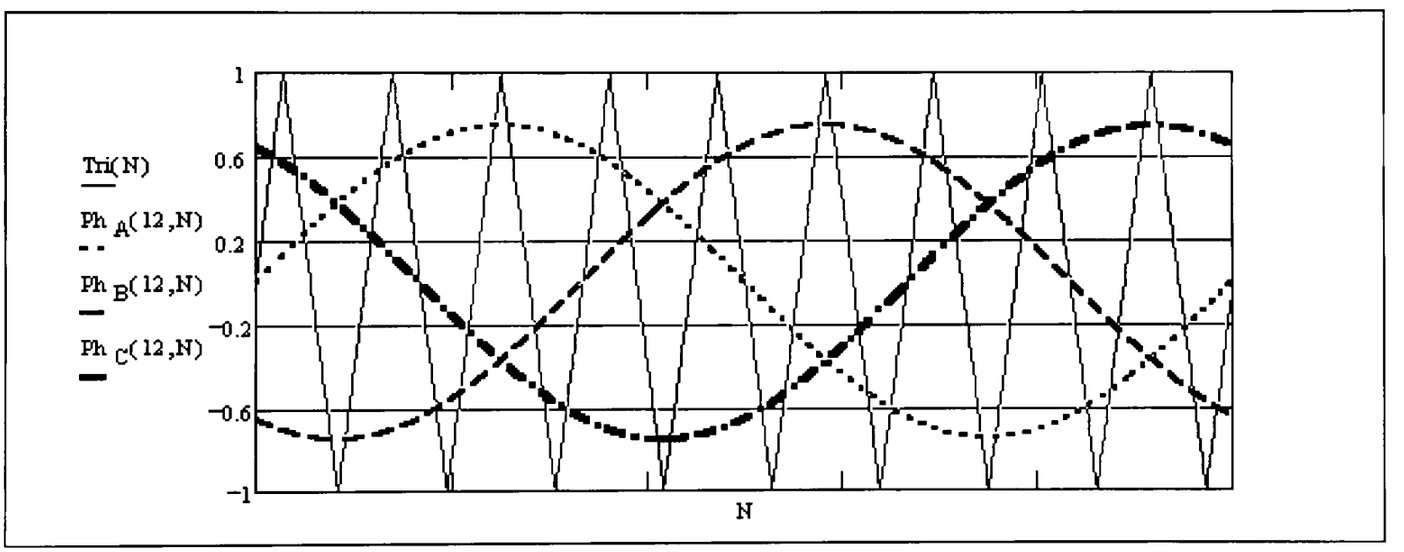


Figure 4.2: Reference waves and triangle wave for PWM signal generation with a frequency modulation ratio of 9.

using Mathcad. The index N is the "time step" used as the argument for the three control voltages (Ph_A, Ph_B, Ph_C) and the triangle reference wave (Tri). The N index sets the resolution for the waveforms and therefore the sensitivity of the output. The other index in the control voltages is the

amplitude-modulation ratio index. The amplitude-modulation ratio index is a pointer to a particular amplitude-modulation ratio. Its use will be better understood later as the Mathcad algorithm is explained. The frequency modulation ratio for Figure 4.2 is not a practical value. However, a low frequency modulation ratio allows for a good illustration. The following figures will explain the derivation of the individual control signals for all the IGBTs.

To accomplish the three level line-to-neutral voltage waveforms, a switching function with three discrete levels is needed for each phase. A switching function shows what the output of the phase will be for the given timestep. Using the control voltage for each phase, the triangle reference wave, and the signum function as defined earlier, a switching function for each phase is given as follows:

$$Sw_A(i,N) = \begin{cases} Sgn(Ph_A(i,N)) & \text{if } \left|Ph_A(i,N)\right| > Tri(N) \\ 0 & \text{otherwise} \end{cases} \tag{4.1}$$

$$Sw_B(i,N) = \begin{cases} Sgn(Ph_B(i,N)) & \text{if } \left|Ph_B(i,N)\right| > Tri(N) \\ 0 & \text{otherwise} \end{cases} \tag{4.2}$$

$$Sw_C(i,N) = \begin{cases} Sgn(Ph_C(i,N)) & \text{if } \left|Ph_C(i,N)\right| > Tri(N) \\ 0 & \text{otherwise} \end{cases} . \tag{4.3}$$

Recalling that the signum function has three discrete values for a given input, the switching function will indeed have three values: -1, 0, or 1. Figure 4.3 shows the switching functions for the waveforms in Figure 4.2.

From the switching functions, it is possible to obtain the individual gate control signals. Again, each phase uses the same method for obtaining the signals, but with the respective switching function. For phase A, the switch A1 is on when the switching function is greater than 0. This connects the phase A output voltage to the positive bus. The switch A2 is conducting when the switching function is greater than -1. Switch A2 must conduct when ever the phase A output must be zero or the positive bus voltage. Similarly, switch A3 is turned on when the switching function is less than 1, i.e. when the phase A output voltage must be zero or the negative bus voltage. Finally, the switch A4 conducts when the phase A output voltage must be connected to the negative bus voltage. Mathematically, these relations appear as follows.

$$\text{Gate signal of A1} = \begin{cases} \text{on} & \text{if } Sw_A(i,N) > 0 \\ \text{off} & \text{otherwise} \end{cases} \tag{4.4}$$

$$\text{Gate signal of A2} = \begin{cases} \text{on} & \text{if } Sw_A(i,N) > -1 \\ \text{off} & \text{otherwise} \end{cases} \tag{4.5}$$

$$\text{Gate signal of A3} = \begin{cases} \text{on} & \text{if } Sw_A(i,N) < 1 \\ \text{off} & \text{otherwise} \end{cases} \tag{4.6}$$

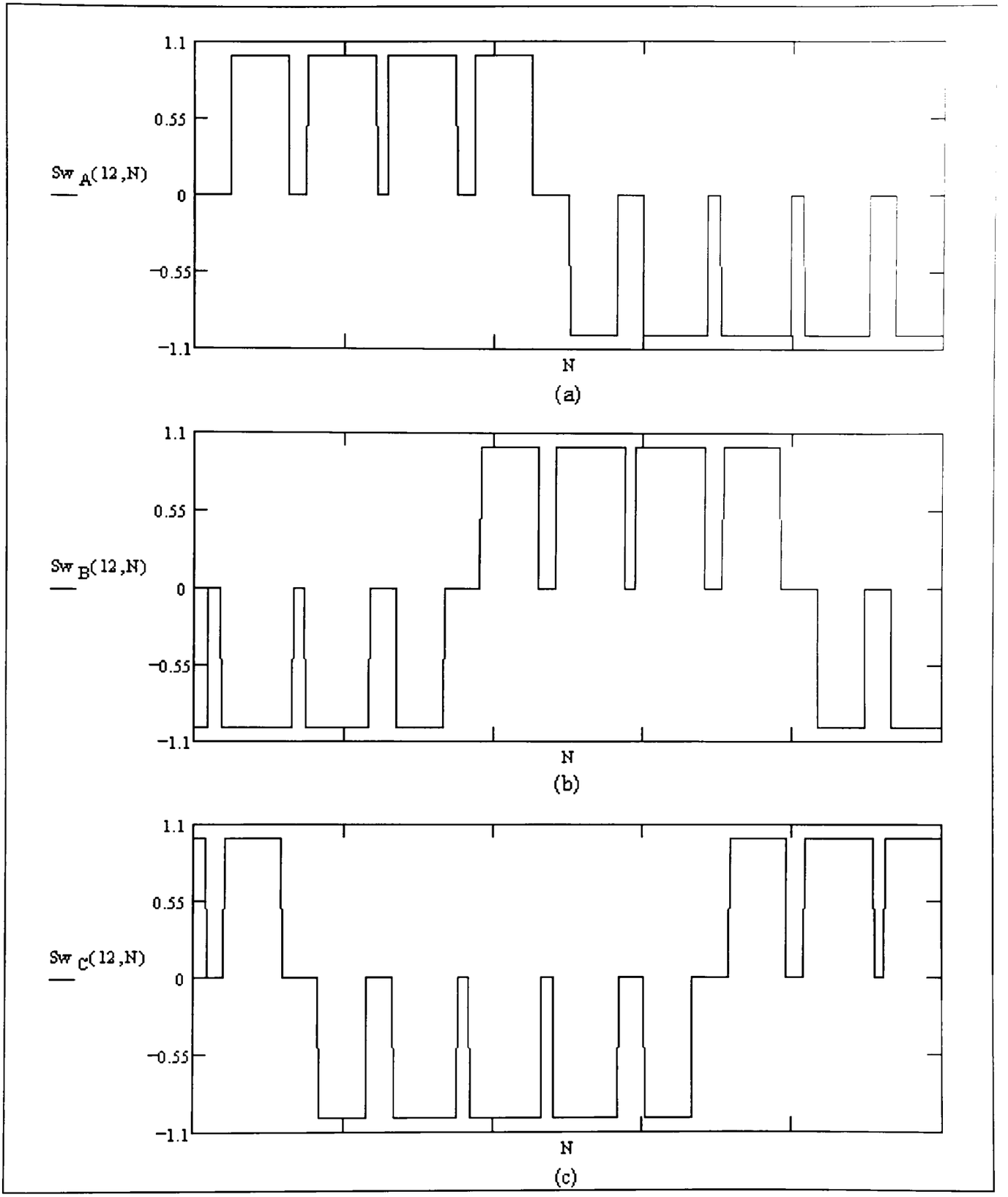


Figure 4.3: Switch functions for Figure 4.2

$$\text{Gate signal of A4} = \begin{cases} \text{on} & \text{if } Sw_A(i,N) < 0 \\ \text{off} & \text{otherwise} \end{cases} \tag{4.7}$$

Graphically, the gate signals for Figure 4.2 are shown in Figure 4.4. This figure is the same as shown in Chapter III concerning the gate signals. For

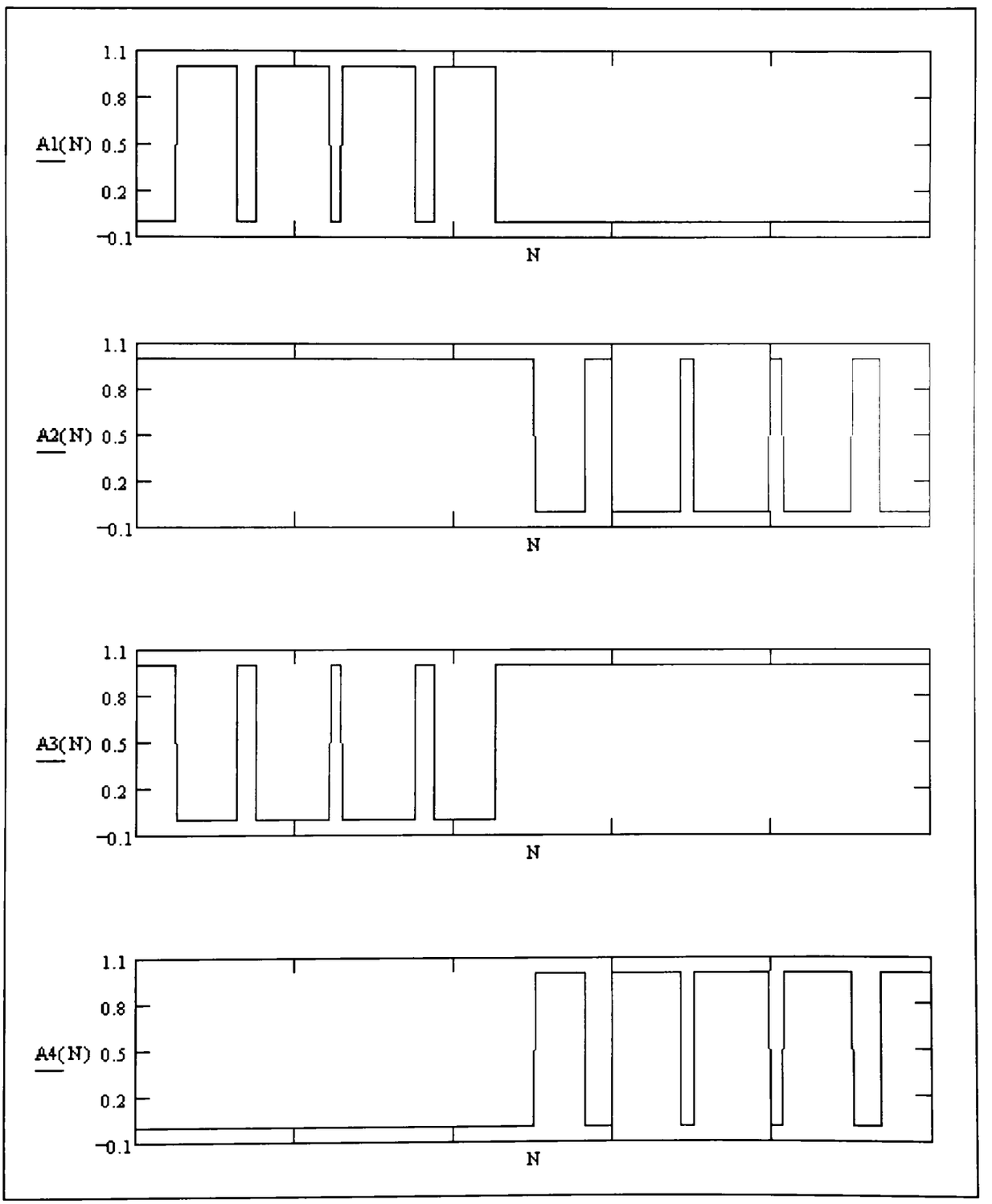


Figure 4.4: Gate signals for Figure 4.2.

the other two phases, the same approach is used, but with the corresponding switching function with respect to the phase.

Code Generation with Mathcad

As mentioned above, the figures shown previously concerning the switching functions and the gate signals were used to illustrate the method for obtaining the desired gate signals. Below, the equations and resulting waveforms used for developing the actual NPCI code are given. The Appendix contains the entire Mathcad document used for code development.

The document begins with a definitions of necessary functions and constants (see Figure 4.5). The number of modulation ratios (I_o) dictates how many different sets of data will be calculated. The amplitude ratios themselves are calculated and stored in the array k_{A_i}. The frequency modulation ratio, m_f, is defined to be 57. With a frequency modulation ratio of m_f, the switching frequency of the IGBTs is given by

$$\text{device switching frequency} = k_f \cdot (\text{desired output frequency}). \qquad (4.8)$$

Since the waveforms used for generation of the gate signals are digital in nature, the resolution or time step for the waveforms is N_o. The value assigned to N_o is dictated by the storage device used to hold the gate signal data. The EPROM used for the NPCI is a 16,384 (16k) word device with each word having 8 bits. With N_o equal to 1024 and assuming each control word

requires 8 bits, the size of the data set in kilobits is $(I_o \cdot N_o \cdot 8/1024)$, or 128. The total number of bits in the EPROM is given by multiplying the number of words in the device times the number of bits per word giving 128 kbits for a 16k EPROM. The choice of N_o now becomes obvious in light of the available space and the number of amplitude modulation ratios. Multiple EPROMs could be used if the number of modulation ratios and the resolution needed to be increased. A resolution of 1024 samples per period gives adequate representation of the desired signals for the parameters given. The resolution of the data could be increased while using only one EPROM by reducing the number of amplitude modulation ratios (I_o).

Definition of Signum Function:	$Sgn(x) := \begin{cases} 1 & \text{if } x>0 \\ -1 & \text{if } x<0 \\ 0 & \text{otherwise} \end{cases}$	
Number of Modulation Ratios:	$I_o \equiv 16$	
Amplitude Modulation Ratios:	$m_{A_i} = \frac{i}{I_o}$	
Frequency Modulation Ratio:	$m_f \equiv 57$	Device switching frequency: $m_f 60 \cdot Hz = 3420 \cdot Hz$
Number of Points in Period:	$N_o \equiv 1024$	
EPROM Size in kbits:	$I_o \cdot N_o \cdot 8 \cdot 1024^{-1} = 128$	

Figure 4.5: Portion of Mathcad document, part 1.

The next portion of the Mathcad document provides the definition of the triangle function, the control voltages (reference sinusoids), and the

switching function for each phase (see Figure 4.6). The triangle function (Tri(N)) takes advantage of the Mathcad's definition of the arcsin function. The range of the arcsin result is defined from $-\frac{\pi}{2}$ to $+\frac{\pi}{2}$. Since the sine function varies from -1 to 1, and including the $\frac{2}{\pi}$ factor, the triangle function has a range from -1 to1. Notice the frequency modulation factor (m_f) in the argument of the sine function. As m_f increases, so does the frequency of the triangle wave. As the name implies, the modulation ratio varies the degree to which the control signals are modulated, and thus the triangle function is the means by which the modulation is controlled.

The control voltage signals, Ph_A, Ph_B, Ph_C, are easily understood from their definitions in Figure 4.6. The (i/I_o) term in front of the control voltage equations is simply the amplitude modulation ratio, or the amplitude of the sinusoid. At this point in the Mathcad document, the index i is only an argument in a function definition, and it need not be defined. Later, the index is defined from 1 to I_o. The switching functions in Figure 4.6 have the same definitions as above but with the Mathcad notation. The notation is as follows:

if(*conditional statement, result if true, result if false*).

Triangle function:

$$Tri(N) := \frac{2}{\pi} \cdot \operatorname{asin}\left(\sin\left(m_f \frac{N}{N_o} \cdot 2 \cdot \pi\right)\right)$$

Reference Sinusoid for Phase a:

$$Ph_A(i,N) := \frac{i}{I_o} \cdot \sin\left(\frac{N}{N_o} \cdot 2 \cdot \pi\right)$$

Reference Sinusoid for Phase b:

$$Ph_B(i,N) := \frac{i}{I_o} \cdot \sin\left(\frac{N}{N_o} \cdot 2 \cdot \pi - 120 \cdot deg\right)$$

Reference Sinusoid for Phase c:

$$Ph_C(i,N) := \frac{i}{I_o} \cdot \sin\left(\frac{N}{N_o} \cdot 2 \cdot \pi + 120 \cdot deg\right)$$

NPC Switching Function, Phase A:

$$Sw_A(i,N) := if\left(\left|Ph_A(i,N)\right| > Tri(N), Sgn\left(Ph_A(i,N)\right), 0\right)$$

NPC Switching Function, Phase B:

$$Sw_B(i,N) := if\left(\left|Ph_B(i,N)\right| > Tri(N), Sgn\left(Ph_B(i,N)\right), 0\right)$$

NPC Switching Function, Phase C:

$$Sw_C(i,N) := if\left(\left|Ph_C(i,N)\right| > Tri(N), Sgn\left(Ph_C(i,N)\right), 0\right)$$

*** BIT#7 is upper IGBT Phase A ****
*** BIT#6 is upper IGBT Phase B ****
*** BIT#5 is upper IGBT Phase C ****
*** BIT#4 is lower IGBT Phase A ****
*** BIT#3 is lower IGBT Phase B ****
*** BIT#2 is lower IGBT Phase C ****
*** BIT#1 & BIT#0 (LSB) not used****

Index h(igh) means on the +/- bus.

Index l(ow) means on the ground bus.

Index u(p) means above ground bus.

Index d(own) means below ground bus.

$$Bit_{Auh}(i,N) := if\left(Sw_A(i,N) > 0, 2^7, 0\right)$$

$$Bit_{Aul}(i,N) := if\left(Sw_A(i,N) > -1, 2^7, 0\right)$$

$$Bit_{Adl}(i,N) := if\left(Sw_A(i,N) < 1, 2^4, 0\right)$$

$$Bit_{Adh}(i,N) := if\left(Sw_A(i,N) < 0, 2^4, 0\right)$$

$$Bit_{Buh}(i,N) := if\left(Sw_B(i,N) > 0, 2^6, 0\right)$$

$$Bit_{Bul}(i,N) := if\left(Sw_B(i,N) > -1, 2^6, 0\right)$$

$$Bit_{Bdl}(i,N) := if\left(Sw_B(i,N) < 1, 2^3, 0\right)$$

$$Bit_{Bdh}(i,N) := if\left(Sw_B(i,N) < 0, 2^3, 0\right)$$

$$Bit_{Cuh}(i,N) := if\left(Sw_C(i,N) > 0, 2^5, 0\right)$$

$$Bit_{Cul}(i,N) := if\left(Sw_C(i,N) > -1, 2^5, 0\right)$$

$$Bit_{Cdl}(i,N) := if\left(Sw_C(i,N) < 1, 2^2, 0\right)$$

$$Bit_{Cdh}(i,N) := if\left(Sw_C(i,N) < 0, 2^2, 0\right)$$

$$Byte_u(i,N) := Bit_{Auh}(i,N) + Bit_{Adl}(i,N) + Bit_{Buh}(i,N) + Bit_{Bdl}(i,N) + Bit_{Cuh}(i,N) + Bit_{Cdl}(i,N)$$

$$Byte_d(i,N) := Bit_{Aul}(i,N) + Bit_{Adh}(i,N) + Bit_{Bul}(i,N) + Bit_{Bdh}(i,N) + Bit_{Cul}(i,N) + Bit_{Cdh}(i,N)$$

$$N := 0 .. \left(N_o - 1\right)$$

Figure 4.6: Portion of Mathcad document, part 2.

The individual gate signals are given by the $Bit_{(\cdot)}(\cdot)$ functions with subscript notation given on the left edge of the Mathcad document. The gate signals have the same conditional statement definitions as given previously but again with a different notation. However, the *result if true* portion of the Mathcad notation is different from that previously shown. The "result if the conditional statement is true" is based upon the location of the data within the storage device (i.e., EPROM). For the device A1 in Figure 4.1, the control bit (Bit_{Auh}) will be located in the eighth position of a control word, where a control word is comprised of eight control bits numbered 0 to 7. The 2^7 value is the decimal representation of a 1 in the eighth position of an eight bit word. For the device A3 in Figure 4.1, the control bit (Bit_{Adl}) will be located in the fourth position of a control word. The 2^4 value is the decimal representation of a 1 in the fourth position of an eight bit word. The remainder of the control bits and words follow the same pattern. Each word holds a single value for each device. The next word holds the next value "in time" for each device, and so on until all N_0 points have been completed.

Now, notice that the result for which the conditional statement is true for the control bits Bit_{Auh} and Bit_{Aul} is the same. This would imply that two control bits occupy one bit location. This is not possible without using multiple storage devices. Using multiple devices provides enough bit locations for each gate signal. Dividing the twelve signals evenly between

the two devices leaves two bits on each storage device empty as noted on the Mathcad document. Further understanding concerning the two storage devices will come when the driver boards are explained in the following chapter.

To combine the individual gate control bits into the respective control words, the Byte functions are needed. The $Byte_u$ function combines control bits for the first and third rows of IGBTs in Figure 4.1. Likewise, the $Byte_d$ combines the control bits for the second and fourth rows of IGBTs. This combination avoids the conflict mentioned concerning bit locations. The Byte functions accomplish a bit addition of the control bits to form control words where again each control word represents one time step of 1024 steps per cycle.

The remainder of the Mathcad document places the data from the Byte functions in the proper order for loading onto the storage device (see Appendix.) Bytes_13 and Bytes_24 are the two gate signal data sets in the form of two dimensional arrays. The WRITEPRN(*filename*) function is the Mathcad command for creating the ASCII file *filename*.prn. The data in the Bytes_13 and Bytes_24 arrays are stored in the files NPC_13.prn and NPC_24.prn, respectively. A BASIC program is used to convert the ASCII files to the proper storage device hexadecimal format. This hexadecimal format can then be loaded onto the EPROMs.

The data are arranged so that an orderly addressing structure can be used to change from one modulation ratio to another. As mentioned previously, the number of gate signal control words per period of the control voltage is 1024. This amount of data requires 10 address lines (2^{10}=1024). Four additional address lines above the original ten access a particular modulation ratio (2^4=16). The schematic of the low power circuitry in the next chapter shows how the EPROM address structure is implemented.

Simulation

The goal in simulating the NPCI was to investigate the topology with approximate devices (i.e., simple device models) while demonstrating the generation of the gate signals. The simulation of the NPCI was performed using PSpice for Windows. Since the number of component connections in the schematic of the NPCI exceeds the PSpice student version limit, the professional version of PSpice is required. The NPCI schematic has multiple layers for the various components. The top layer of the schematic is shown in Figure 4.8. This figure resembles previous figures regarding the layout of the switches and diodes. The IGBTs, diodes, and the NPC_Load component all have two layers. The IGBT and diode symbols represent a simple model of the behavior of the respective device. The NPC_Load symbol contains an

appropriate model, also. The NPC_PWM component has three layers. The second layer contains three instances of the symbol for the third layer.

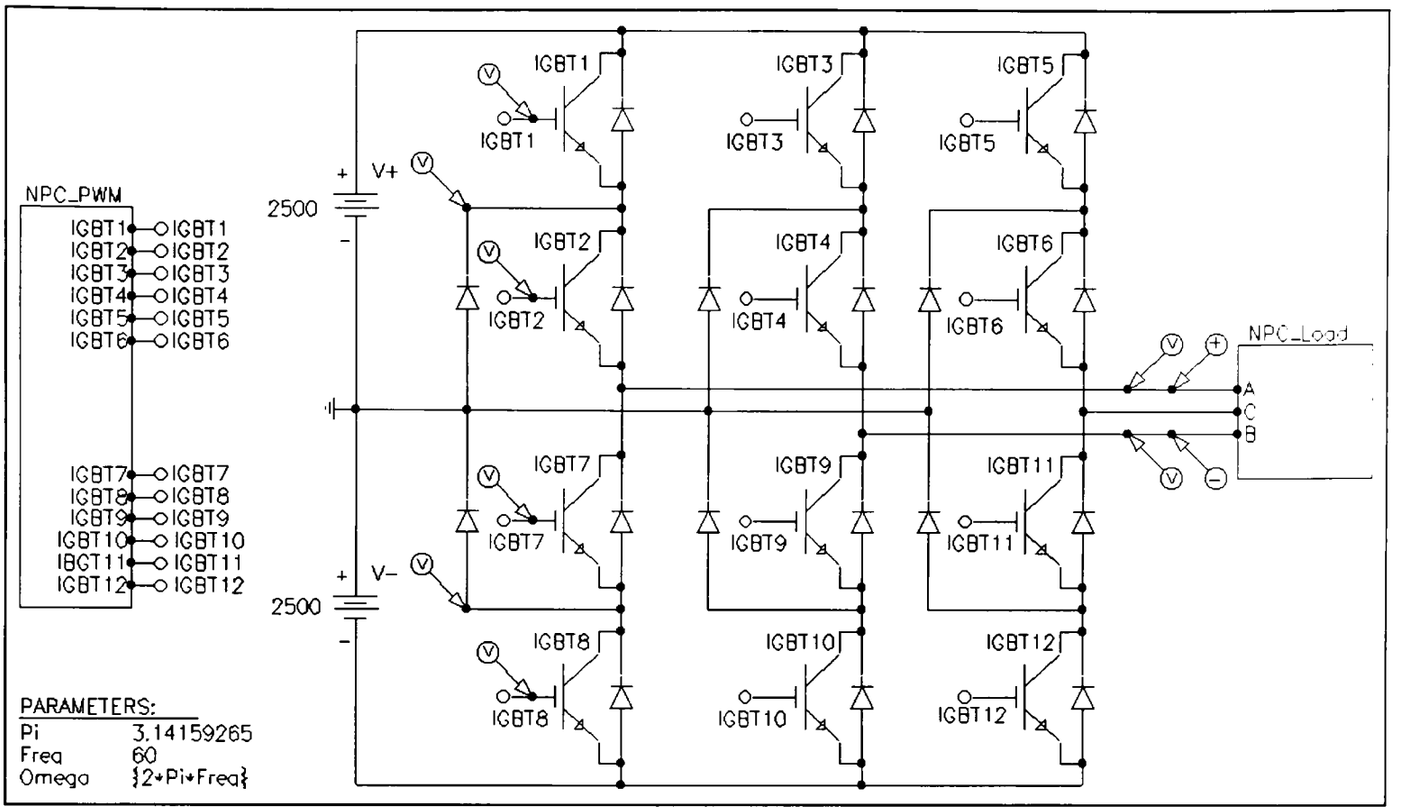


Figure 4.7: NPCI schematic from PSpice.

The IGBT second layer is shown in Figure 4.9 (a). The terminals of the IGBT are connected to a voltage controlled switch. The switch is a PSpice tool for developing models of devices and systems. This switch model has the following characteristics:

Turn off voltage (switch opens):	V_{off} = 0.0 V
Resistance when switch is open:	R_{off} = 100 kΩ
Turn on voltage (switch closes):	V_{on} = 1.0 V
Resistance when switch is closed:	R_{on} = 100 mΩ

So, when the base of any of the IGBTs in Figure 4.8 has a voltage of 1.0 V or greater, the switch closes and current flows through the model. The diodes in

Figure 4.8 utilize the same switch block along with another analog behavioral modeling block (ABM) used for comparing two signals. Figure 4.8 (b) shows the model for the diode. The second ABM block performs the equation given below it:

IF(V(%IN1) > V(%IN2), 1, 0).

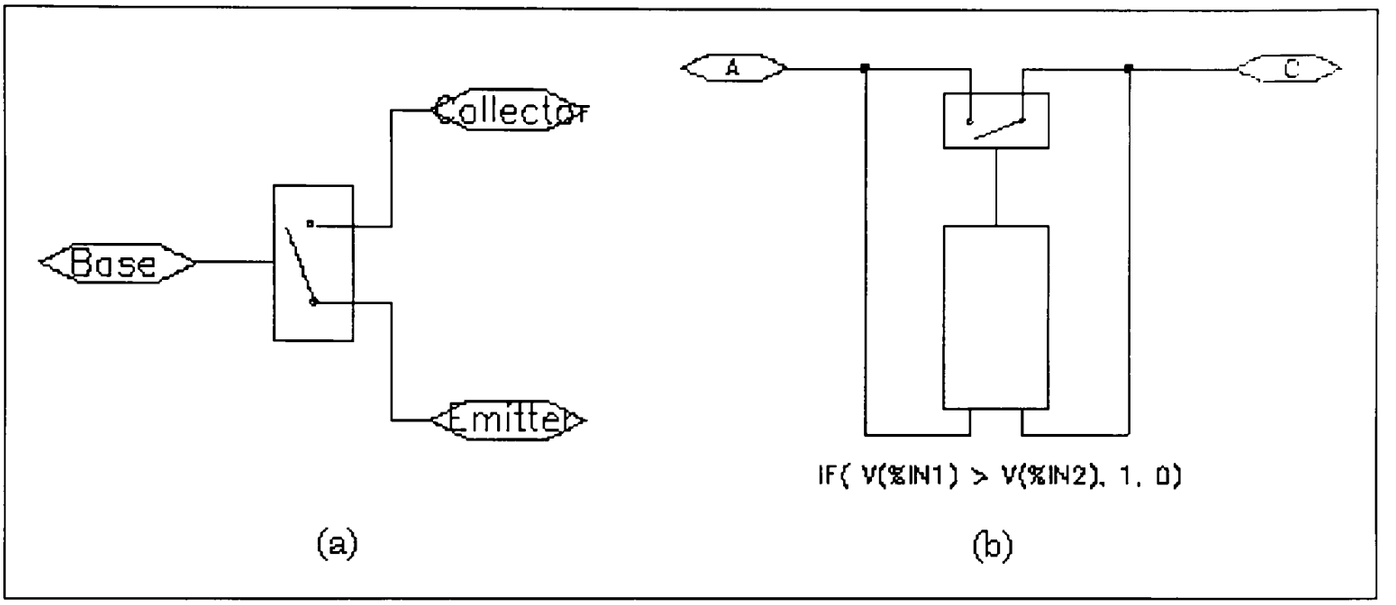


Figure 4.8: PSpice models: (a) IGBT model and (b) diode model.

The PSpice representation of the above equation is understood from the following table:

Table 4.1: Truth table for ABM block in Figure 4.9 (b)

IF	OUTPUT
$V_1 > V_2$ is true	1
$V_1 > V_2$ is false	0

With the anode as the V_1 input and the cathode as the V_2, the model operates like a diode based on the V_1-V_2 relationship.

The second layer of the NPC_Load block in Figure 4.8 shows a simple inductive load model. The load model is shown in Figure 4.10. The parameters section in the left hand corner of Figure 4.10 defines the value of the inductance of the load based upon the Omega parameter. The Omega parameter in Figure 4.10 is defined in the top layer of the NPCI schematic.

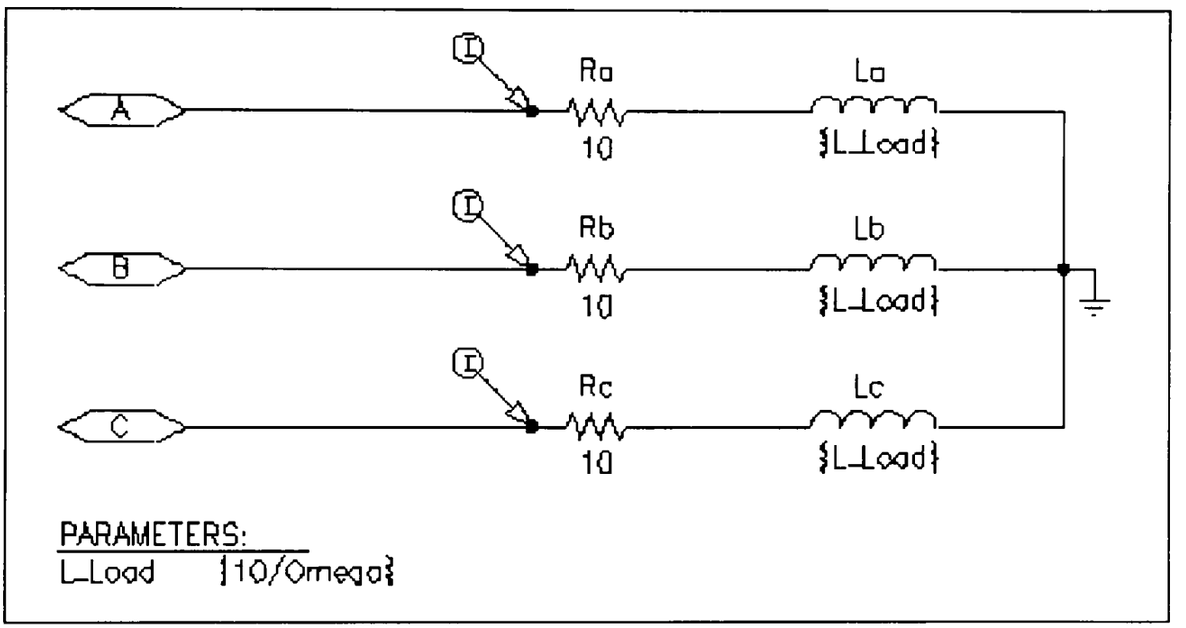


Figure 4.9: Model of NPCI load.

The last model to explain is the NPC_PWM block. The second layer of the NPC_PWM is shown in Figure 4.11 and the third layer is shown in Figure 4.12. The second layer has three instances, one for each of the phases, of an ABM block and PWM_x block. The ABM block implements the three level signum function. The sinusoidal voltage sources represent the control signals that are 120° out of phase with each other as discussed in previous

chapters. The V_triangle voltage source represents the triangle wave need for PWM signal generation.

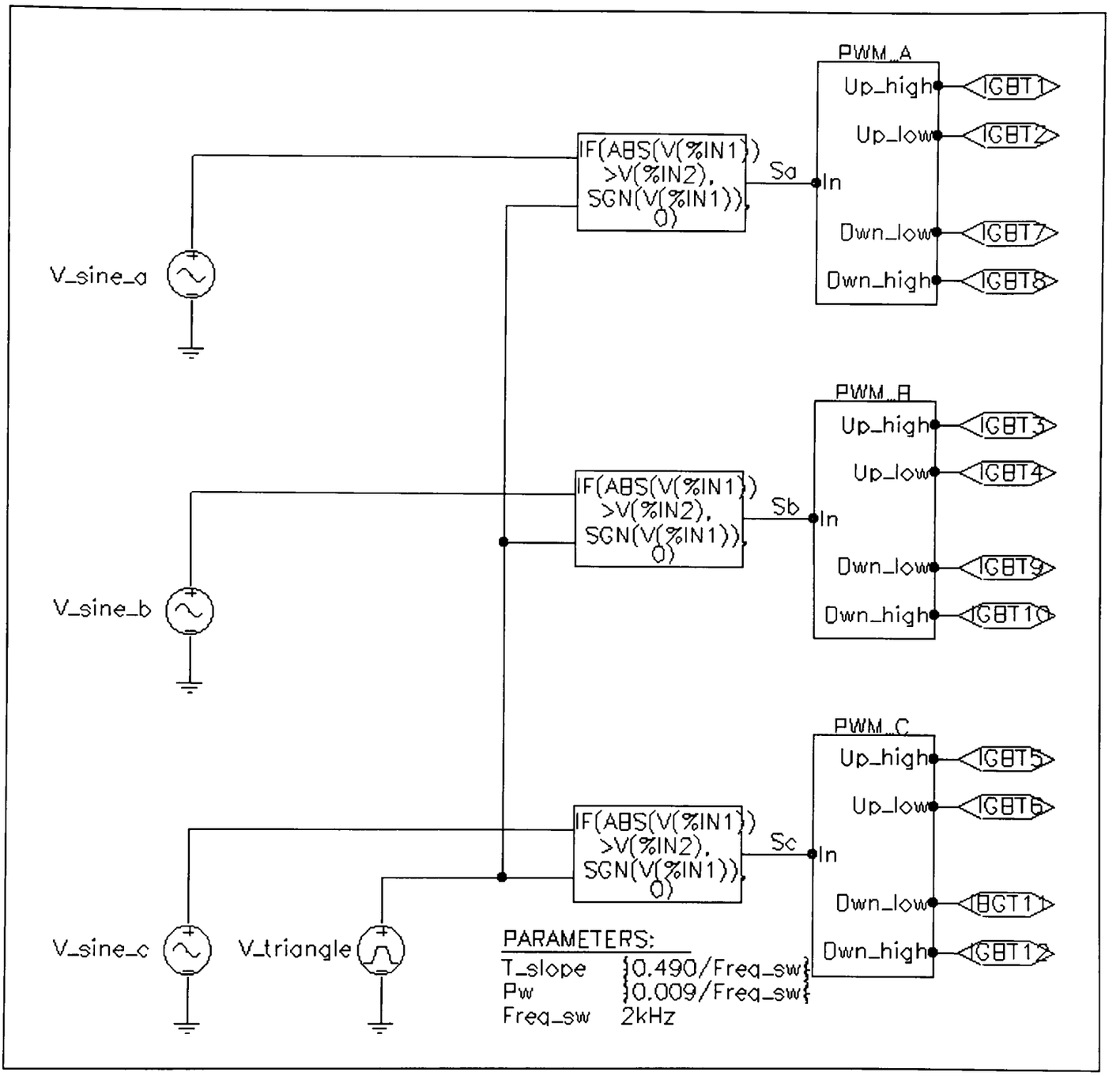


Figure 4.10: First layer of the NPC_PWM block of Figure 4.7.

As defined in the Mathcad document, the respective control signals are compared to the triangle wave using the signum ABM block. The ABM block operates according to Table 4.2. The signum function (sgn(x)) has the same

definition as in the Mathcad document. Note that when the conditional statement in Table 4.2 is true, the output has three possible values: -1,0, and 1.

Table 4.2: Truth table for ABM block in Figure 4.11

IF	OUTPUT
$\lvert V_1 > V_2 \rvert$ is true	sgn(V_1)
$\lvert V_1 > V_2 \rvert$ is false	0

The PWM_x block contains four ABM blocks as shown in Figure 4.12. These blocks perform the respective equation listed below each block. For the topmost block, the equation follows Table 4.3.

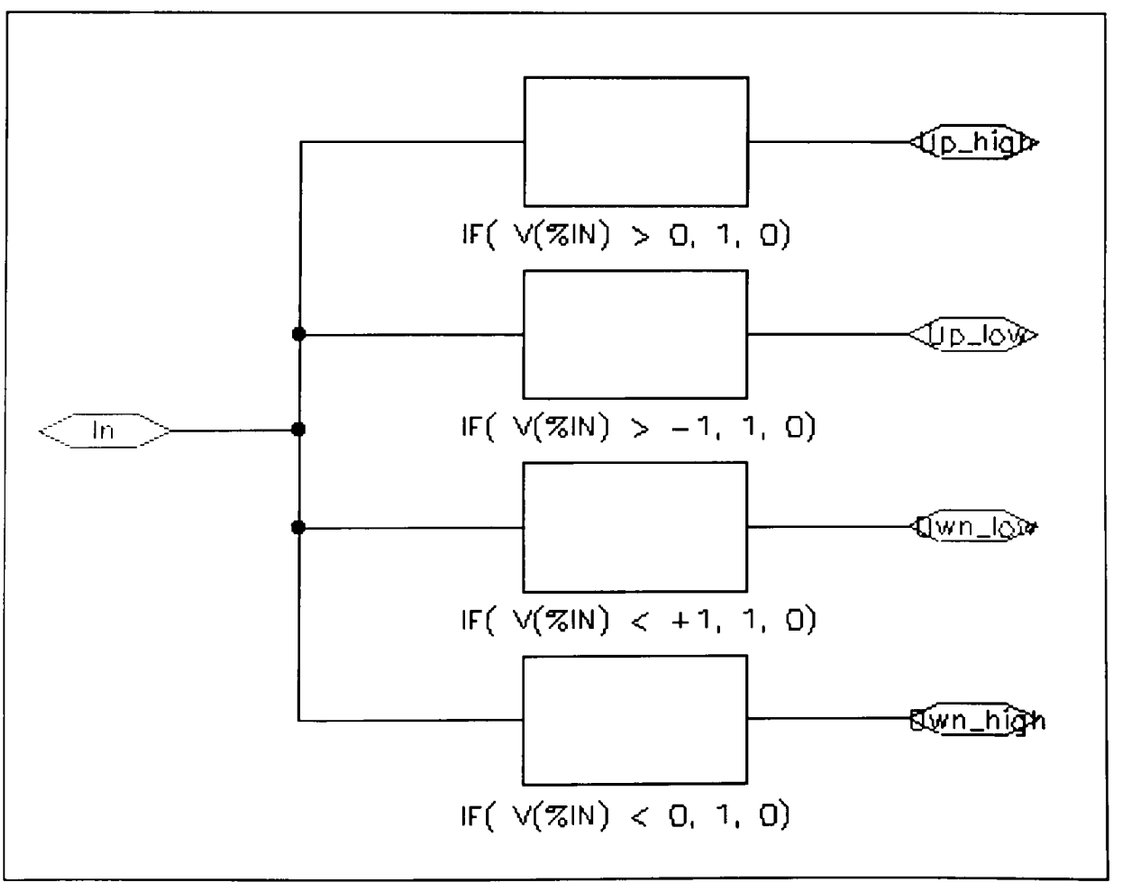


Figure 4.11: PWM_x block of Figure 4.10

Table 4.3: Truth table for ABM block in Figure 4.12

IF	OUTPUT
$V_{in}>0$ is true	1
$V_{in}>0$ is false	0

Notice the change in the conditional statement for each of the four ABM blocks. These conditional statements as well as the others used in the NPC_PWM block are very similar to the equations used to generate the gate signals in the Mathcad document. The resulting four outputs from the PWM_x block are the gate signals for the four IGBTs in a particular leg of the NPCI.

The results from the simulation are given in the following figures. Notice the similarities between the Mathcad predicted waveforms and the Pspice simulation waveforms. Also, notice the ripple and the initial transient conditions in the line current waveforms. The ripple in the current waveforms has a frequency equal to the switching frequency.

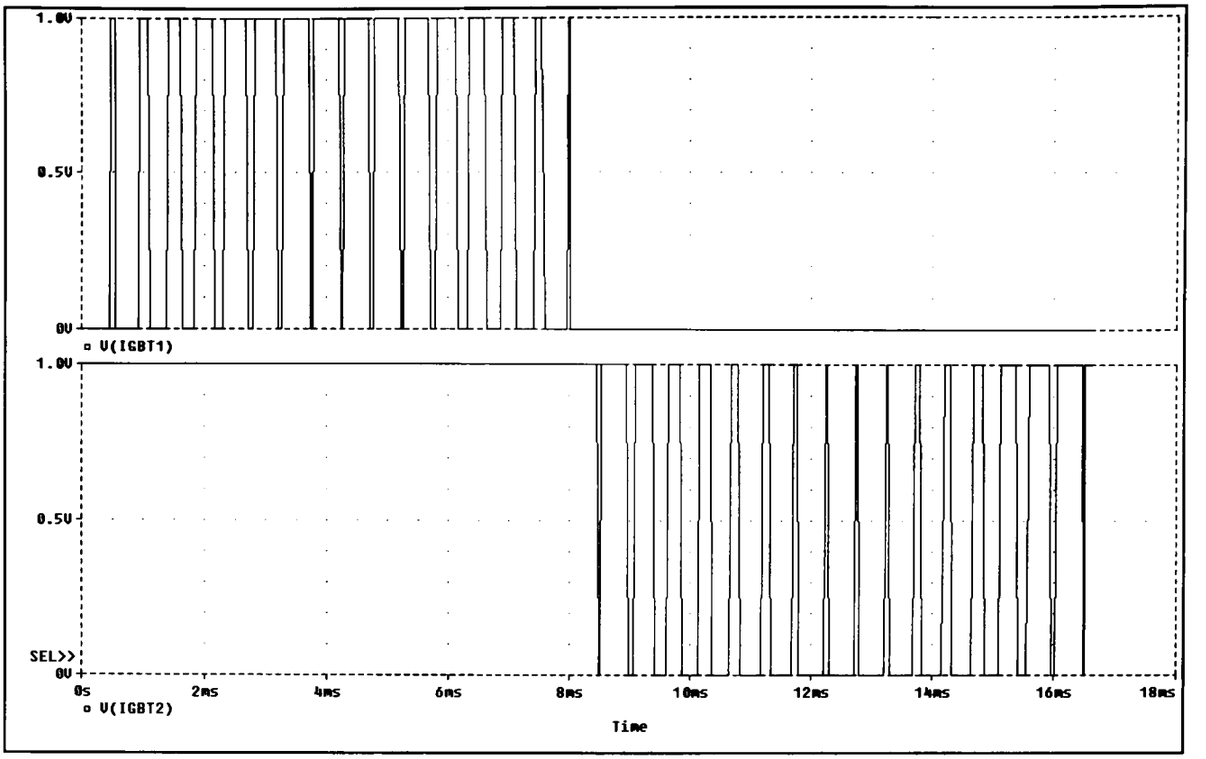


Figure 4.12: Gate drive signals for upper IGBTs of phase A

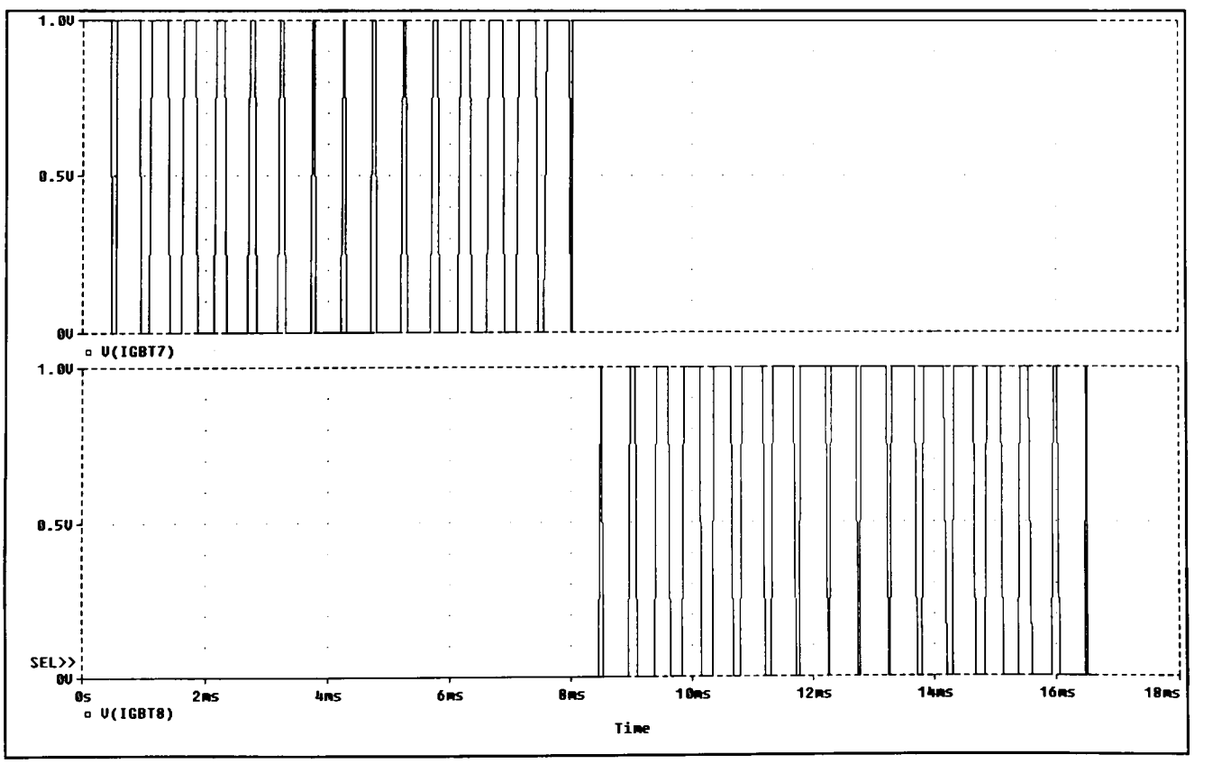


Figure 4.13: Gate drive signals for lower two IGBTs of phase A.

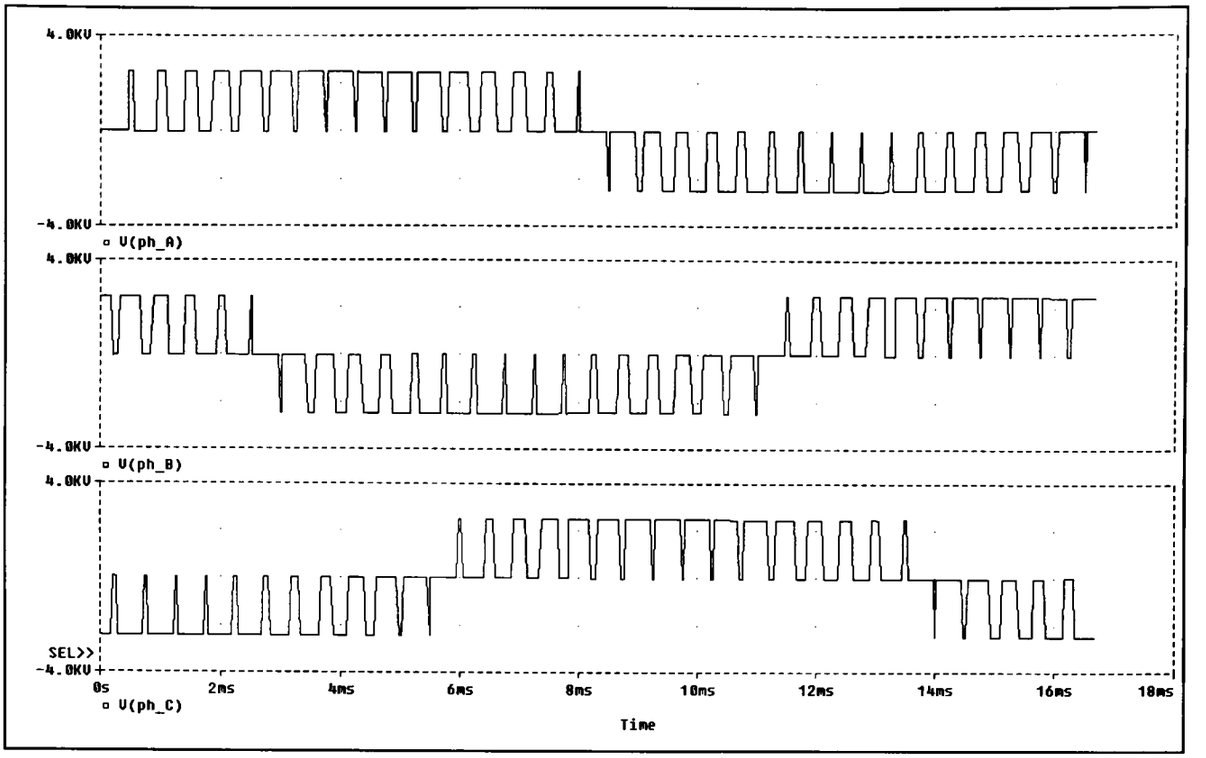


Figure 4.14: Line-to-neutral voltage waveforms

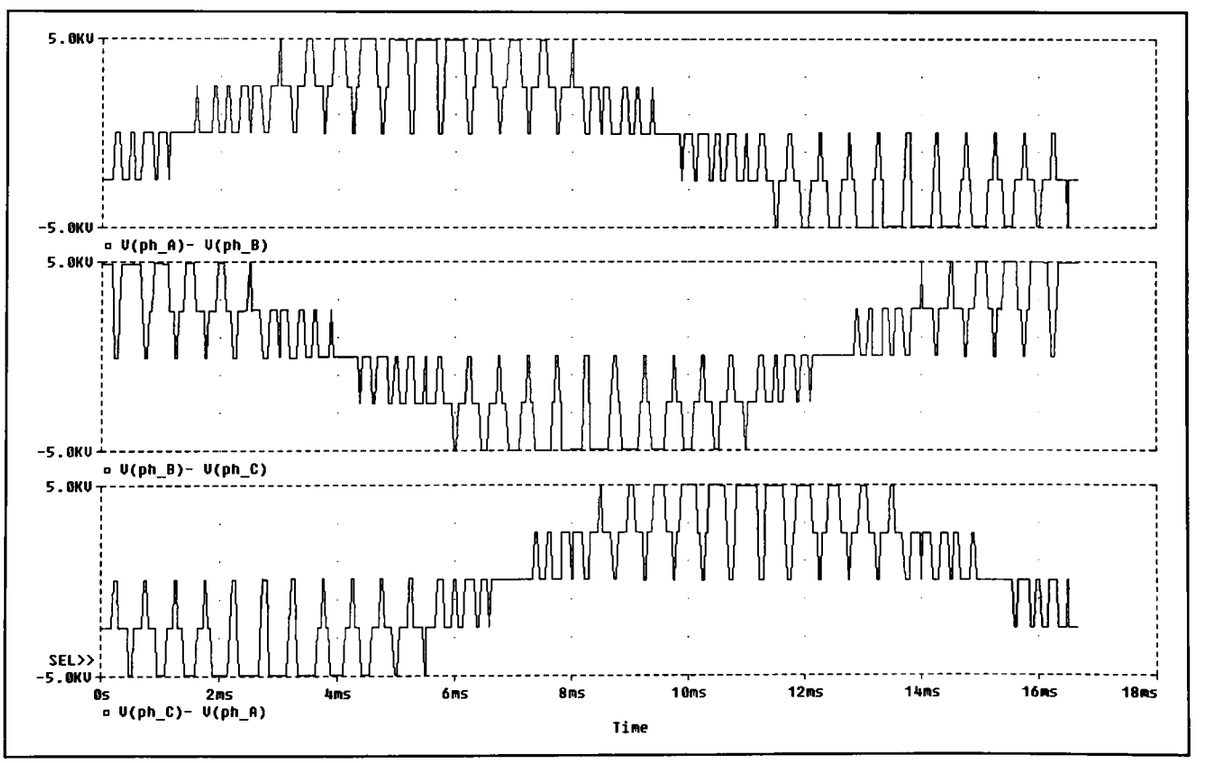


Figure 4.15: Line-to-line voltage waveforms.

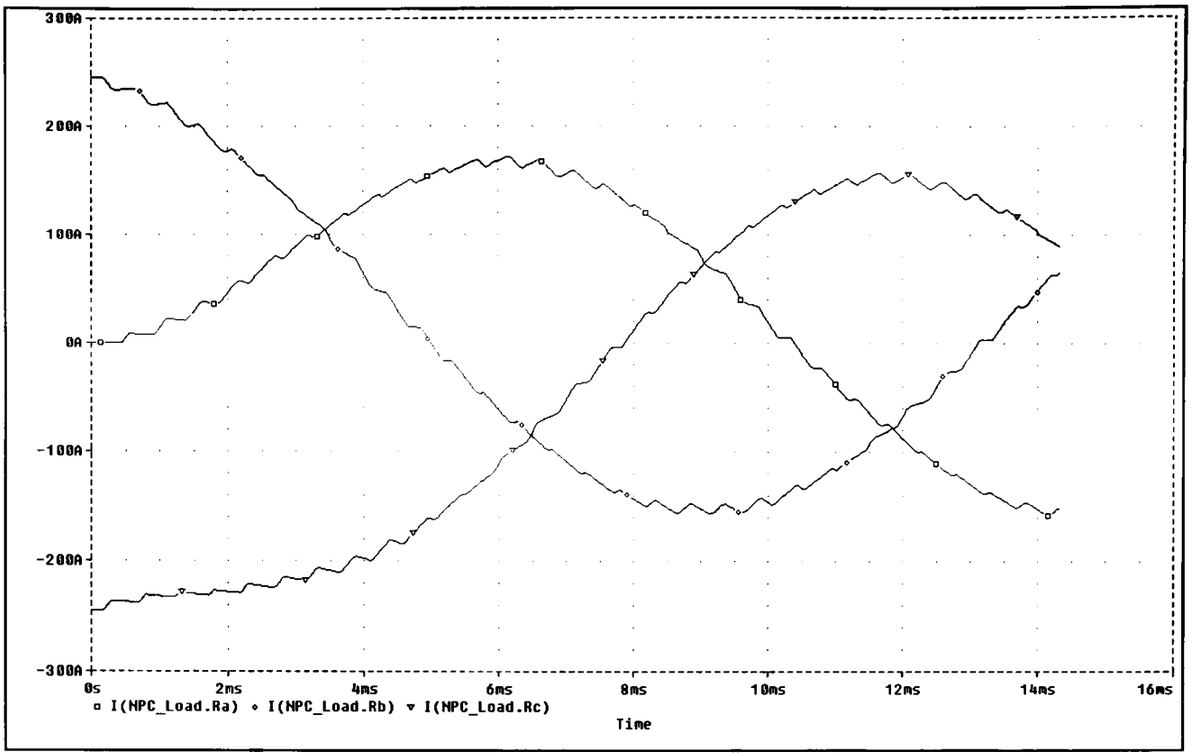


Figure 4.16: Line current waveforms.

CHAPTER V

PHYSICAL SYSTEM DESCRIPTION

The NPCI system can be broken into four major groups aside from a power supply and an output filter. Although an output filter is needed to smooth the NCPI output voltage waveforms, it is not necessary to the operation of the inverter. Multiple types of power supplies could be employed with the a neutral point clamped inverter, but for testing only a minimal supply is needed. Both the filter proposed and power supply utilized are covered later. The four basic sections of the inverter are the low power control circuitry, the gate drive circuitry, and the busbar, high power switch and clamping diode layout. Figure 5.1 shows the basic interconnects of the primary sections.

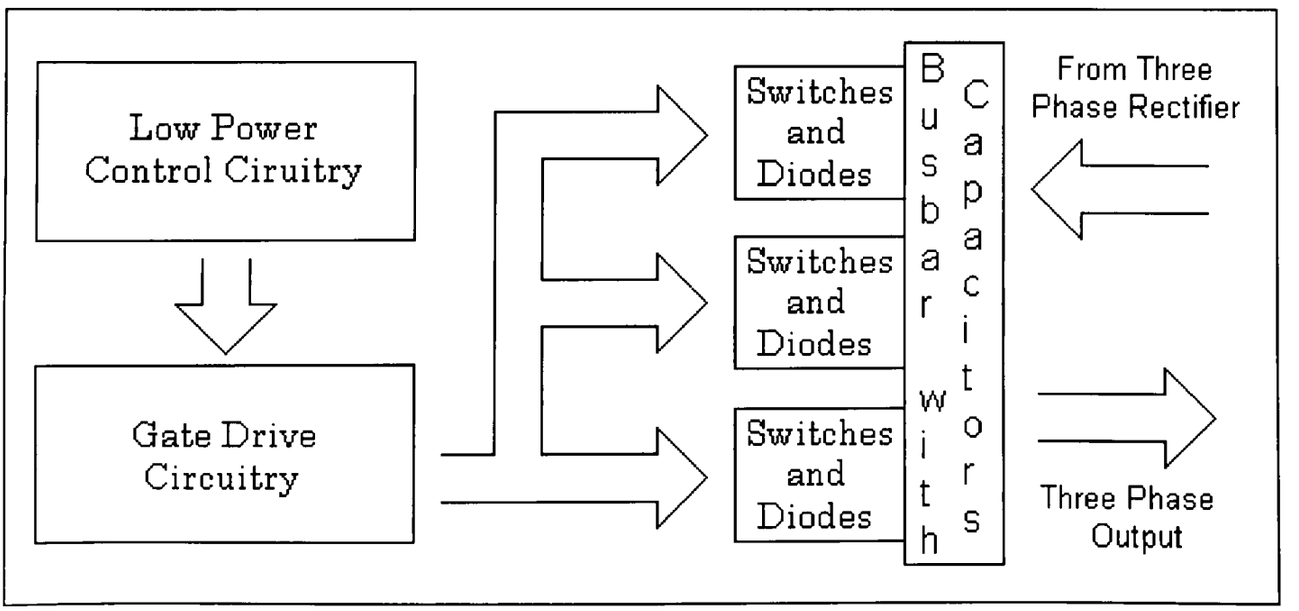


Figure 5.1: Basic interconnects of the primary sections of the NPCI.

Low Power Control Circuitry

As mentioned in the previous chapter, the gate signals for the IGBTs are stored in EPROMs. The information in the EPROMs is delivered to the driver boards via simple digital circuitry. A block diagram of the control circuitry is shown in Figure 5.2, and a schematic of the circuit is shown in

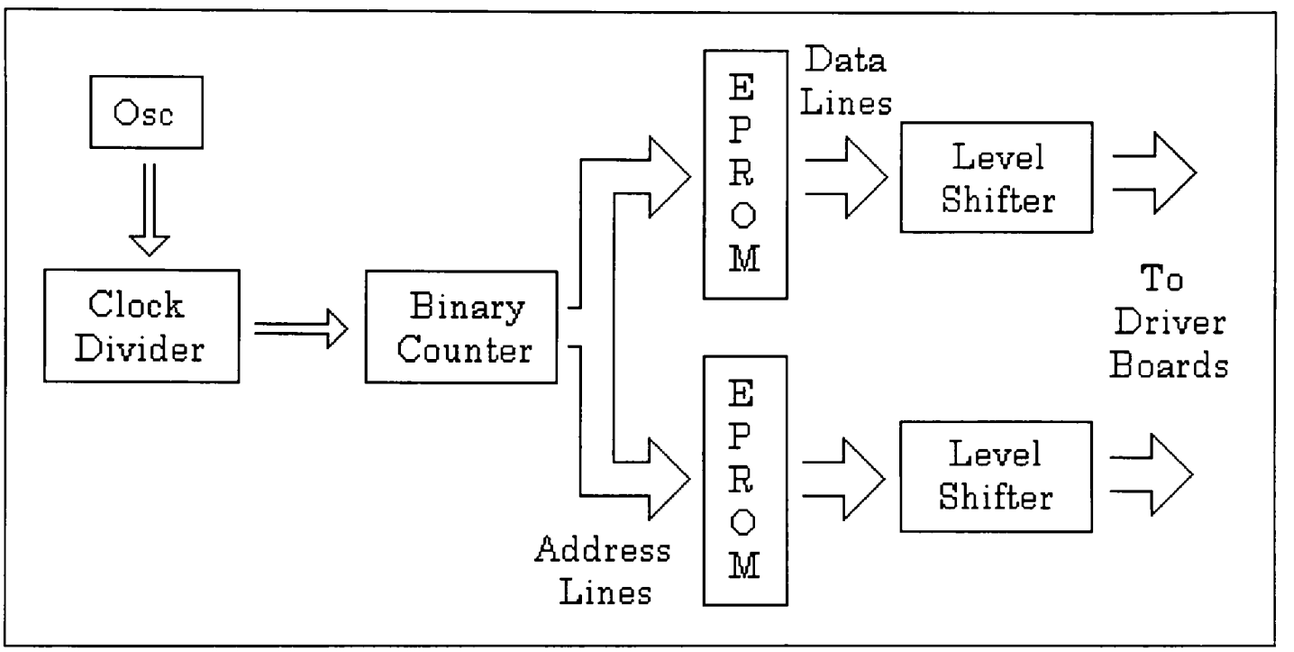


Figure 5.2: Block Diagram of low power control circuitry.

Figure 5.3. The crystal oscillator has a frequency of 1.2288 MHz. A clock divider is used to divide the oscillator frequency down to 61440 Hz (i.e. divide by 20). This frequency is obtained by multiplying 60 Hz times the number of samples per period of the gate signals, 1024.

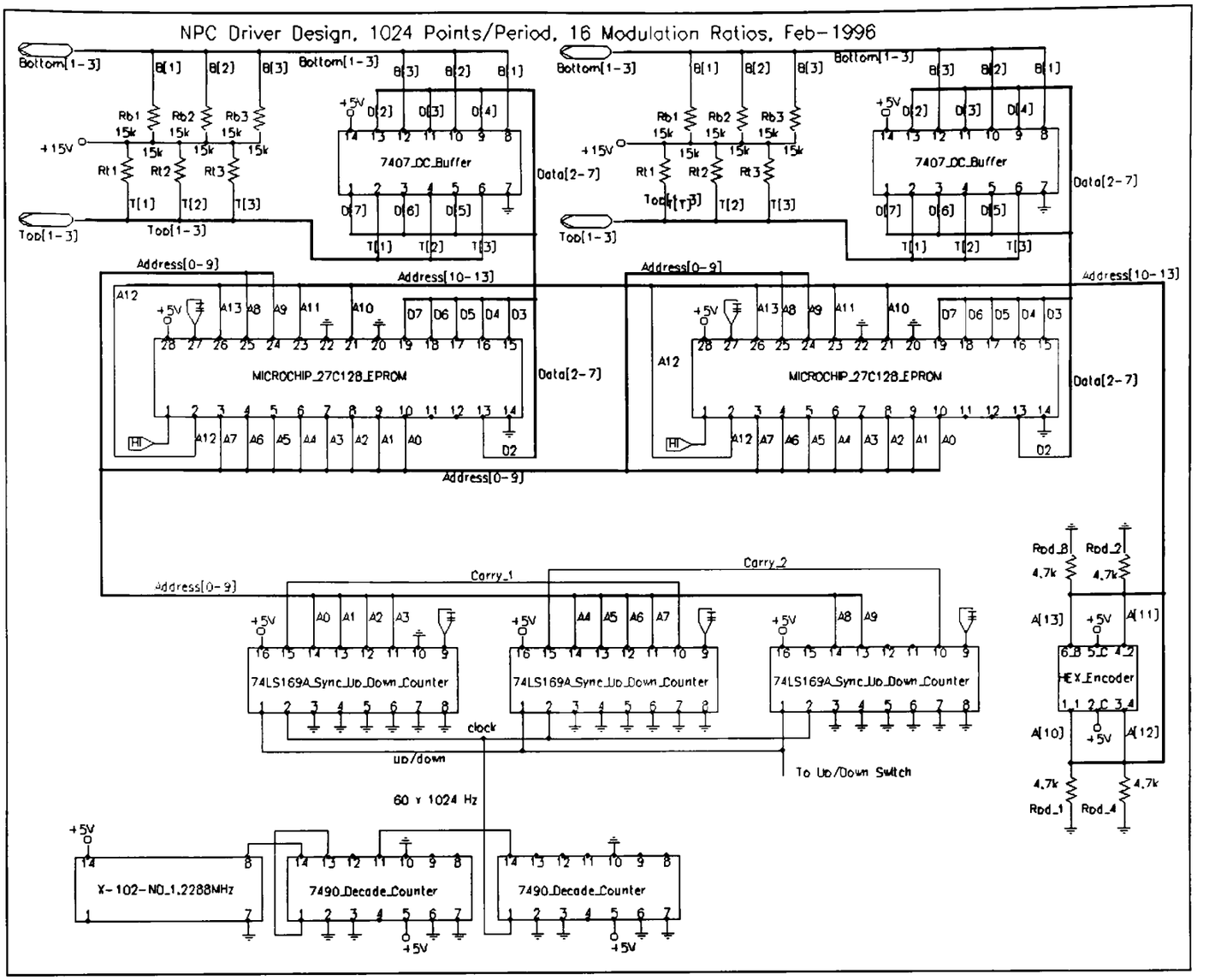


Figure 5.3: Schematic of low power control circuit.

The binary counter is composed of three, four bit binary counters in a cascade configuration. The cascade configuration allows the three four bit counters to act as a twelve bit counter. Ten of the twelve bits are fed into the EPROM address inputs with the remaining two counter bits left floating.

As the signals on the address lines count up from 0 to 1024, the data in the EPROM appear on the output lines of the EPROM and is fed into the level shifters. The level shifters are required to change the voltage range of

the data from a binary 0 V to 5 V to a binary 0 V to 15 V. The change in range is to meet the driver board requirement of a 15 V input. The upper four address lines of the EPROM are controlled by a manual switch that is used to address one of the 16 modulation ratios. As seen in the schematic, one set of counters is used to address both EPROMs simultaneously. However, the EPROM data goes only to the respective gate driver board.

Gate Driver Boards

The gate drivers are the interface between the low power digital control circuitry and the high power components of the inverter. The primary features of the driver boards include electrical isolation (2500 V) between the low voltage and high voltage components and voltage and current output capabilities such that the switches enter into and remain in hard saturation or cutoff. Furthermore, the boards monitor the collector-emitter saturation voltage during the on-time of each device in order to sense over-current conditions. Should such a condition occur, the boards automatically turn all switches off and can only be reset by cycling the power supply. The driver boards are compatible with both metal-oxide-semiconductor FETs (MOSFET) and insulated gate bipolar transistors (IGBT). Figure 5.4 shows a picture of one of the driver boards. The square boards with the three circular cores are

the isolation transformers are responsible for the 2500 V isolation between the high voltage side and the low voltage side.

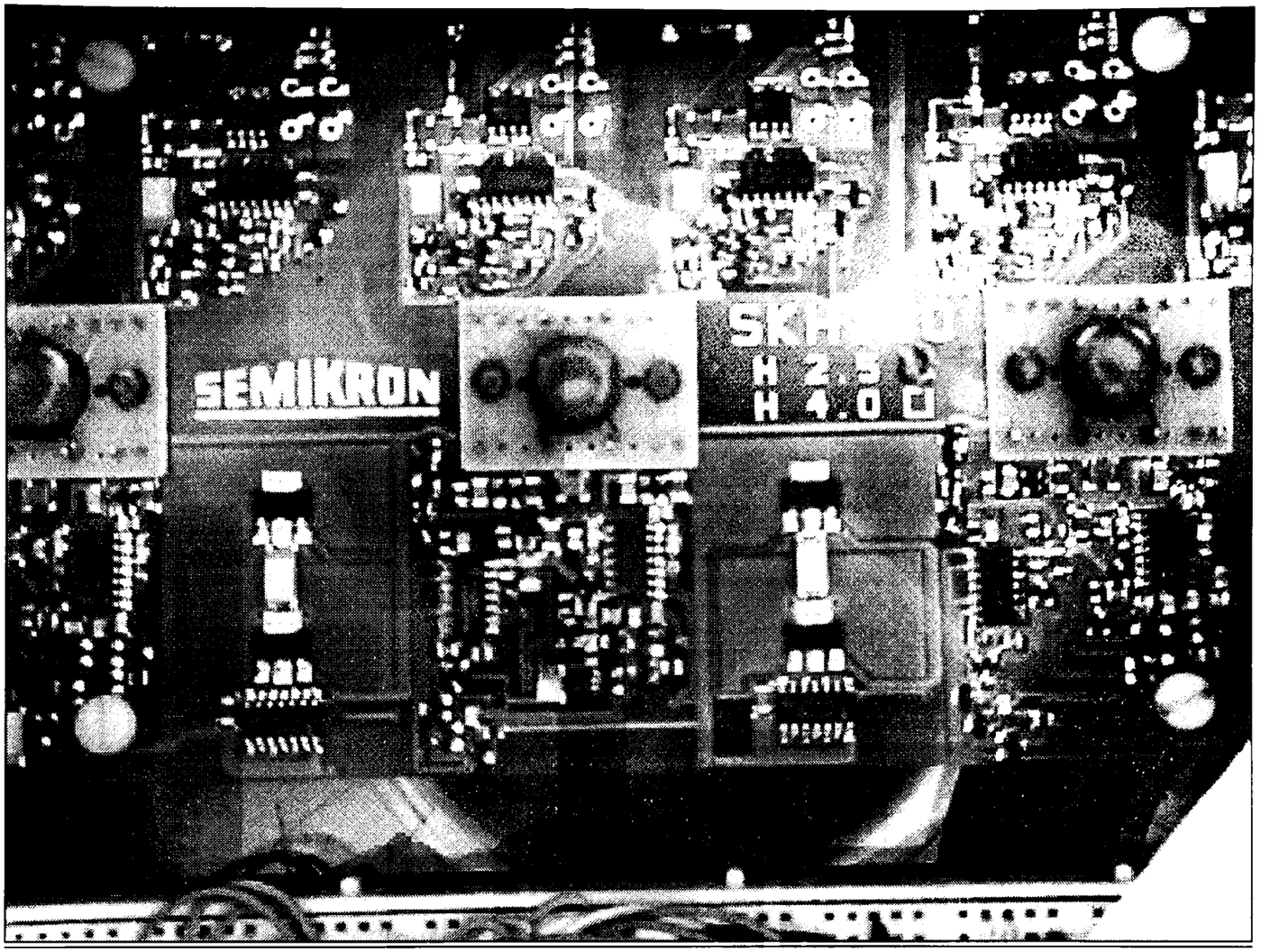


Figure 5.4: Picture of Semikron driver board

The driver boards are designed to control conventional three phase inverters. In so doing, these driver boards do not allow for adjacent switches in series to be simultaneously conducting (so called cross conduction lockout), and they also generate a 10 μs blanking time (allowing a switch to come to a steady state of operation during a transition). As mentioned before, the NPCI requires at times for adjacent switches in series to be simultaneously

conducting. The solution for using these boards with the NPCI is to use two driver boards with each board controlling two rows of switches. One board controls rows one and three, switches A1, B1, C1, A3, B3, and C3 as in Figure 4.1, and the other board controls rows two and four, switches A2, B2, C2, A4, B4, and C4 as in Figure 4.1. Now, the use of the two EPROMs is fully understood. The EPROM with the data for rows 1 and 3 feeds the driver board for rows 1 and 3, and the EPROM with the data for rows 2 and 4 feeds the driver board for rows 2 and 4.

Switches, Diodes, and Busbar

The switches used in the system are 600 V, 165 A IGBTs from International Rectifier. The IGBTs come inmodules with two devices which are in a series connection. The diodes are 800 V, 45 A devices from Semikron. The diodes also come in modules of two devices with a series connection.

Also attached to the busbar between the positve, negative, and neutral layers are low frequency and high frequency capacitors. The large low frequency capacitors provide the DC bus filtering while the smaller high frequency capacitors absorb high frequency switching ripple.

The high switching speeds of the IGBTs necessitate low inductance connections between the switches and the diodes. A layered busbar for

connecting the switches and diodes provides the low inductance connections. The busbar is constructed from 0.040 inch aluminum with the dielectric being 0.030 inch thick plastic (polyethelene).

Two IGBT modules and one diode module make one leg of the inverter. Figure 5.5 shows the busbar connections for one leg, and Figure 5.6 is the cross-section of the busbar layout. Figure 5.7 is a photograph of the switches, diodes, and busbar assembly. Notice the tabs on either end of the busbar in Figure 5.7 for the capacitors.

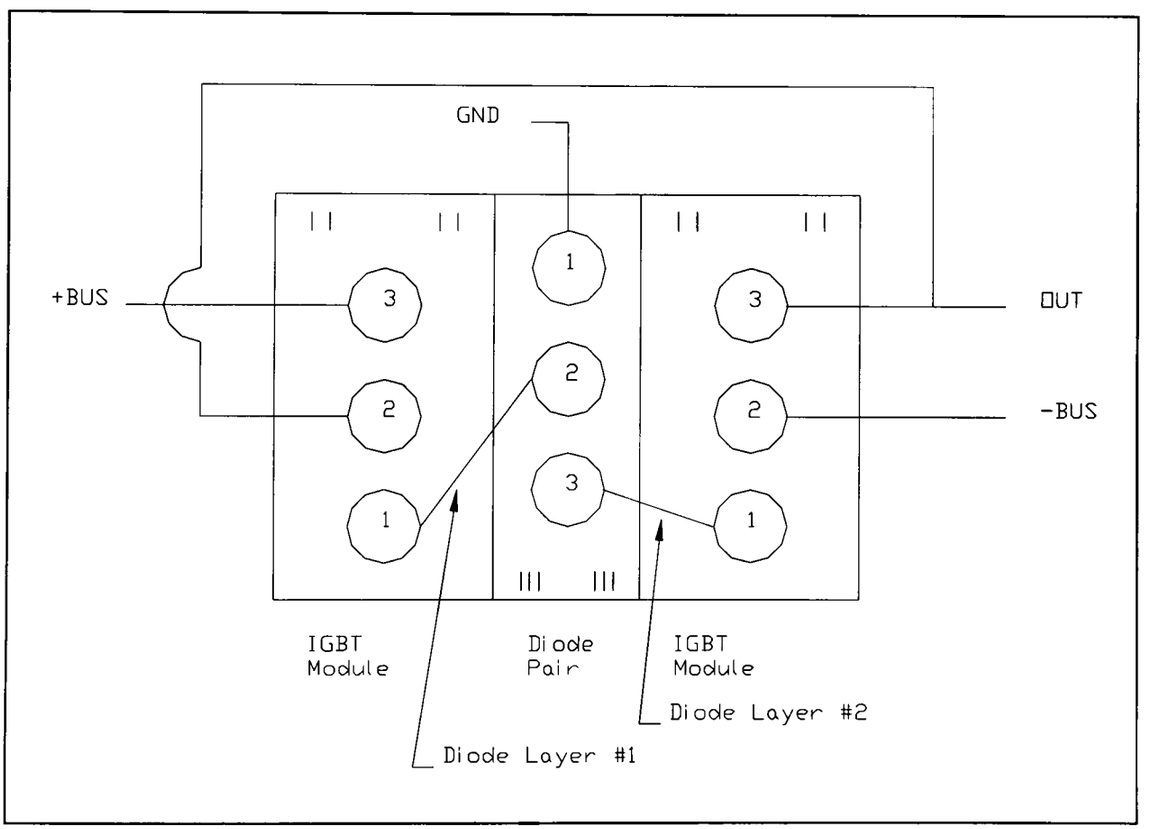


Figure 5.5: Busbar connections for one leg of inverter.

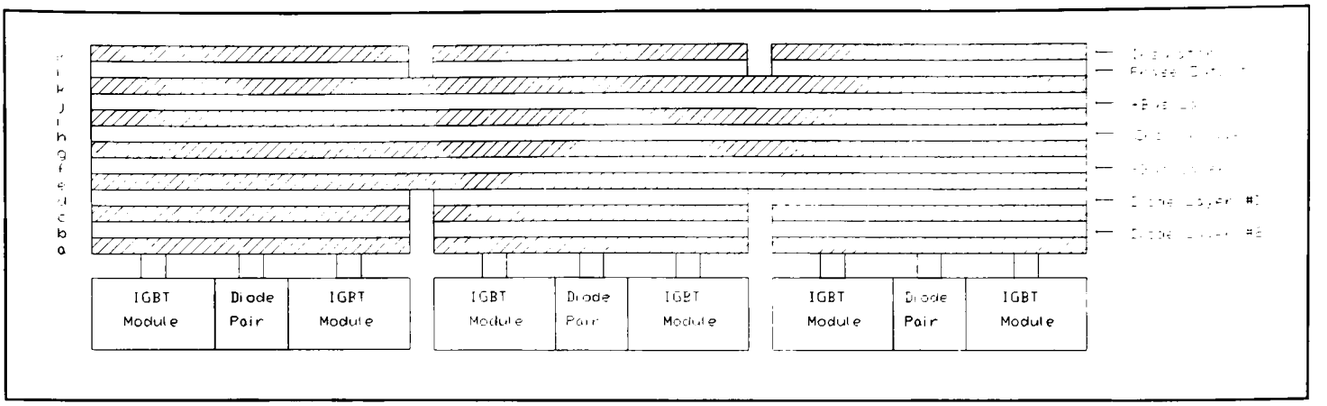


Figure 5.6: Cross section of busbar layout.

The tabs across the top of the inverter are the phase outputs. Also, the black modules are the IGBTs and the white modules are the diodes.

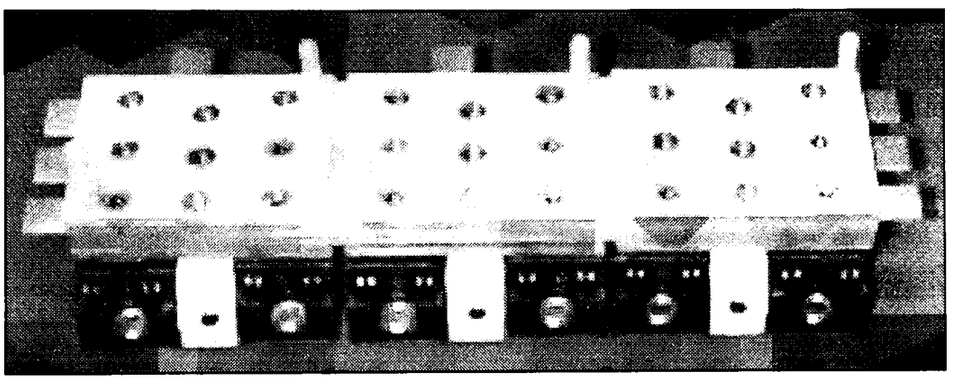


Figure 5.7: Photograph of switches, diodes, and busbar assembly.

Figure 5.1 shows an input to the busbar from a three phase rectifier. For the purposes of this project, the rectifier circuit needs only to meet minimum requirements i.e. rectification of a power source. The rectifier is a simple three phase diode rectifier as shown in Figure 5.8. The output of the rectifier connects to the positive and negative busbar tabs (see Figure 5.6). The three phase power source is a motor-controlled Variac (autotransformer) capable of 0-560 V output. To prevent the neutral point of the inverter from

floating, the neutral from the Variac is connected to the neutral of the inverter.

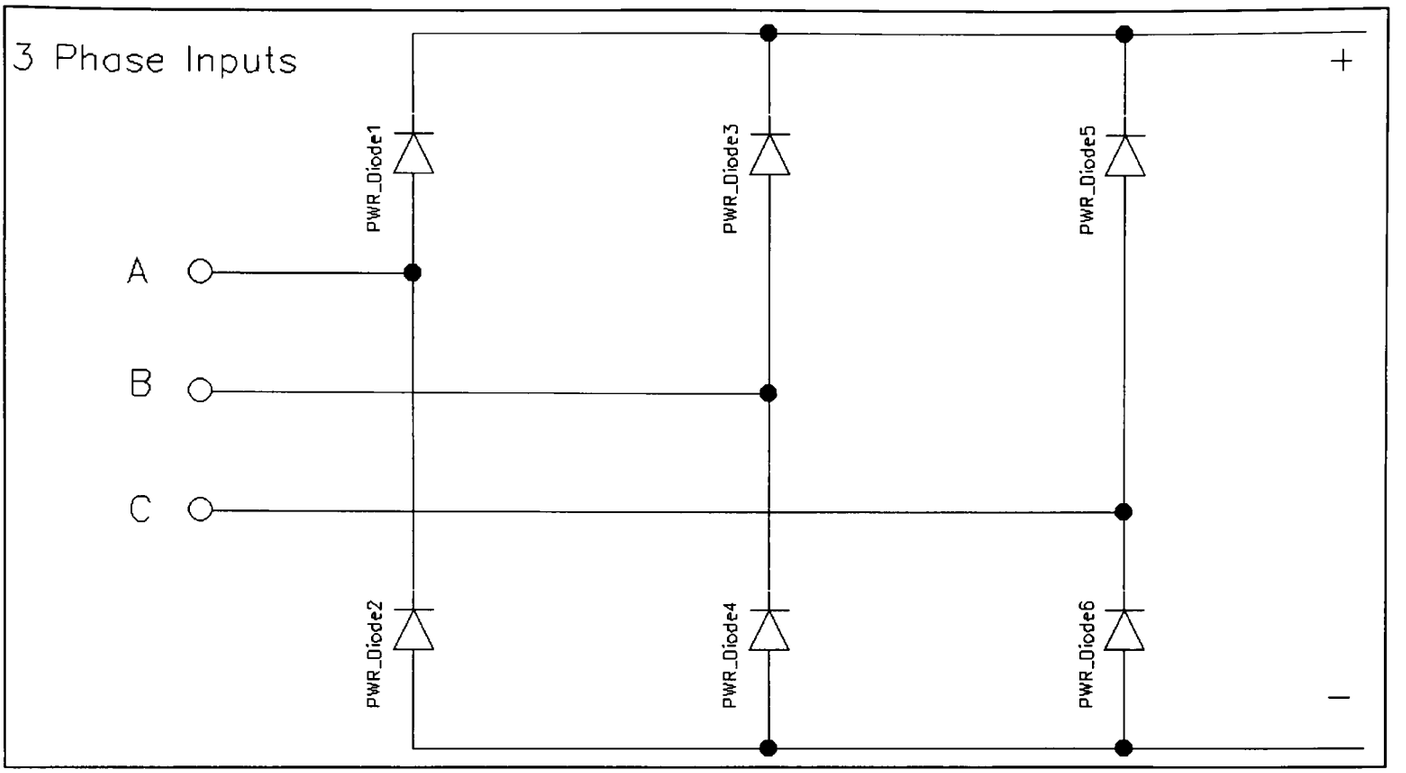


Figure 5.8: Rectifier circuit.

Output Filter

Although the currents drawn from the inverter are sinusoidal in nature with some switching frequency ripple, an output filter can be used to further shape the output current waveform. Figure 5.9 shows the schematic of the filter.

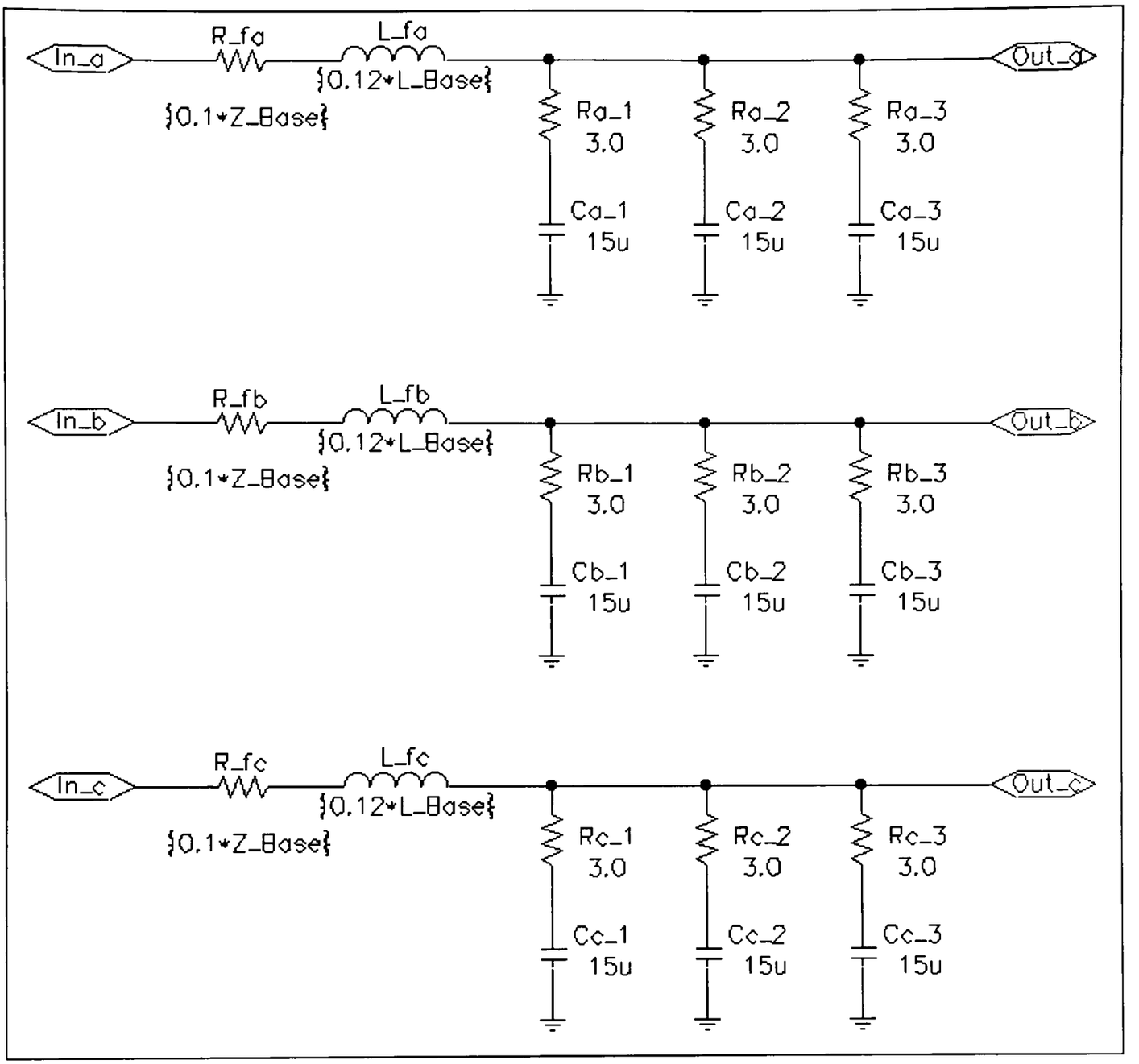


Figure 5.9: Filter schematic

Inverter Load

The initial load for testing the functionality of the inverter was a 1 hp, 208 V induction motor. A larger load of 10 hp has also been utilized.

Figure 5.10 shows a picture of the inverter test platform. The digital circuitry is on the breadboard, the driver boards are connected to the breadboard via two ribbon cables, and the driver boards are connected to the IBGTs and diodes via six ribbon cables. The capacitors are connected to either end of the busbar, and the rectifier is made up of the three white diode modules on the far left of the picture.

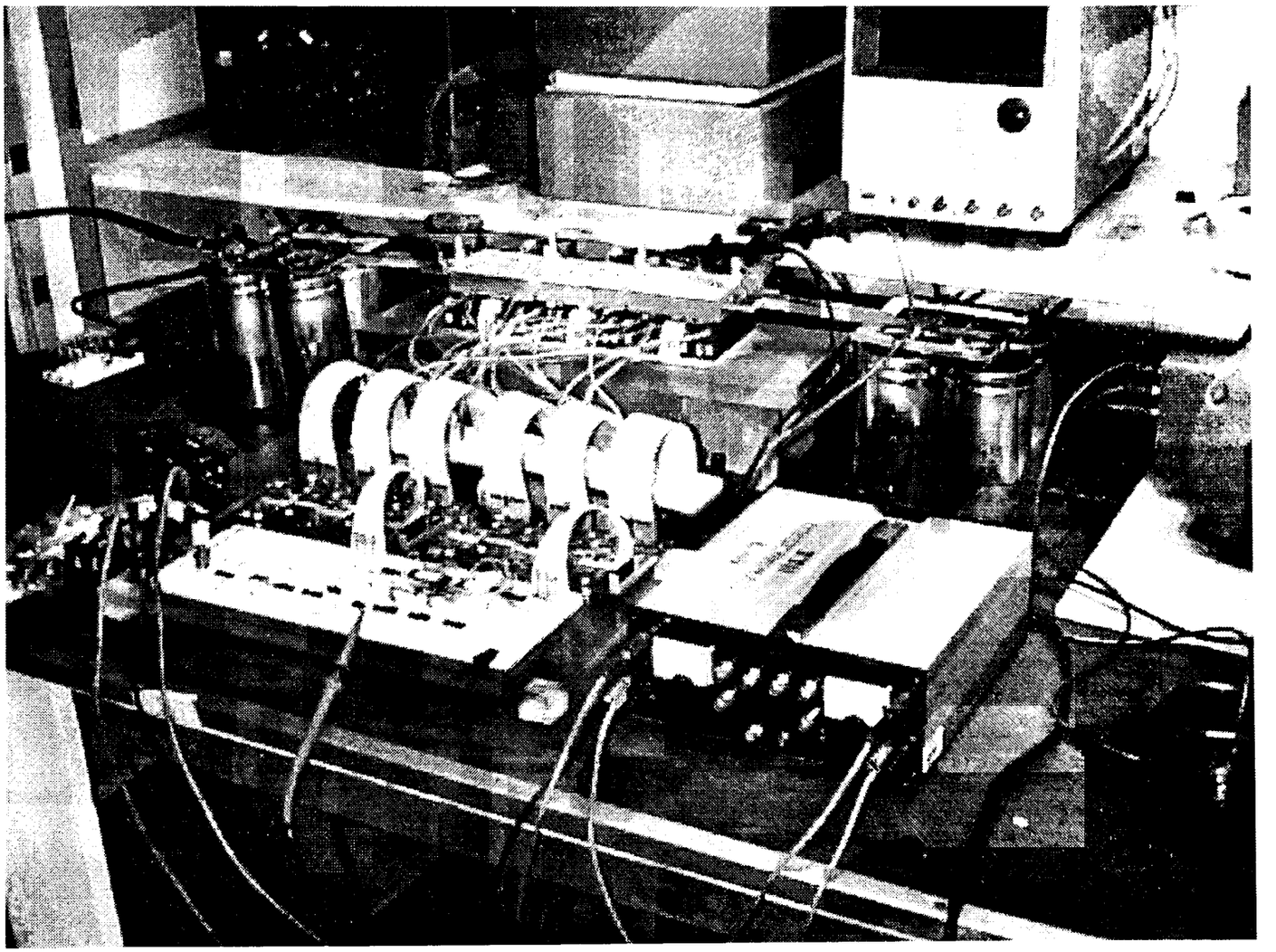


Figure 5.10: Picture of inverter test platform.

CHAPTER VI

RESULTS AND DATA ANALYSIS

All figures in this chapter were obtained using a digital oscilloscope that captured the particular trace from the oscilloscope screen and created a bitmap file containing the trace. Note the captions for pertinent information concerning the type and scale of trace shown. The use of high voltage differential probes and magnetic current probes change the y-axis scaling on some of the waveforms (Figures 6.8-6.10).

Results for 1 hp, Three Phase Induction Motor, No Load

Figures 6.1-6.8 show the preliminary test results. The goal of the initial tests were to verify the functionality of the inverter. The gate signals and voltage waveforms should be compared to those from the Mathcad document and the PSpice simulation.

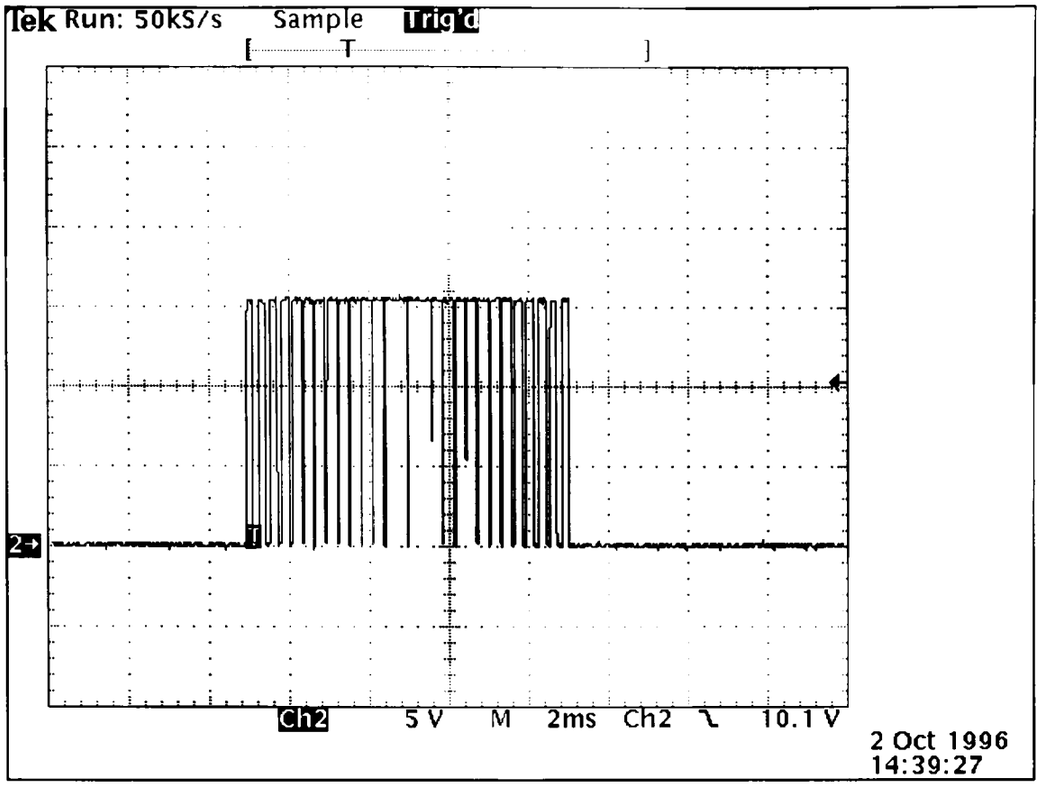


Figure 6.1: Gate signal for IGBT A1 in Figure 4.1

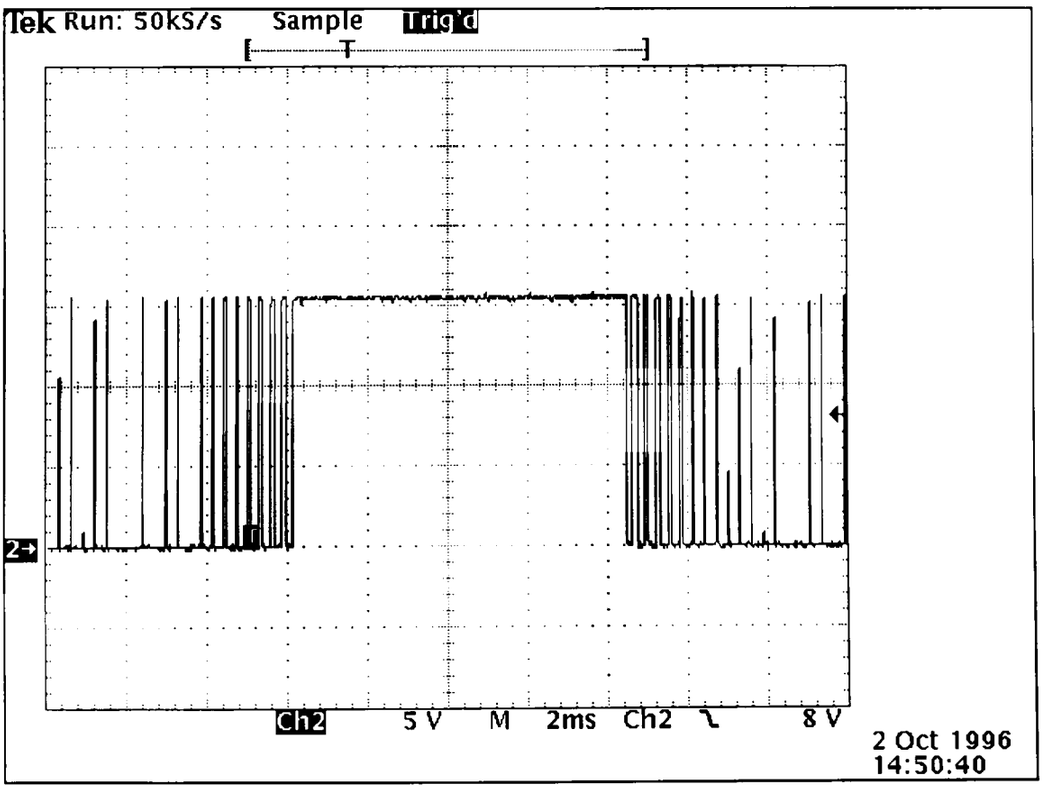


Figure 6.2: Gate signal for IGBT A2 in Figure 4.1

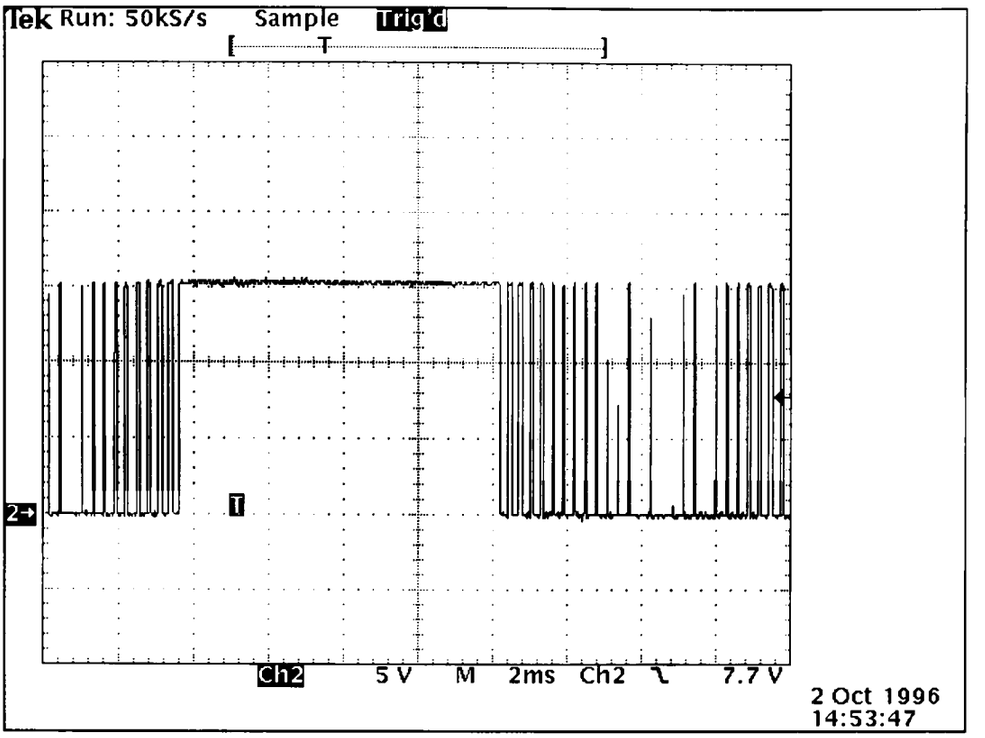


Figure 6.3: Gate signal for IGBT A3 in Figure 4.1

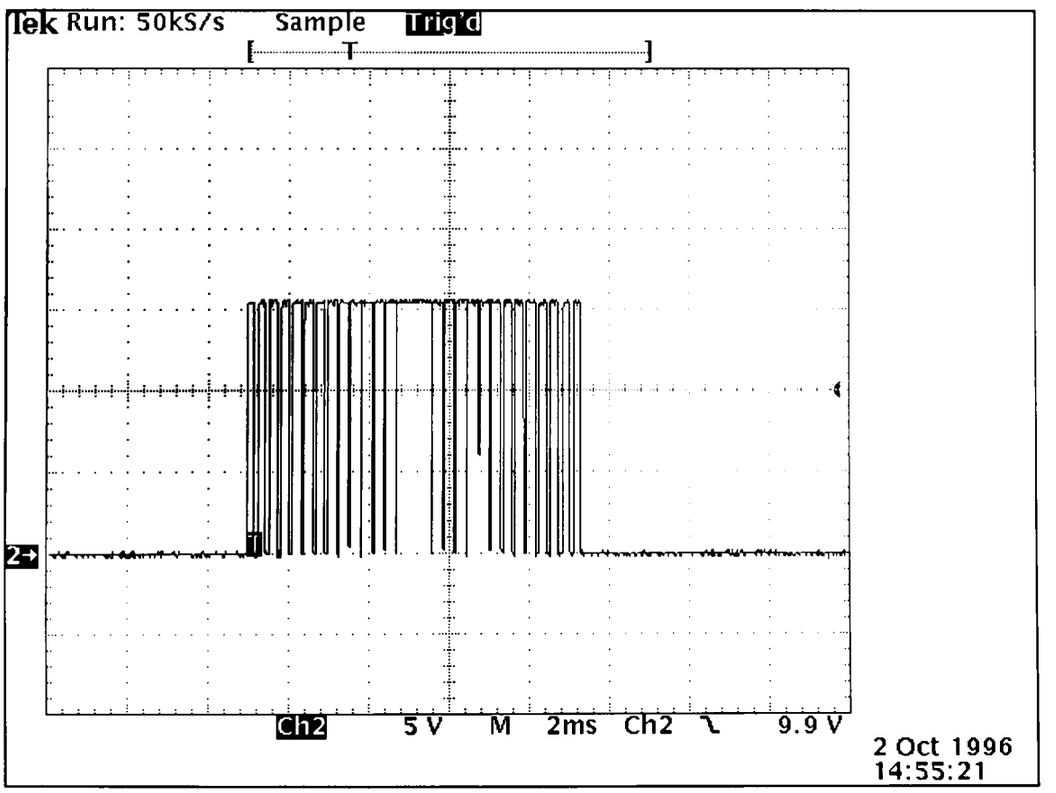


Figure 6.4: Gate singal for IGBT A4 in Figure 4.1

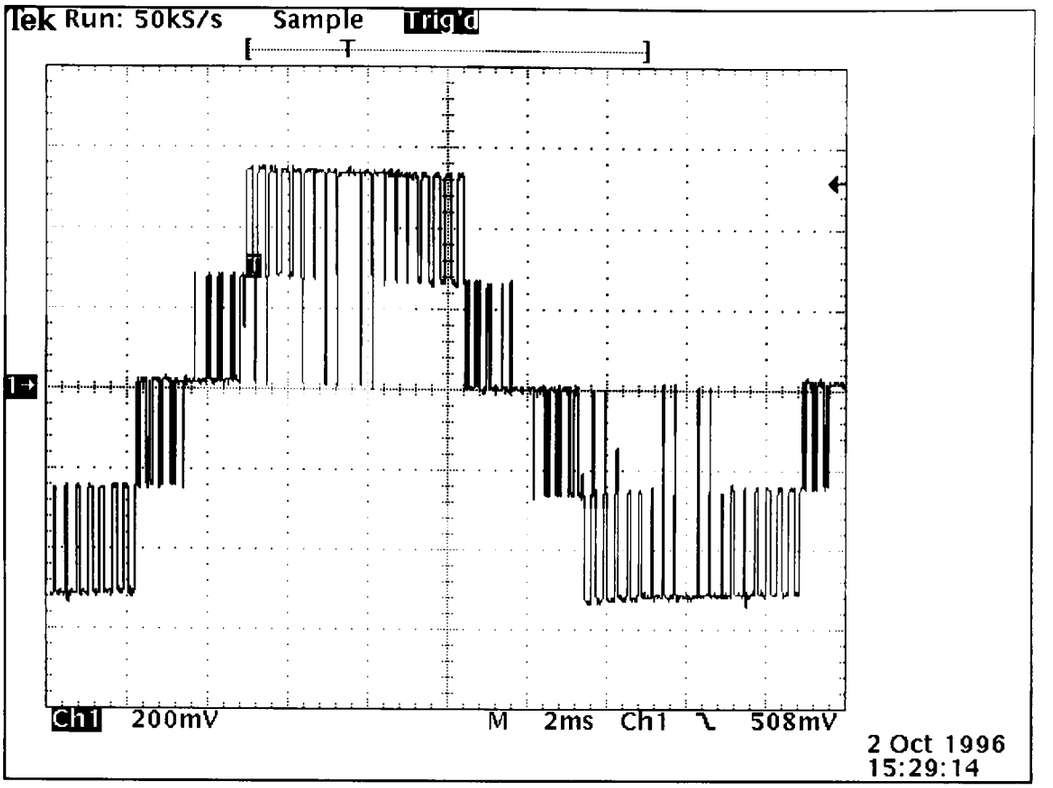


Figure 6.5: Line-to-line voltage - Phase A-Phase B, 100 V/div

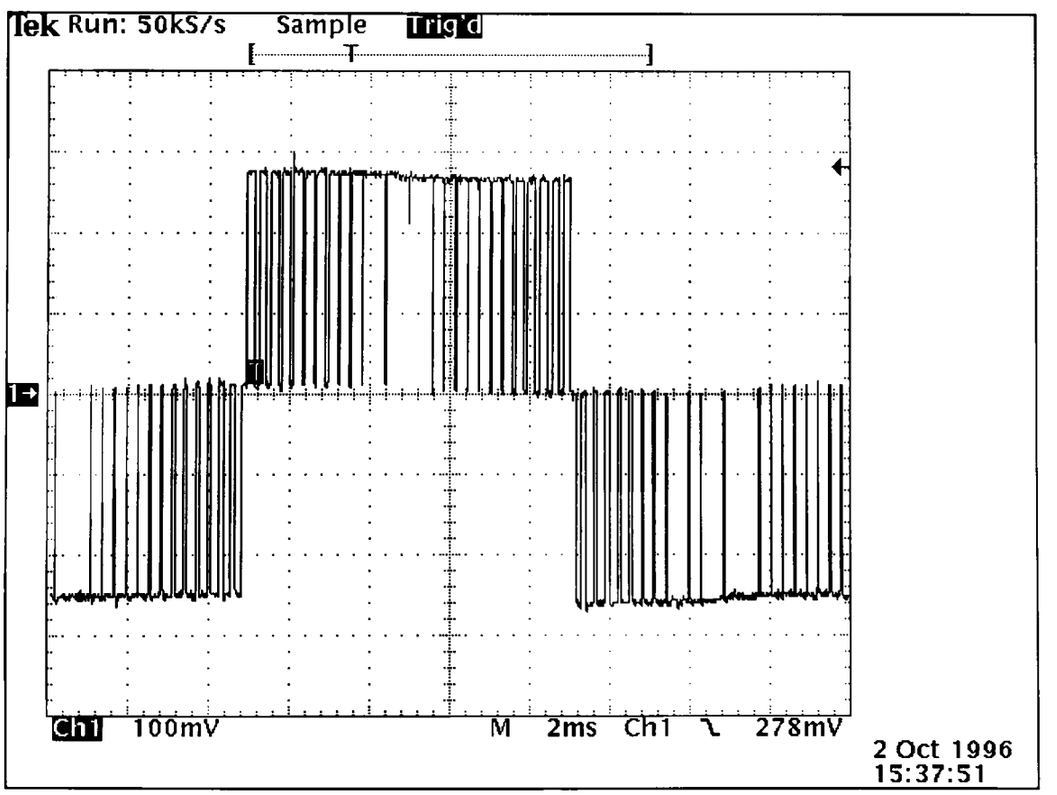


Figure 6.6: Line-to-neutral voltage for Phase A - 50 V/div

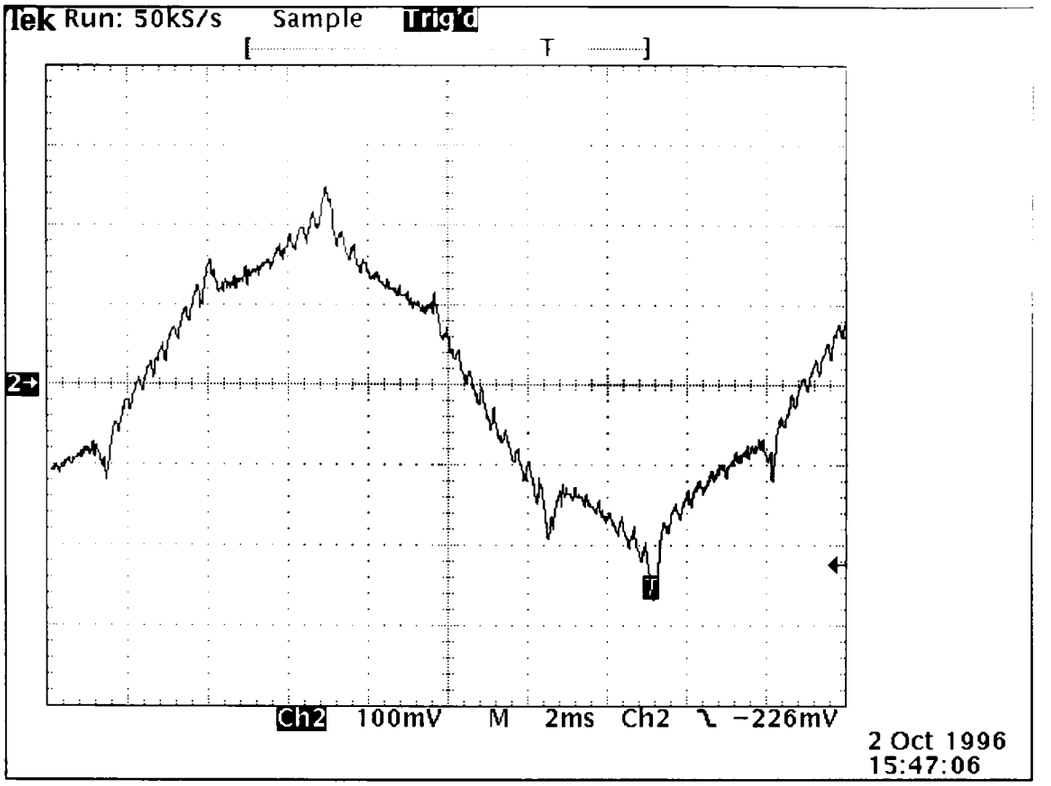


Figure 6.7: Line current for Phase A, 1 A/div

Results for 10 hp, Three Phase Induction Motor

Figures 6.8 through 6.9 show the waveforms for a 10 hp motor as the load for the NPCI. The two current waveforms indicate two different loads on the motor. For the first current waveform, the load on the motor is approximately 10.8 kW. For the second current waveform, the load on the motor is approximately 21.6 kW. Both current waveforms correspond to the voltage waveform of Figure 6.8.

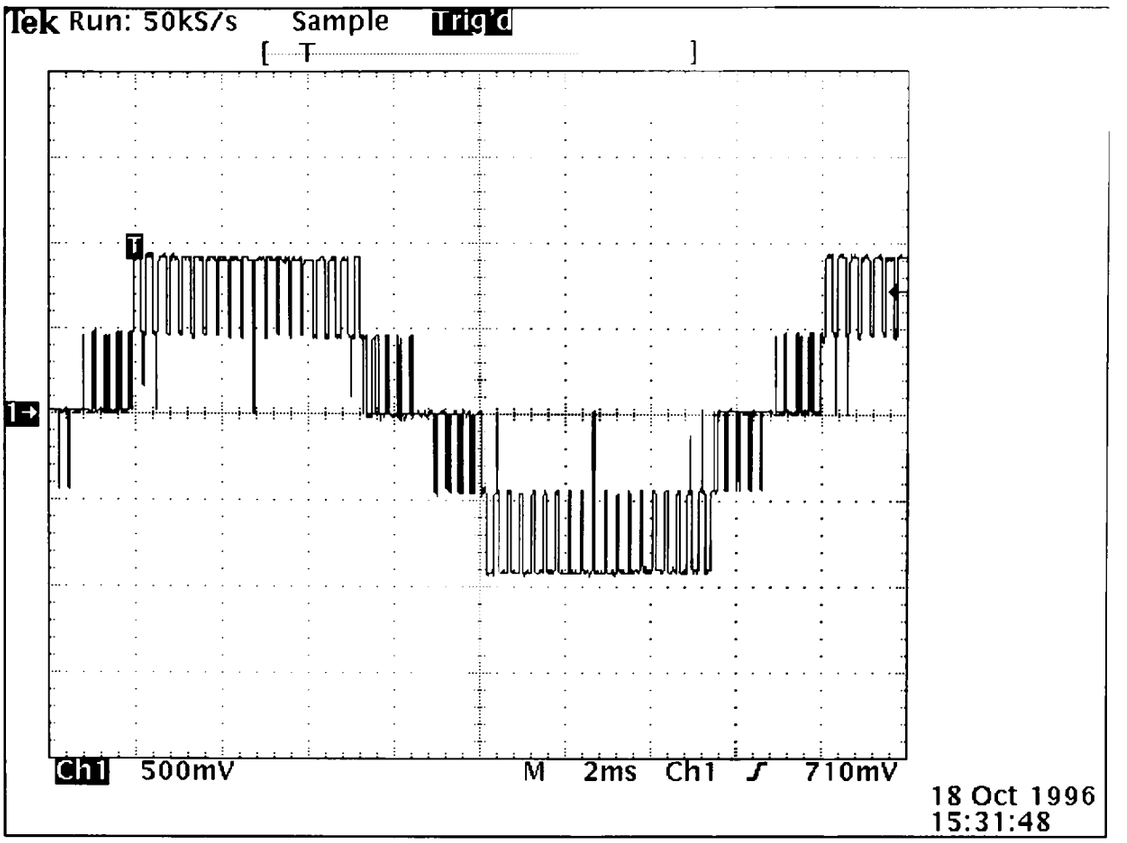


Figure 6.8: Line-to-line voltage - Phase B Phase C, 250 V/div

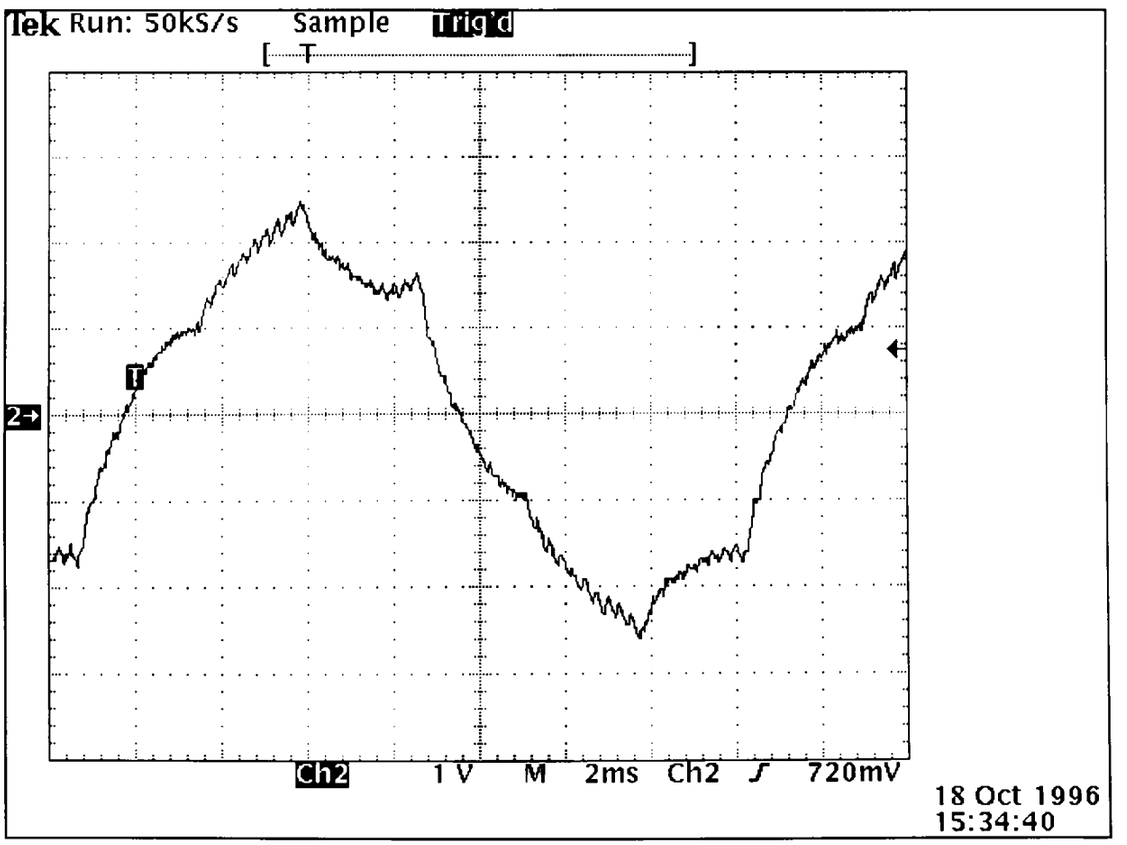


Figure 6.9: Line current, 10 A/div

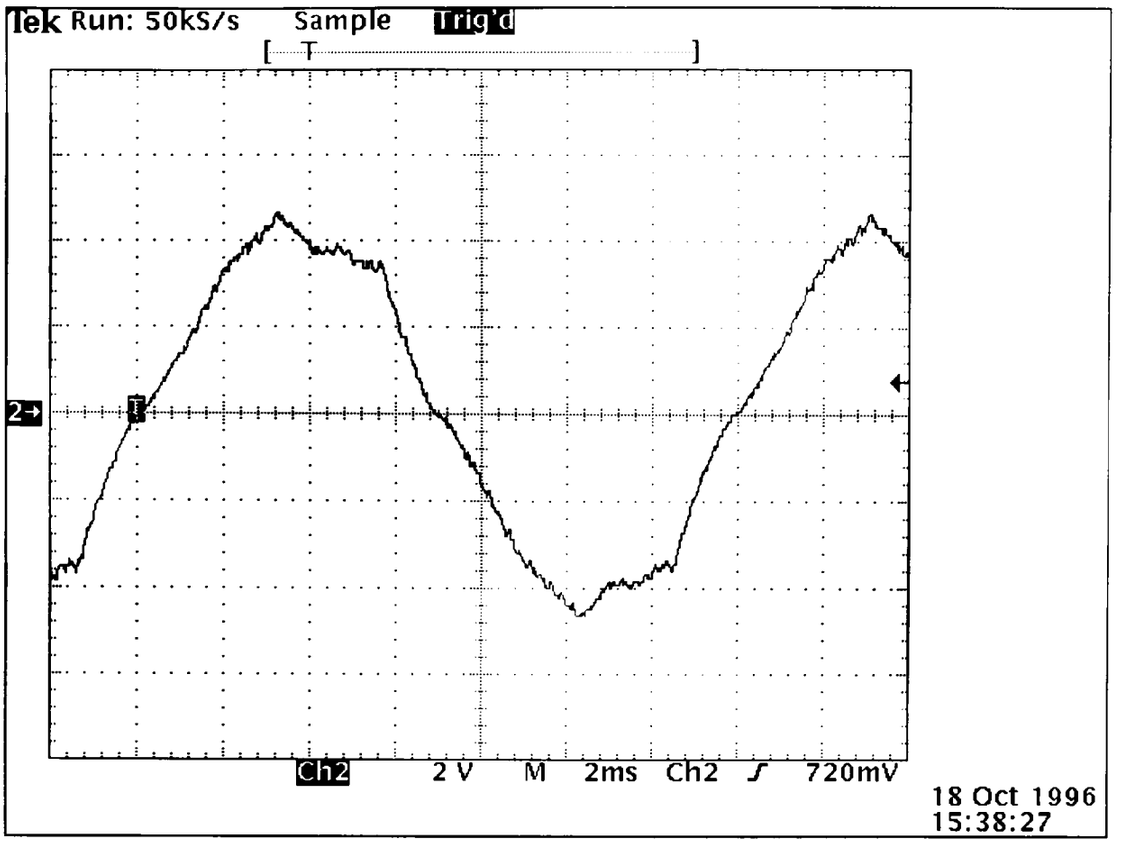


Figure 6.10: Line current, 20 A/div

CHAPTER VII

CONCLUSIONS AND COMMENTS

This report details the design and construction of a neutral point clamped inverter. This NPCI topology can use either IGBTs or power MOSFETs (metal-oxide semiconductor field-effect transistor) as switching devices. Although there are other semiconductors available for higher power uses, they are not as easily controlled as IGBTs and power MOSFETs.

The NPCI is only a part of a power supply structure capable of use in any power grid given DC bus voltage limitations. The bus voltage limit is primarily dictated by the devices used for the switches. The current voltage rating of IGBTs is about 1000 V. As technology for fabrication of semiconductors improves, the voltage limitation of the switches will increase, and the use of the NPCI topology will have an even broader range of applications. Furthermore, this same NPC topology can be used as a converter. A converter would take the place of the three phase rectifier and because of the converter's four quadrant operation and controlled rectification capability the power factor, the harmonics injected in the utility, and the direction of power flow could all be controlled.

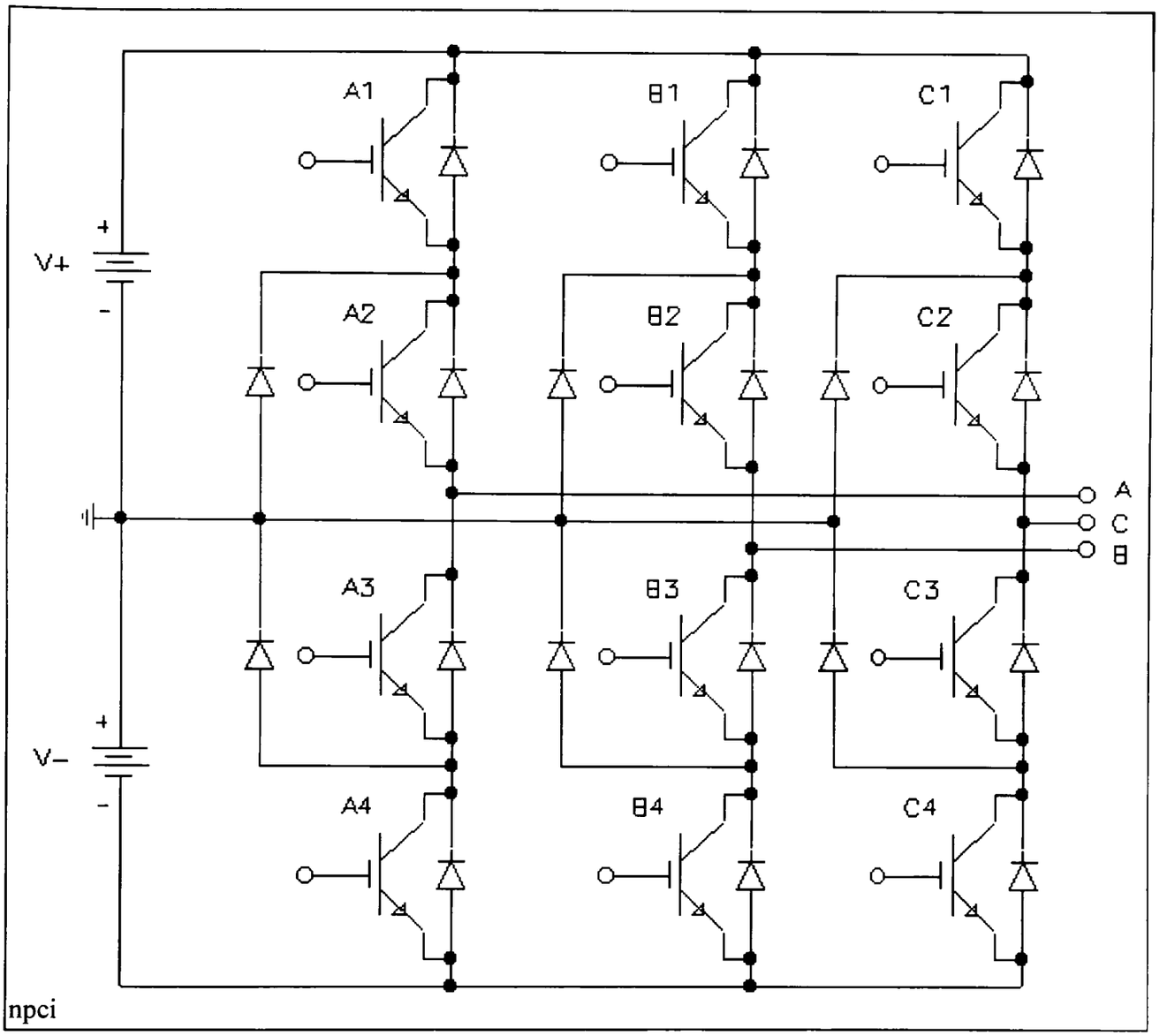
REFERENCES

1. S. Fukuda, K. Suzuki and Y. Iwaji, "Harmonic Evaluation of an NPC PWM Inverter Employing the Harmonic Distortion Determining Factor," Proceedings of the IEEE IAS Annual Meeting, October 1995, pp. 2417-2421.
2. Mohan, Undeland. Power Electronics: Applications and Design, John Wiley and Sons, New York, 1989, pp. 104-112.
3. SKHI 60 Data Sheet, Semikron Inc., 11 Executive Drive, P.O. Box 66, Hudson, NH 03051.
4. S. Upchurch, "Bus Bars Improve Power Module Interconnections", Power Conversion & Intelligent Motion, April 1995, p.18..25.

APPENDIX

Mathcad DOCUMENT FOR NPCI CODE GENERATION

NPC _ Pulse Width Modulation (SPWM):



Neutral Point Clamped Inverter Topology

Definition of Signum Function:

$$Sgn(x) = \begin{cases} 1 & \text{if } x>0 \\ -1 & \text{if } x<0 \\ 0 & \text{otherwise} \end{cases}$$

Number of Modulation Ratios: $I_o \equiv 16$

Amplitude Modulation Ratios: $k_{A_i} = \frac{i}{I_o}$

Frequency Modulation Ratio: $k_f \equiv 57$

$k_f \cdot 60 \cdot Hz = 3420 \cdot Hz$

Number of Points in Period: $N_o \equiv 1024$

EPROM Size in kbits: $I_o \cdot N_o \cdot 8 \cdot 1024^{-1} = 128$

Triangle function: $Tri(N) := \frac{2}{\pi} \cdot \asin\left(\sin\left(k_f \frac{N}{N_o} \cdot 2 \cdot \pi\right)\right)$

Reference Sinusoid for Phase a: $Ph_A(i,N) := \frac{i}{I_o} \cdot \sin\left(\frac{N}{N_o} \cdot 2 \cdot \pi\right)$

Reference Sinusoid for Phase b: $Ph_B(i,N) := \frac{i}{I_o} \cdot \sin\left(\frac{N}{N_o} \cdot 2 \cdot \pi - 120 \cdot deg\right)$

Reference Sinusoid for Phase c: $Ph_C(i,N) := \frac{i}{I_o} \cdot \sin\left(\frac{N}{N_o} \cdot 2 \cdot \pi - 120 \cdot deg\right)$

NPC Switching Function, Phase A:

$Sw_A(i,N) := if\left(|Ph_A(i,N)| > Tri(N), Sgn\left(Ph_A(i,N)\right), 0\right)$

NPC Switching Function, Phase B:

$Sw_B(i,N) := if\left(|Ph_B(i,N)| > Tri(N), Sgn\left(Ph_B(i,N)\right), 0\right)$

NPC Switching Function, Phase C:

$Sw_C(i,N) := if\left(|Ph_C(i,N)| > Tri(N), Sgn\left(Ph_C(i,N)\right), 0\right)$

*** BIT# 7 is upper IGBT Phase A **** $Bit_{Auh}(i,N) := if\left(Sw_A(i,N) > 0, 2^7, 0\right)$

*** BIT# 6 is upper IGBT Phase B **** $Bit_{Aul}(i,N) := if\left(Sw_A(i,N) > -1, 2^7, 0\right)$

*** BIT# 5 is upper IGBT Phase C **** $Bit_{Adl}(i,N) := if\left(Sw_A(i,N) < 1, 2^4, 0\right)$

*** BIT# 4 is lower IGBT Phase A **** $Bit_{Adh}(i,N) := if\left(Sw_A(i,N) < 0, 2^4, 0\right)$

*** BIT# 3 is lower IGBT Phase B **** $Bit_{Buh}(i,N) := if\left(Sw_B(i,N) > 0, 2^6, 0\right)$

*** BIT# 2 is lower IGBT Phase C **** $Bit_{Bul}(i,N) := if\left(Sw_B(i,N) > -1, 2^6, 0\right)$

*** BIT# 1 & BIT# 0 (LSB) not used**** $Bit_{Bdl}(i,N) := if\left(Sw_B(i,N) < 1, 2^3, 0\right)$

Index h(igh) means on the +/- bus. $Bit_{Bdh}(i,N) := if\left(Sw_B(i,N) < 0, 2^3, 0\right)$

Index l(ow) means on the ground bus. $Bit_{Cuh}(i,N) := if\left(Sw_C(i,N) > 0, 2^5, 0\right)$

Index u(p) means above ground bus. $Bit_{Cul}(i,N) := if\left(Sw_C(i,N) > -1, 2^5, 0\right)$

Index d(own) means below ground bus. $Bit_{Cdl}(i,N) := if\left(Sw_C(i,N) < 1, 2^2, 0\right)$

$Bit_{Cdh}(i,N) := if\left(Sw_C(i,N) < 0, 2^2, 0\right)$

$Byte_u(i,N) := Bit_{Auh}(i,N) + Bit_{Adl}(i,N) - Bit_{Buh}(i,N) + Bit_{Bdl}(i,N) + Bit_{Cuh}(i,N) - Bit_{Cdl}(i,N)$

$Byte_d(i,N) := Bit_{Aul}(i,N) + Bit_{Adh}(i,N) + Bit_{Bul}(i,N) - Bit_{Bdh}(i,N) + Bit_{Cul}(i,N) + Bit_{Cdh}(i,N)$

$N := 0 .. \left(N_o - 1\right)$

Number of Columns in Print File: $Cols \equiv 20h$ $Cols = 32$

Defining a function for Array Columns: $Col(x) := mod(x, Cols)$

Defining a function for Array Rows: $Row(x, y) := floor\left(\frac{(x-1)\cdot N_o}{Cols}\right) + floor\left(\frac{y}{Cols}\right)$

Build Bytes_13 Array for Print File:

$$Bytes\_13 := \left| \begin{array}{l} \text{for } i \in 1..I_o \\ \quad \text{for } n \in 0..N_o - 1 \\ \quad\quad Bytes_{Row(i,n),Col(n)} \leftarrow Byte_u(i,n) \\ Bytes \end{array} \right.$$

$cols(Bytes\_13) = 32$ $rows(Bytes\_13) = 512$

Build Bytes_24 Array for Print File:

$$Bytes\_24 := \left| \begin{array}{l} \text{for } i \in 1..I_o \\ \quad \text{for } n \in 0..N_o - 1 \\ \quad\quad Bytes_{Row(i,n),Col(n)} \leftarrow Byte_d(i,n) \\ Bytes \end{array} \right.$$

$cols(Bytes\_24) = 32$ $rows(Bytes\_24) = 512$

Set Column Width for Print File: $PRNCOLWIDTH := 4$

Print Bytes_13 Array to File: $WRITEPRN(NPC\_13) := Bytes\_13$

Print Bytes_24 Array to File: $WRITEPRN(NPC\_24) := Bytes\_24$

IGBT's Row 1 and 3 from the top (+) bus bar:

IGBT's Row 2 and 4 from the top (+) bus bar:

End Mathcad document for NPCI code generation

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