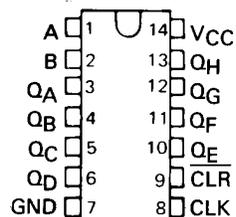


SN54164, SN54LS164, SN74164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

MARCH 1974 — REVISED MARCH 1988

- Gated Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

SN54164, SN54LS164 . . . J OR W PACKAGE
SN74164 . . . N PACKAGE
SN74LS164 . . . D OR N PACKAGE
(TOP VIEW)



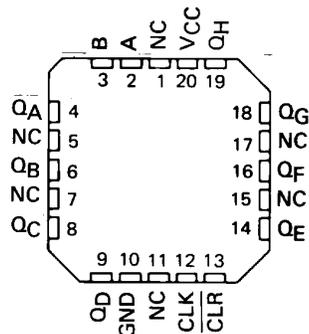
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'164	36 MHz	21 mW per bit
'LS164	36 MHz	10 mW per bit

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74164 and SN74LS164 are characterized for operation from 0°C to 70°C .

SN54LS164 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	QA	QB . . . QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

H = high level (steady state), L = low level (steady state)

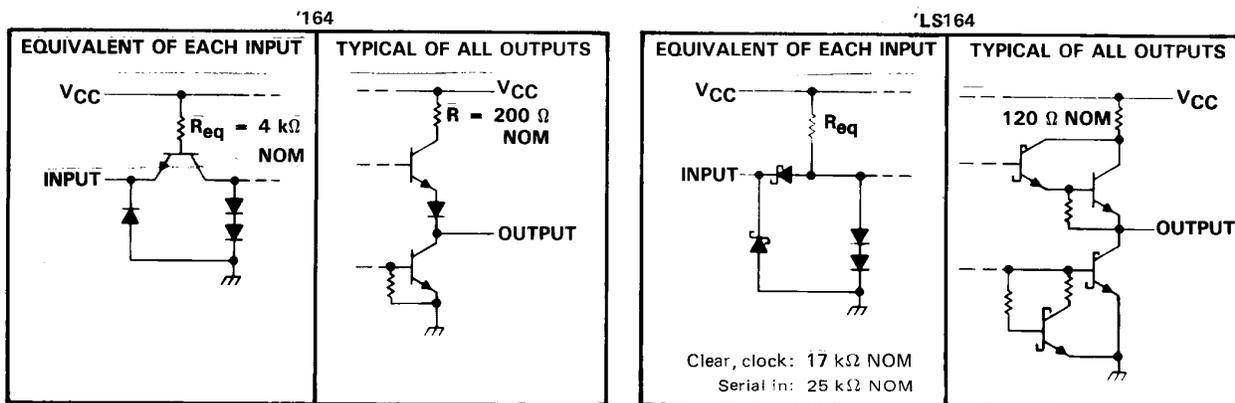
X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

QAn, QGn = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

schematics of inputs and outputs

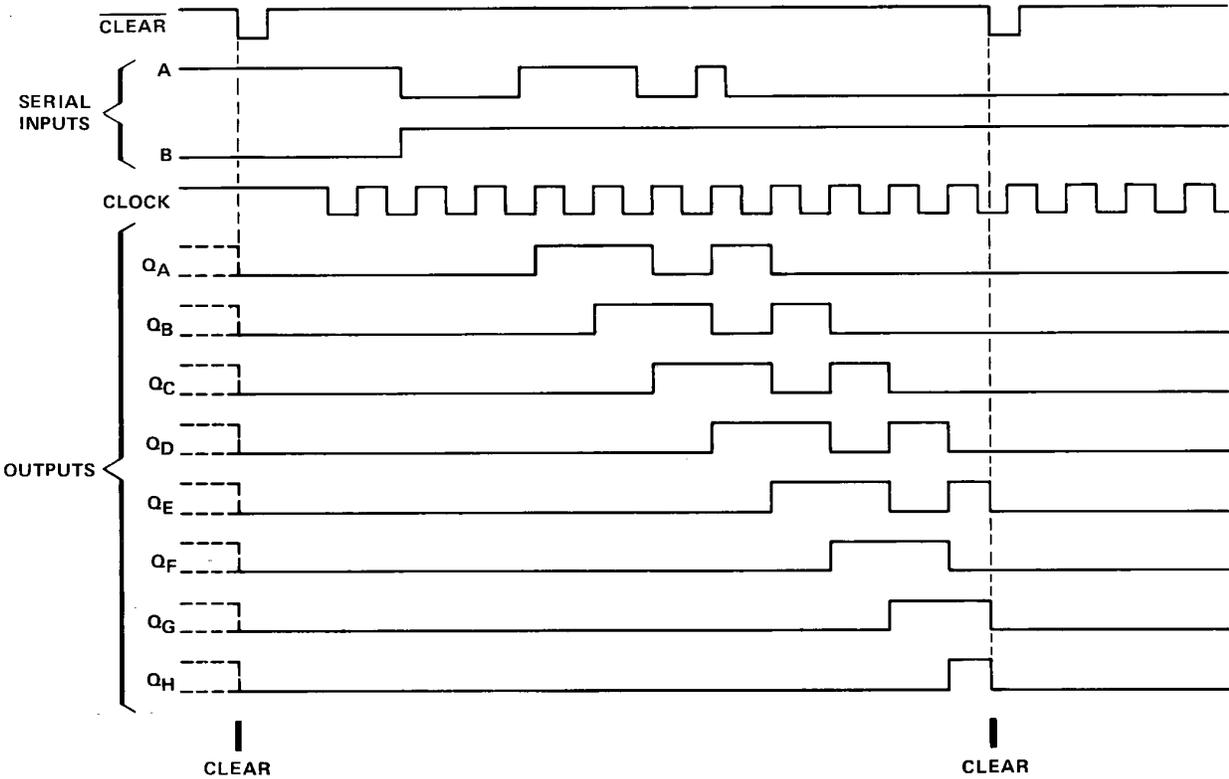


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TTL Devices

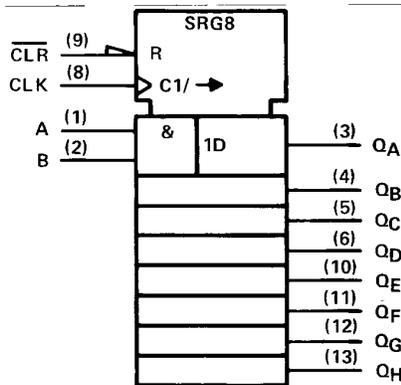
SN54164, SN54LS164, SN74164, SN74LS164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

typical clear, shift, and clear sequences



2
TTL Devices

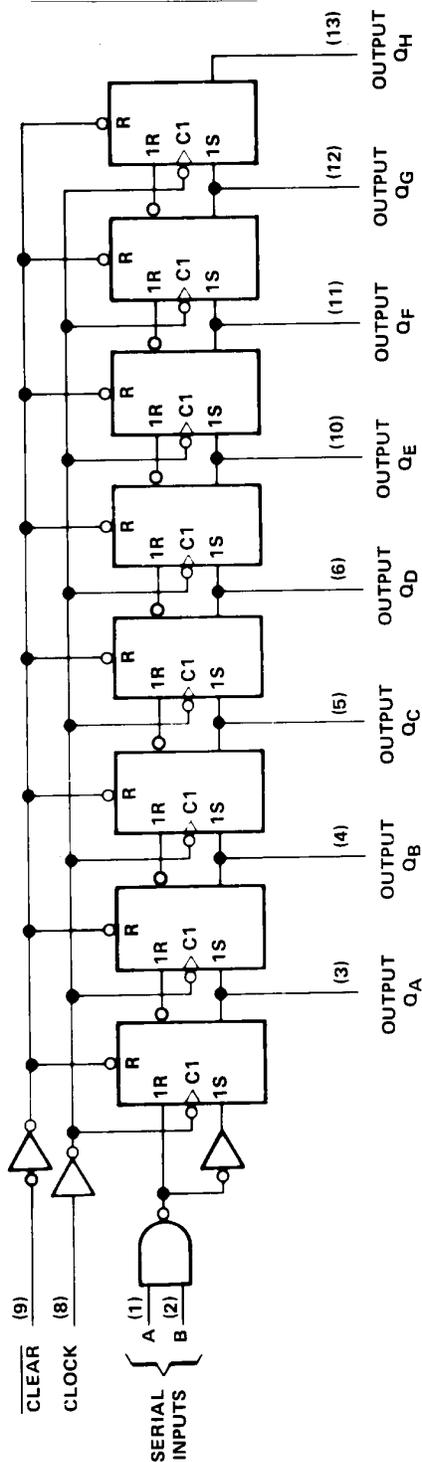
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

SN54164, SN54LS164, SN74164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

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TTL Devices