# Compensation For The LM3478 Boost Controller

The LM3478 is a low side N-Channel controller for switching regulators. Like many switching controllers, the added flexibility in component selection can cause problems for users when determining the compensation scheme. It is the goal of this paper to present a decent groundwork to allow the reader to select with confidence the correct compensation components. To achieve this we will look at the small signal models for the feedback loop to determine how each component interacts and eventually calculate the desired compensation.

The first question that is often asked is: Why is compensation necessary? Any DC-DC converter that regulates the output voltage utilizes negative feedback to ensure accuracy across line and load changes. An incorrect compensation scheme could lead to a phase reversal of the loop causing positive feedback and an erratic uncontrolled output. A minor problem that is typically encountered is an over or under-damped response of the output when a load transient is experienced. This is a sign that the loop stability could be optimized. Before compensation components can be selected and the response measured, the first step to undertake is to understand the operation of the controller and feedback loops. It is assumed that the reader is already familiar with the basic operation of the switcher covered in the LM3478 datasheet. Examining the block diagram of the LM3478 boost regulator in *Figure 1*, it can be clearly seen that two feedback loops exist. This is a unique feature that is indicative of a current mode control switching regulator. The first loop is the output voltage loop created by VOUT passing through the resistor divider into an error amplifier. The output of the error amplifier is referred to as the control voltage, VC, which is one of the two inputs to the PWM comparator.

The other input to the comparator is the second feedback loop. With current mode control architecture the switch current is sensed and is used to determine, in conjunction with the control voltage, when the FET should be turned off. To achieve this the switch current is measured across the external sense resistor before being summed with an internal ramp. The slope compensation ramp is present to prevent a large signal stability issue that is inherent in current mode control. While this ramp voltage is included in our small signal models, its requirement and adjustment will not be discussed here. For more information about the slope compensation please consult the LM3478 datasheet.
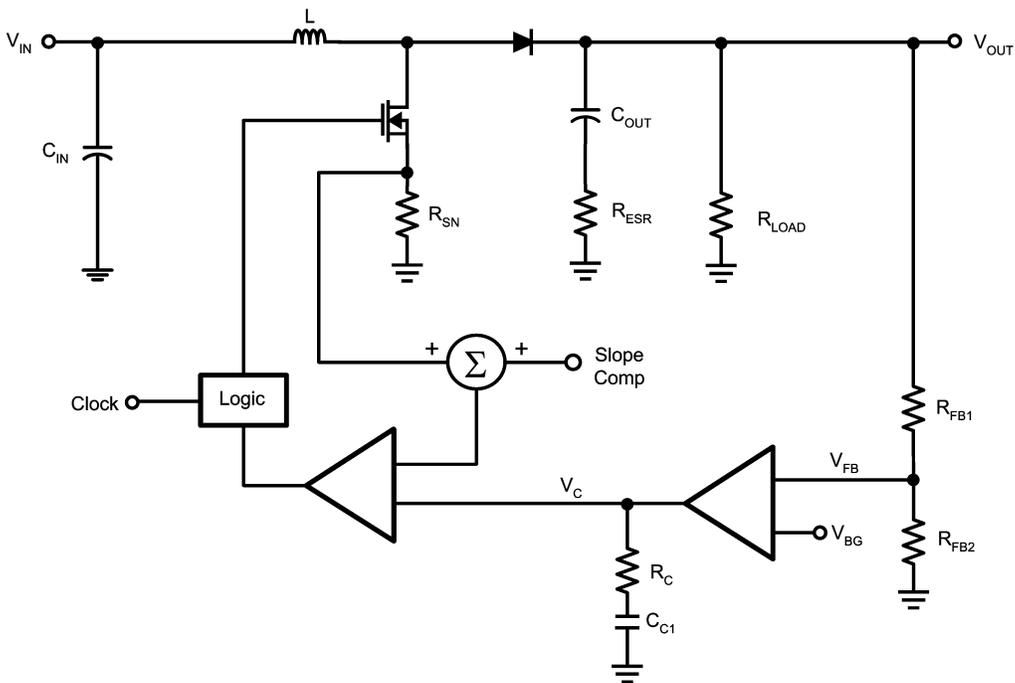
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FIGURE 1. Overview of LM3478 Current Mode Control Boost Regulator

Figure 1 shows the overall block diagram of the LM3478 with its application circuit. The next step is to derive the small signal equation for the entire loop. To simplify the analysis the loop can be effectively divided into three separate parts.

The first transfer function that will be examined is the control voltage, VC, to the output voltage, V_{OUT}. This takes into account the effects of the current loop, switch, and the output filter stage such as the inductor and output capacitor.

The equation can be written as:

$$T = A_{DC} \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 - \dfrac{s}{\omega_{z2}}\right)}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{Q\left(\dfrac{\omega_s}{2}\right)} + \dfrac{s^2}{\left(\dfrac{\omega_s}{2}\right)^2}\right)}$$

At first inspection the equation consists of two zeros, one of which is in the right half plane, a single pole and a complex pole pair. The DC gain of the system is written ACM and can be calculated by the equation below:

$$A_{CM} = \frac{(D'(\omega_c L_e \parallel R_{LOAD} \parallel R_{LOAD})}{R_{SN}}$$

where,

$$\omega_c L_e = \frac{\omega_s L}{D'^3 \pi n}$$

and,

$$n = 1 + \frac{2 \times S_e}{S_n}$$

and

$$S_e = \frac{V_{SL} \times f_s}{R_{SN}}$$

and,

$$S_n = \frac{V_{IN}}{L}$$

This is a rather long formula that incorporates the slope compensation and the inductor into the equation. It has been provided for completeness, however in this analysis the equation has been reduced to a simpler and more manageable form. You will find this simplification works extremely well and no real noticeable difference will be seen in the analysis. Therefore for all LM3478 compensation calculations this equation should be used:

$$A_{cm} = \frac{D' R_{LOAD}}{2 R_{SN}}$$

The next step is to calculate the two zeros that were found in the control to output equation. The first zero is created by the output capacitor and its associated equivalent series resistance:

$$\omega_{z1} = \frac{1}{C_{OUT} R_{ESR}}$$

The second zero is actually a right half plane zero. When examining its response on a bode plot it has the effect of increasing the gain by 20dB/decade like a left hand plane zero, but causing a 90 degree drop in phase like a pole. Its occurrence can be related to the application circuit by thinking of the response of the output voltage. If the output voltage starts dropping the switch will turn on to increase the current through the inductor. This causes the output voltage to drop even lower since the output current is provided solely by the output capacitor during this time. It is this effect that can be thought of as the source of the right half plane zero, which explains why it does not occur in a buck converter.

$$\omega_{z2} = \frac{R_{LOAD} \left(\dfrac{V_{IN}}{V_{OUT}}\right)^2}{L}$$

Looking at the denominator of the equation the poles can be calculated. The first pole is from the output capacitor and the load resistance and can be expressed as:

$$\omega_{p1} = \frac{1}{C_{OUT} R_{LOAD}}$$

The complex pole pair occurs at half the switching frequency and will be simply attributed to sampling theory for the sake of length in this application note. A Q factor also appears that can be calculated based on the inductor current slopes and duty-cycle:

$$\omega_s = 2 \times \pi \times f_s$$

$$Q = \frac{1}{\pi \left(D' \dfrac{S_e}{S_n} + \frac{1}{2} - D\right)}$$

Error Amplifier

This completes the equation of the control to output transfer function. The second stage that needs to be analyzed is the error amplifier. Of particular interest, we will derive the transfer function from the feedback pin to the control voltage. To achieve this the error amplifier block diagram has been converted to a small signal model.

Error Amplifier (Continued)

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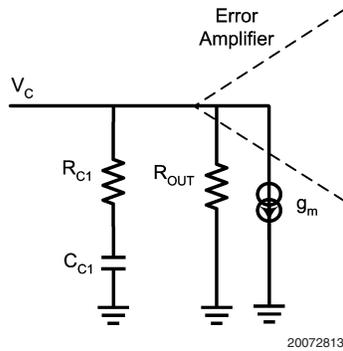
As can be seen the LM3478 uses a gm amplifier for the error amplifier. With this model the equation can be written by inspection as:

$$A_{comp} = A_{EA} = \frac{\left(1 + \dfrac{s}{\omega_{z3}}\right)}{\left(1 + \dfrac{s}{\omega_{p2}}\right)}$$

The DC gain of the system AEA is simply the output conductance multiplied by the output resistance of the amplifier. These values can be found in the electrical characteristics table of the datasheet.

$A_{EA} = g_m R_{OUT}$

The single zero is formed by the two external compensation components that are added at the COMP pin of the LM3478, the capacitor and resistor.

$$\omega_{z3} = \frac{1}{C_{C1} R_{C1}}$$

The error amplifier pole is formed by the combination of the output resistance of the error amplifier and the external compensation capacitor. An additional pole can be added with the introduction of another capacitor CC2 in parallel. However, for most power supplies this is not necessary.

$$\omega_{p2} = \frac{1}{C_{C1} R_{OUT}}$$

The last transfer function that needs to be derived in the loop is from the output voltage, VOUT, to the feedback pin. This can be calculated by inspection and is simply a voltage divider, caused by the feedback resistors. This can be written as a combination of the resistors or the output voltage and feedback voltage for convenience

$$A_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = \frac{V_{FB}}{V_{OUT}}$$

Total Loop Gain

Now that the transfer function for the separate circuits has been calculated the loop gain can be calculated by multiplication of these functions. We can then express the total loop gain as T:

$$T = A_{DC} \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 - \dfrac{s}{\omega_{z2}}\right)\left(1 + \dfrac{s}{\omega_{z3}}\right)}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)\left(1 + \dfrac{s}{Q\left(\dfrac{\omega_s}{2}\right)} + \dfrac{s^2}{\left(\dfrac{\omega_s}{2}\right)^2}\right)}$$

The DC gain of the system is also a result of the product of DC terms in the three transfer functions and can be calculated by the equation below:

$A_{DC} = A_{CM} A_{EA} A_{FB}$

Stability

Now that the loop gain, T, has been defined from the application parameters it is possible to use this to determine system stability and hence calculate the correct compensation components. To calculate the stability we will use a simple procedure invoking the Nyquist Stability Theorem. A special case of this theorem states that the stability of a system can be determined by analysis of the phase margin. To calculate the phase margin the crossover frequency, fc, first needs to be determined. This is defined as the frequency where the magnitude of the loop (|T|) is unity, equal to 0 dB. The phase of the loop gain, T, can then be calculated at this frequency and the difference between it and 180 degrees is the phase margin. Expressing it as an equation:

$||T(\omega = 2 \times \pi \times f_c|| = 1 = 0dB$

$\Phi_m = 180° + angleT\ (\omega = 2 \times \pi \times f_c)$

To design for an exact phase margin we need to know the desirable range for which our switching regulator should reside. If phase margin is less than or equal to 0 degrees the system will be unstable. Therefore a positive number is always required. But increasing the phase margin excessively causes the system to become over-damped, while a lower phase margin will create an under-damped response. For the sake of simplicity it will be stated that a good value for the LM3478 phase margin is in the range of 30 to 100 degrees.

Putting It Together

Now that the system has been modeled and the desired stability understood the compensation section can be designed. This is usually the last stage completed after the inductor and output capacitor selection. However, it might be prudent to revise these values if a better compensation scheme could be obtained. For instance, the output capacitor could be increased to bring in a pole to adjust the phase margin for improved settling on transient response.

To start selecting the compensation components it is good practice to have an idea where the crossover frequency should occur. With a boost converter like the LM3478 the right half plane zero causes severe difficulty with the loop

Putting It Together   (Continued)

response. Therefore, it is best to locate the crossover frequency one decade before this RHP zero occurs. If there is ever a choice between crossover frequencies it is best to choose the higher frequency.

Once the known equations have been calculated, the easiest way to set the compensation components is to use algebra on the graph technique for drawing bode plots. This allows the user to graphically place the pole and zero combinations to create the best response possible.

Design Example

To illustrate how to set the compensation for the LM3478 an example circuit will be used.

Conditions:

  Vin = 5V

  Vout = 12V

  Iload = 1.5A

  Fs = 400KHz

Components:

  L = 3.3uH

  Cout = 150uF

  ESR = 50mOhm

Calculations:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} = \frac{12 - 5}{1.5} = 0.58$$

Duty-Cycle:

$$R_{LOAD} = \frac{V_{OUT}}{I_{LOAD}} = \frac{12}{1.5} = 8\Omega$$

D' = 1 - D = 1 - 0.58 = 0.42

Control to Output Transfer Function

$$A_{cm} = \frac{D'R_{LOAD}}{2R_{SN}} = \frac{0.42 \times 8}{2 \times 0.01} = 167 \text{ V/V}$$

$$\omega_{z1} = \frac{1}{C_{OUT}R_{ESR}} = \frac{1}{150\mu F \times 0.05\Omega} = 133,333 \text{ rad/sec}$$

$$\omega_{z2} = \frac{R_{LOAD}\left(\dfrac{V_{IN}}{V_{OUT}}\right)^2}{L} = \frac{8\left(\dfrac{5}{12}\right)^2}{3.3\mu H} = 420,875 \text{ rad/sec}$$

$$\omega_{p1} = \frac{1}{C_{OUT}R_{LOAD}} = \frac{1}{150\mu F \times 8k\Omega} = 833 \text{ rad/sec}$$

$$Q = \frac{1}{\pi\left(D'\dfrac{S_e}{S_n} + \frac{1}{2} - D\right)} = \frac{1}{\pi\left(0.42\dfrac{S_e}{S_n} + 0.5 - 0.58\right)} = 0.38$$

where,

S_e = 3,320,000 A/Sec

S_e =1,515,151 A/Sec

Vout to Control Voltage:

$A_{EA} = g_m R_1 = 800\mu mho \times 50k\Omega = 38V/V$

$$A_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = \frac{V_{FB}}{V_{OUT}} = \frac{1.26}{12} = 0.105 \text{ V/V}$$

Therefore, the DC magnitude of the loop gain can be calculated:

$A_{DC} = A_{comp}A_{cm}A_{fb} = 167 \times 38 \times 0.105 = 665V/V$

$A_{DC} = 20\log_{10}(665) = 56.4dB$

Since the RHP zero occurs at ~67KHz (420,875 rad/sec) the cross-over frequency should be set approximately a decade lower or ~6KHz. A point to remember is that this zero will decrease with heavier loads and lower input voltages. Therefore, a worst case condition would be with the minimum input voltage and maximum load. If a 10% tolerance was expected on the input rail this would mean we should set the cross-over frequency below 5KHz.

Using algebra on the graph we can now create our first bode plot without the compensation poles and zeroes. For simplicity Q was assumed to be equal to 0.5, which means that an identical real pole pair would be located at half the switching frequency. This is a reasonable first pass approximation given that the value for Q was found to be 0.38

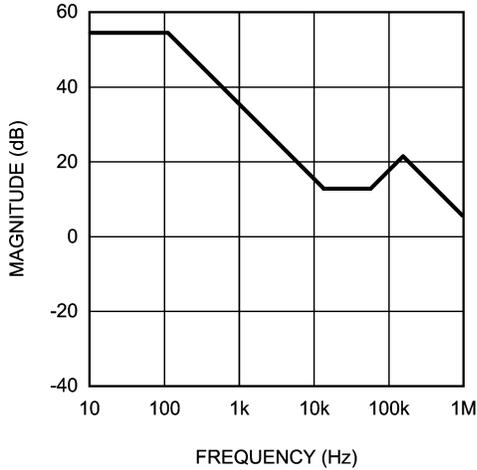# Putting It Together (Continued)

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FIGURE 2. Uncompensated Loop Gain

The next step is to calculate the exact placement of the compensation pole and zero to get the desired response. First, we will decide on the pole placement to get the cross-over frequency desired before using the zero to obtain the phase margin. Typically this process can undergo multiple revisions, including the power components.

Knowing that we want a cross-over frequency below 5KHz we can observe that the magnitude in the range of 1KHz - 5KHz is 25dB to 35dB. To ensure adequate roll-off the compensation pole was chosen to be ~30Hz which is 2 decades back from the middle of the range. This also corresponded to a capacitor of 0.1uF which is a commonly available size.

$$\omega_{p2} = \frac{1}{C_{C1}R_{OUT}} = \frac{1}{0.1\mu F \times 50k\Omega} = 31Hz$$

Updating the bode it can be seen that the magnitude is well below unity before the RHP zero occurs.
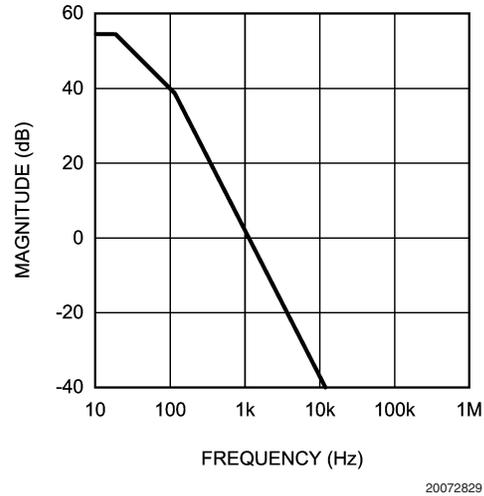

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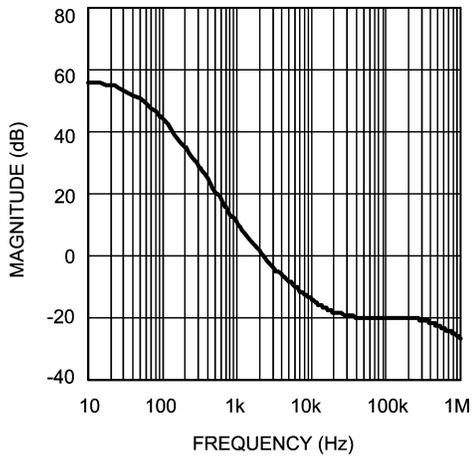**FIGURE 3. Loop Gain with Dominant Compensation Pole**

The last component necessary is the compensation resistor which sets a zero in the loop gain. It will be necessary to introduce this zero in the proximity of the cross-over frequency (~1KHz), because looking at the second bode plot the phase margin will be close to zero. This is because 2 poles have already occurred a decade before which introduces a phase change of 180 degrees. Therefore a zero in this location would correspond to approximately 45 degrees of phase margin. The bandwidth can also be increased safely as the gain is lower than −40dB before the next zero is introduced. Choosing a value of 1000 Ohms:

$$\omega_{z2} = \frac{1}{C_{C1}R_{C1}} = \frac{1}{0.1\mu F \times 1k\Omega} = 1,590Hz$$

Now that the values have been obtained a full bode plot generated from the derived equation can be plotted and modifications made if necessary. As can be seen the cross-over frequency is 2KHz with a phase margin of 60 degrees.
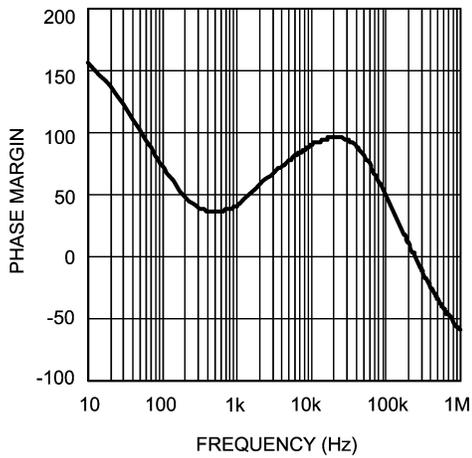
Putting It Together (Continued)

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Loop Gain Magnitude

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Phase Margin of Loop Gain

Overall this method represents a simple analysis that can be performed to design an effective compensation network. It should be remembered that variations in all the components will occur, therefore bench analysis should always be used to verify stability.

Notes

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