

VA30_HB

Schematics Document

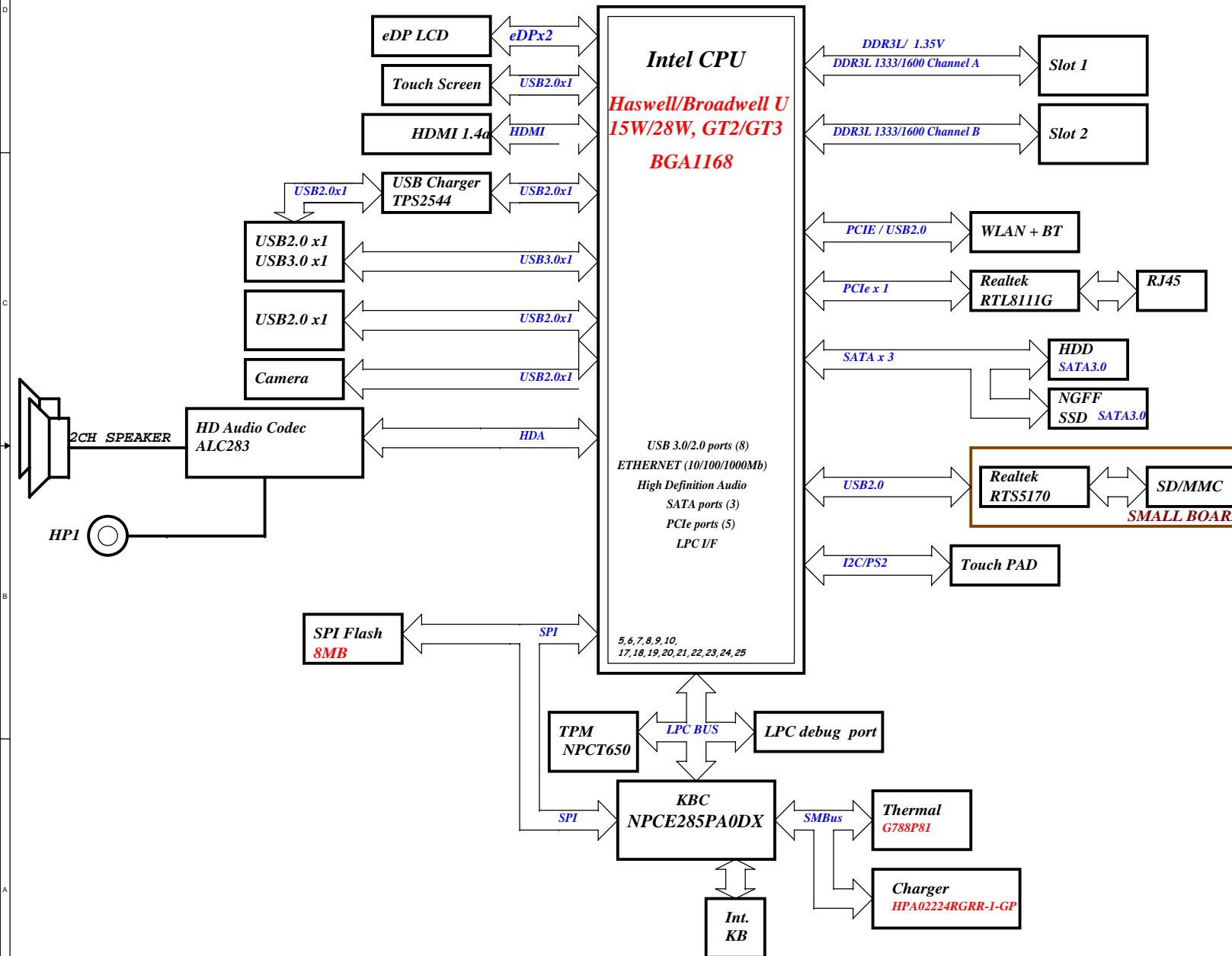
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Title			Cover Page		
Size	Document Number			Rev	
A3	MA30 HB ULT			2	
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VA30_HB Board Block Diagram

Project code : 91.40Q01.001
 PCB P/N : 13334
 Revision : SA



CHARGER	
HPA02224	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_Charger 3D3V_s5
CPU DC/DC	
TPS51622 46-47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
NN30331 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
uP1740P 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_s3
SYSTEM DC/DC	
S-1339 51	
INPUTS	OUTPUTS
DCBATOUT	1D5V_s0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title: **Block Diagram**

Size: Custom Document Number: **VA30_HB_ULT** Rev: SA

Date: Tuesday, April 15, 2014 Sheet 2 of 102

SSID = CPU

5

4

3

2

1

D

D

C

C

B

B

A

A

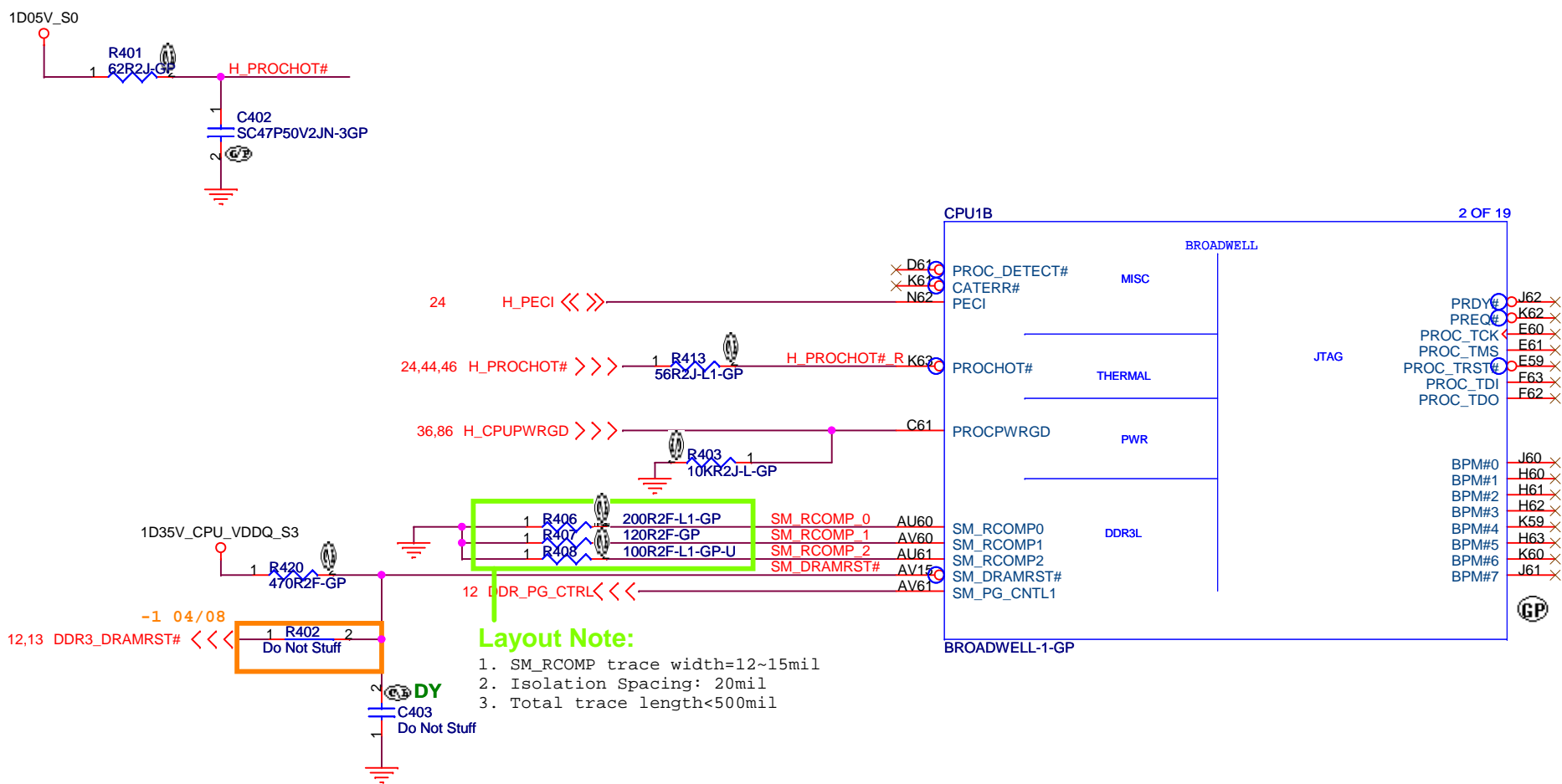
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Title			CPU (Reserved)		
Size	Document Number				Rev
A3	MA30 HB ULT				SA
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SSID = CPU

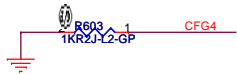


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Title CPU (THERMAL/CLOCK/PM)		
Size A4	Document Number MA30 HB ULT	Rev SA
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eDP Enable	
CFG4	1:Disable 0:Enable



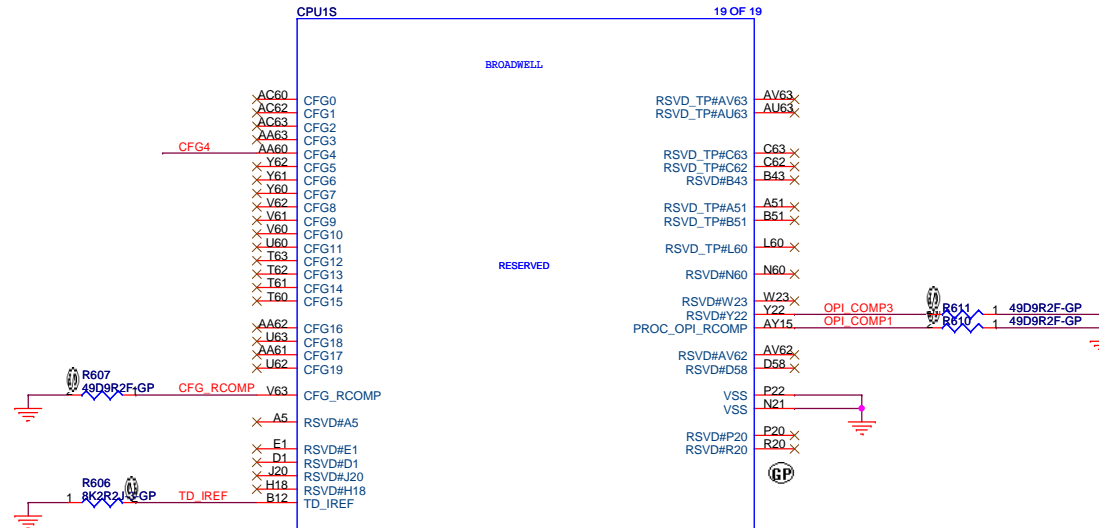
Signal Name	Description	Direction/Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none"> • CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — • CFG[4]: eDP enable <ul style="list-style-type: none"> — 1 = Disabled — 0 = Enabled • [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands. 	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

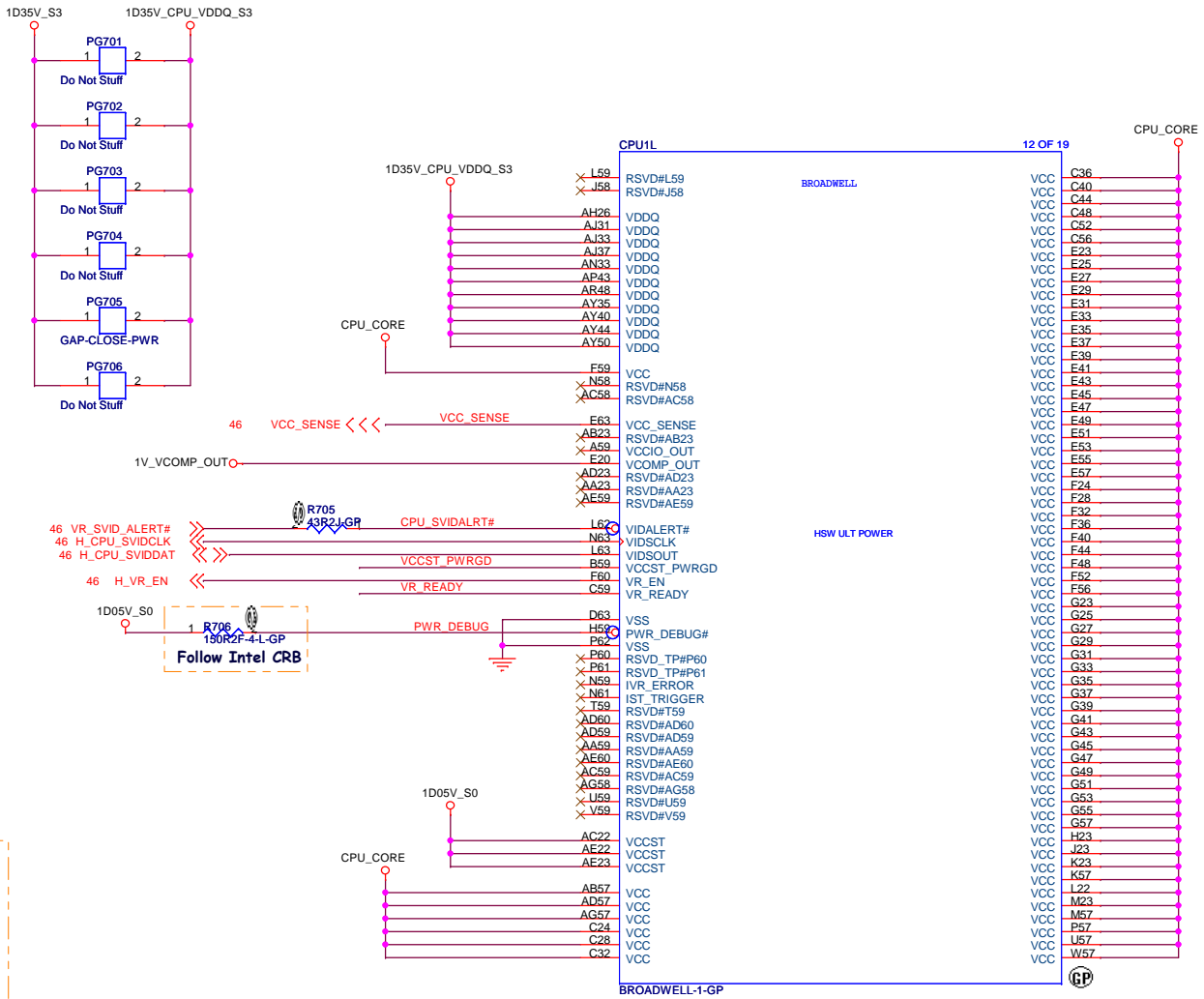
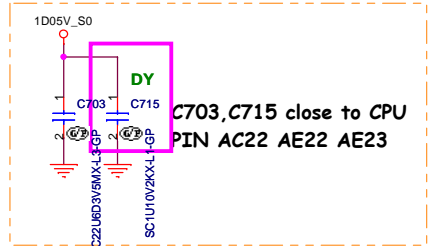
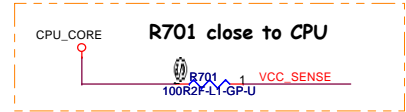
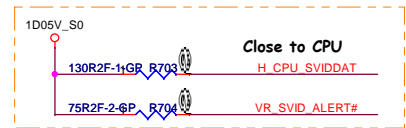


Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value
CFG[0]		Connect a series 1 KΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	Reserved. No connect.		
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0:Enabled - An external Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.	1
CFG[19:5]	Reserved configuration lands. A test point may be placed on the board for these lands.		

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File			
CPU (CFG)			
Size Custom	Document Number	Rev	
	MA30 HB ULT	2	
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SSID = CPU



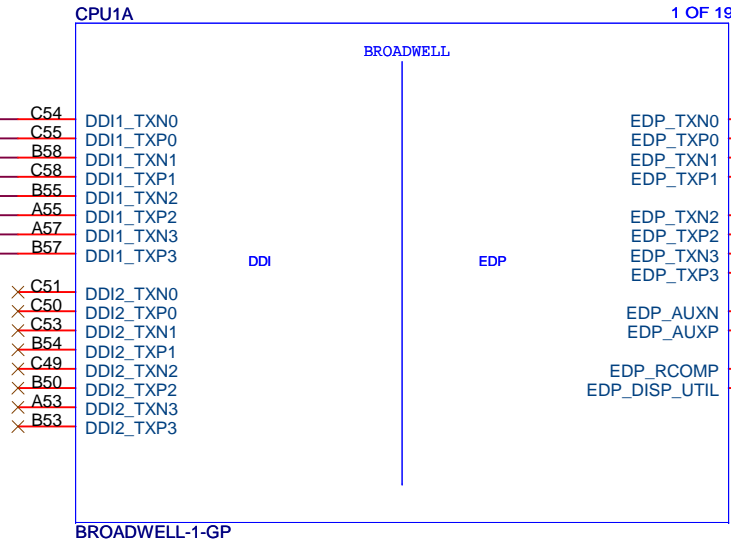
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CPU (VCC CORE)	
Title	Rev
Size A3	SA
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SSID = CPU

HDMI

54 HDMI_DATA_CPU_N2 <<<
 54 HDMI_DATA_CPU_P2 <<<
 54 HDMI_DATA_CPU_N1 <<<
 54 HDMI_DATA_CPU_P1 <<<
 54 HDMI_DATA_CPU_N0 <<<
 54 HDMI_DATA_CPU_P0 <<<
 54 HDMI_DATA_CPU_N3 <<<
 54 HDMI_DATA_CPU_P3 <<<



C45 EDP_TXN0
 B46 EDP_TXP0
 A47 EDP_TXN1
 B47 EDP_TXP1
 C47 EDP_TXN2
 C46 EDP_TXP2
 A49 EDP_TXN3
 B49 EDP_TXP3
 A45 EDP_AUXN
 B45 EDP_AUXP
 D20 EDP_RCOMP
 A43 EDP_DISP_UTIL

eDP



Layout Note:

Design Guideline:
 EDP_COMP keep routing length max 100 mils.
 Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Bit Rate	Supports (in # of lanes)	Peak Bandwidth
1.62 Gb/s	4	4 x 162 MB/s = 648 MB/s
5.4 Gb/s	4	4 x 540 MB/s = 2160 MB/s
2.7 Gb/s	4	4 x 270 MB/s = 1080 MB/s

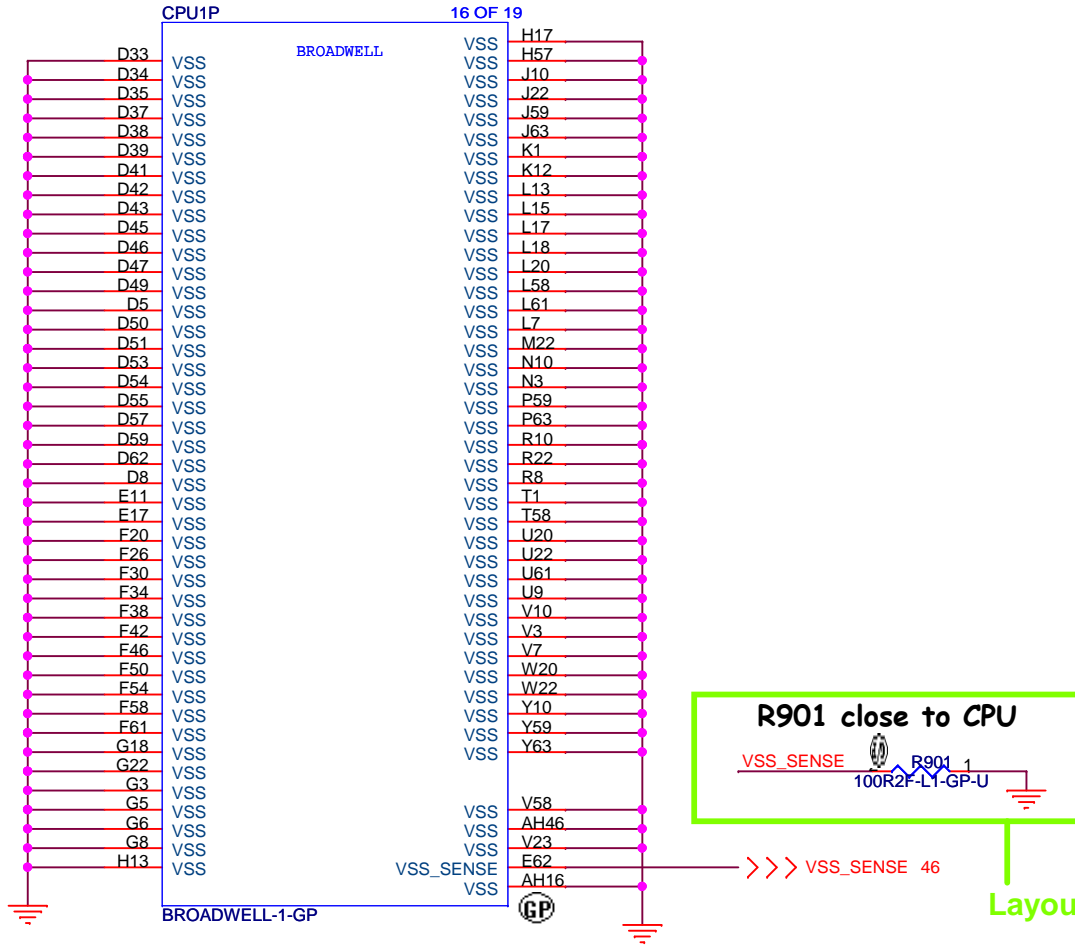
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Title: **CPU (DDI/EDP)**

Size A4	Document Number MA30 HW ULT	Rev SA
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SSID = CPU



Layout Note:

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Title

CPU (VSS)

Size
A4

Document Number

MA30 HB ULT

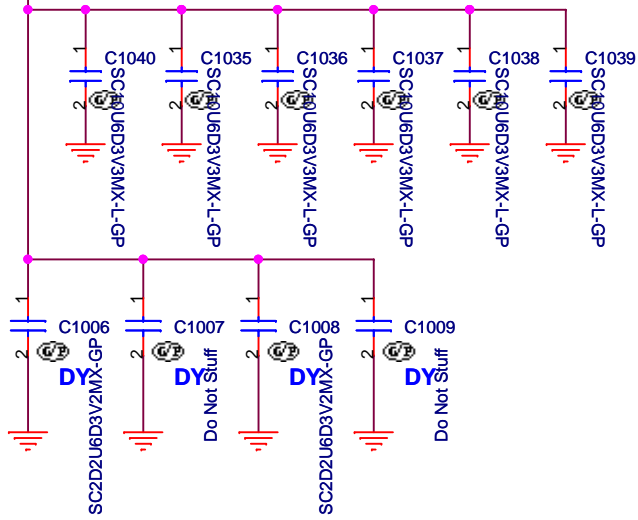
Rev
SA

Date: Tuesday, April 15, 2014

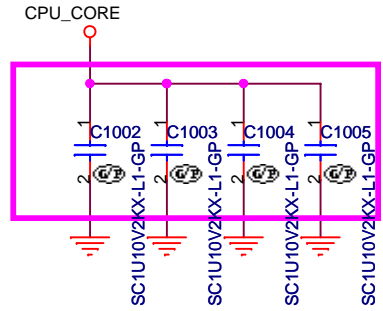
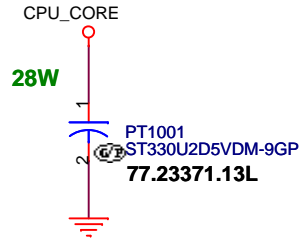
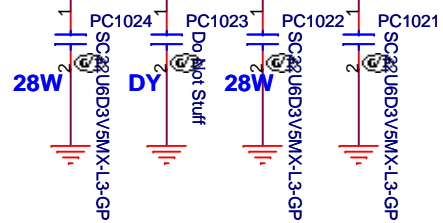
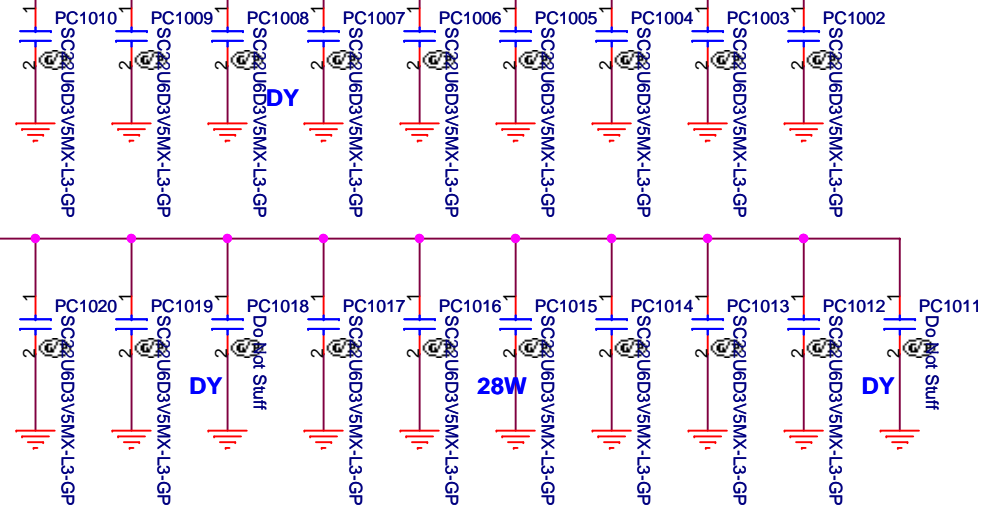
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1D35V_CPU_VDDQ_S3

CPU_CORE



For Intel Recommend EE Part



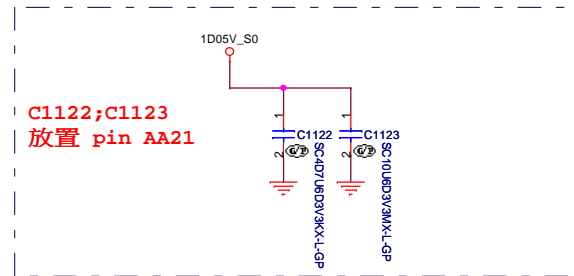
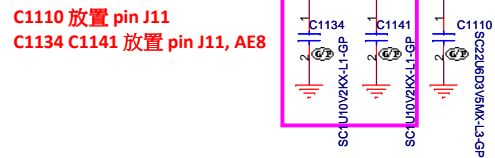
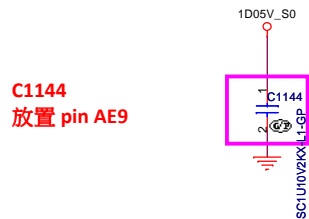
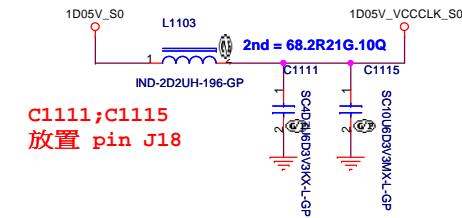
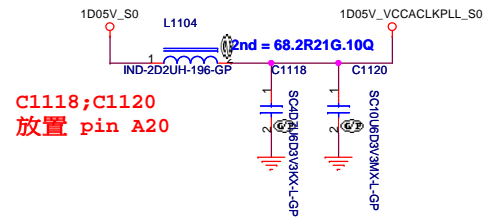
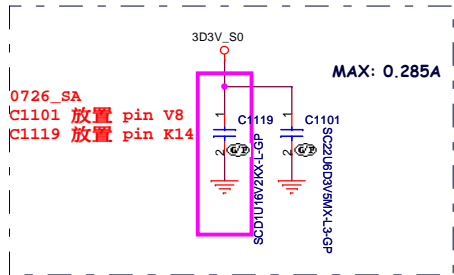
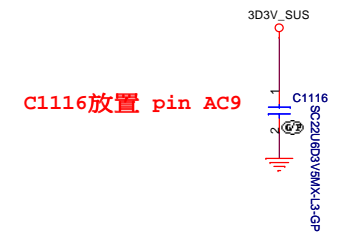
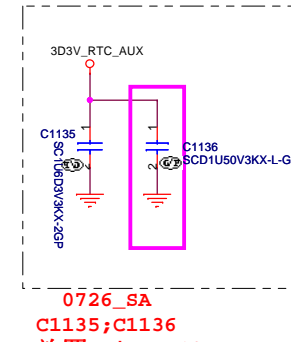
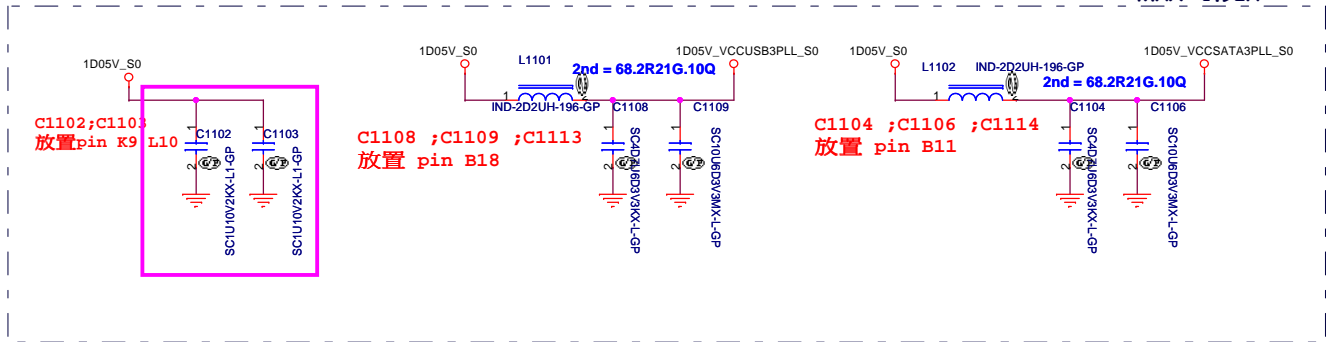
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Title			
CPU (Power CAP1)			
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0726_SA 擺放電容的位置請參考Page 21
每個位置如下



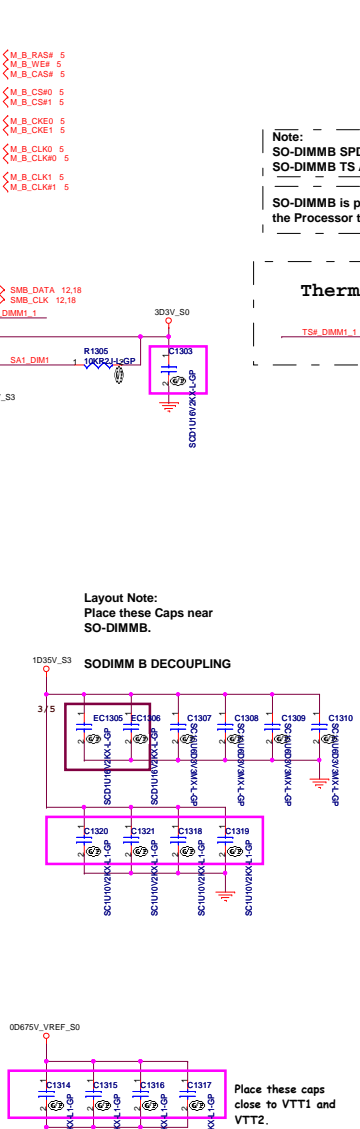
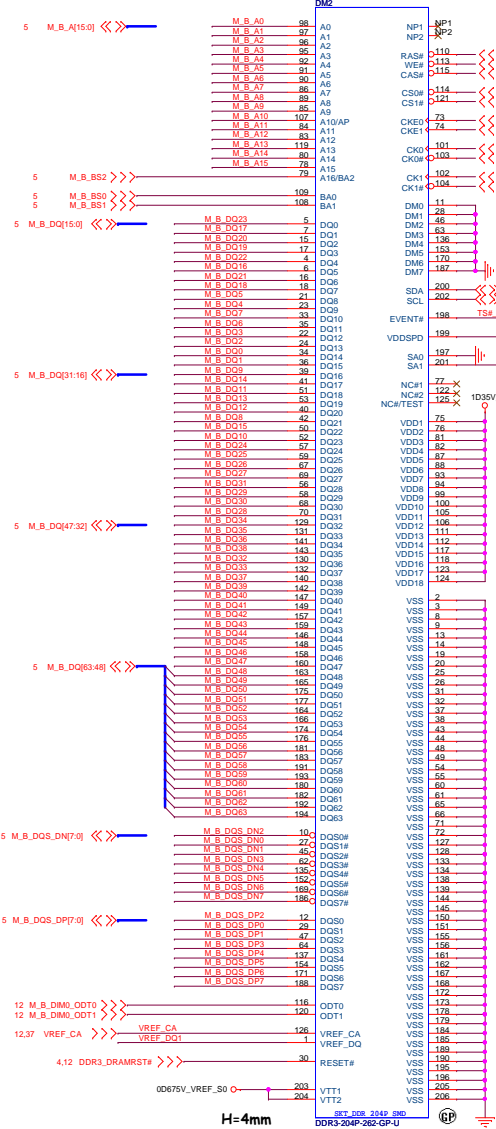
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Title CPU (Power CAP2)		
Size Custom	Document Number MA30 HB ULT	Rev 2
Date: Tuesday, April 15, 2014	Sheet 11	of 102

SSID = MEMORY

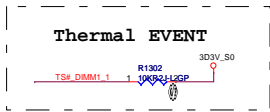
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	M_A_A1 97 A1	NP2	NP2
	M_A_A2 96 A2	RAS# 110	<<< M_A_RAS# 5
	M_A_A3 95 A3	WE# 113	<<< M_A_WE# 5
	M_A_A4 94 A4	CS# 116	<<< M_A_CS# 5
	M_A_A5 93 A5		
	M_A_A6 92 A6	CSW# 114	<<< M_A_CS# 5
	M_A_A7 91 A7	CS# 121	<<< M_A_CS# 5
	M_A_A8 90 A8	CKE0# 73	<<< M_A_CKE0 5
	M_A_A9 89 A9	CKE1# 74	<<< M_A_CKE1 5
	M_A_A10 88 A10	CK0# 101	<<< M_A_CLK0 5
	M_A_A11 87 A11	CK0# 103	<<< M_A_CLK#0 5
	M_A_A12 86 A12	CK1# 102	<<< M_A_CLK1 5
	M_A_A13 85 A13	CK1# 104	<<< M_A_CLK#1 5
	M_A_A14 84 A14		
	M_A_A15 83 A15		
	M_A_A16/BA2 82 A16/BA2		
5 M_A_BS2 >>>			
5 M_A_BS0 >>>			
5 M_A_BS1 >>>			
5 M_A_DQ[15:0] <<<	M_A_DQ0 5 DQ0	DM0 28	
	M_A_DQ1 6 DQ1	DM1 46	
	M_A_DQ2 7 DQ2	DM2 64	
	M_A_DQ3 8 DQ3	DM3 82	
	M_A_DQ4 9 DQ4	DM4 100	
	M_A_DQ5 10 DQ5	DM5 118	
	M_A_DQ6 11 DQ6	DM6 136	
	M_A_DQ7 12 DQ7	DM7 154	
	M_A_DQ8 13 DQ8		
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SSID = MEMORY

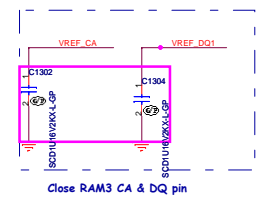
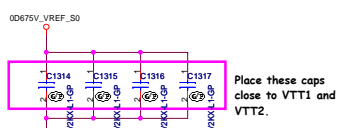
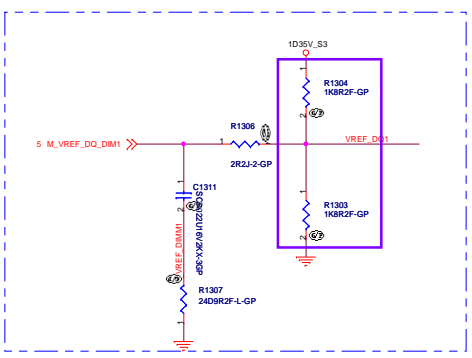
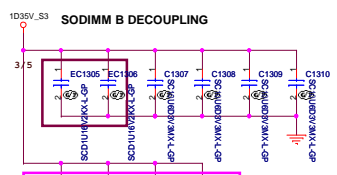


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near SO-DIMMB.



H=4mm
4th = 62.10017.I31
2nd = 62.10024.M31
62.10024.S21
3rd = 62.10024.Q61

5

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Title			
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Size	Document Number		Rev
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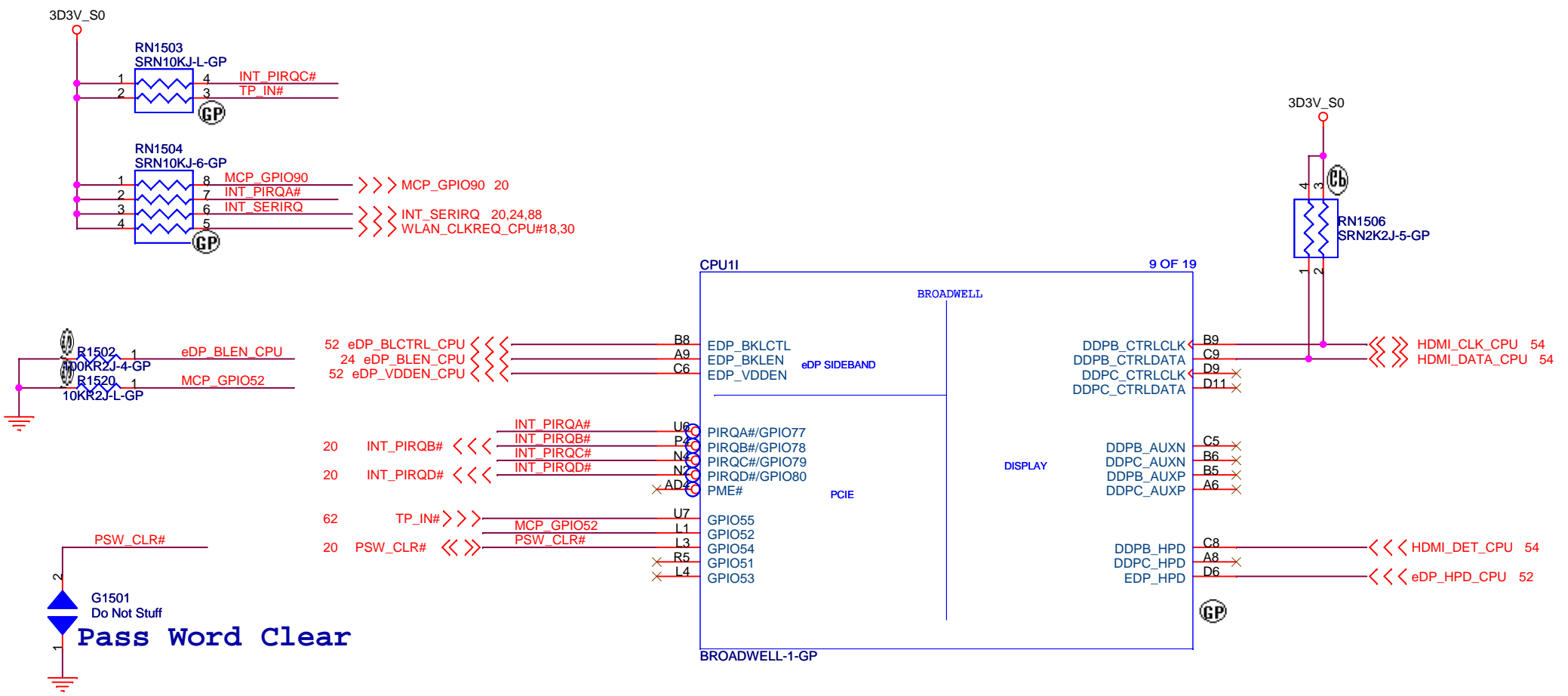
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1

SSID = CPU



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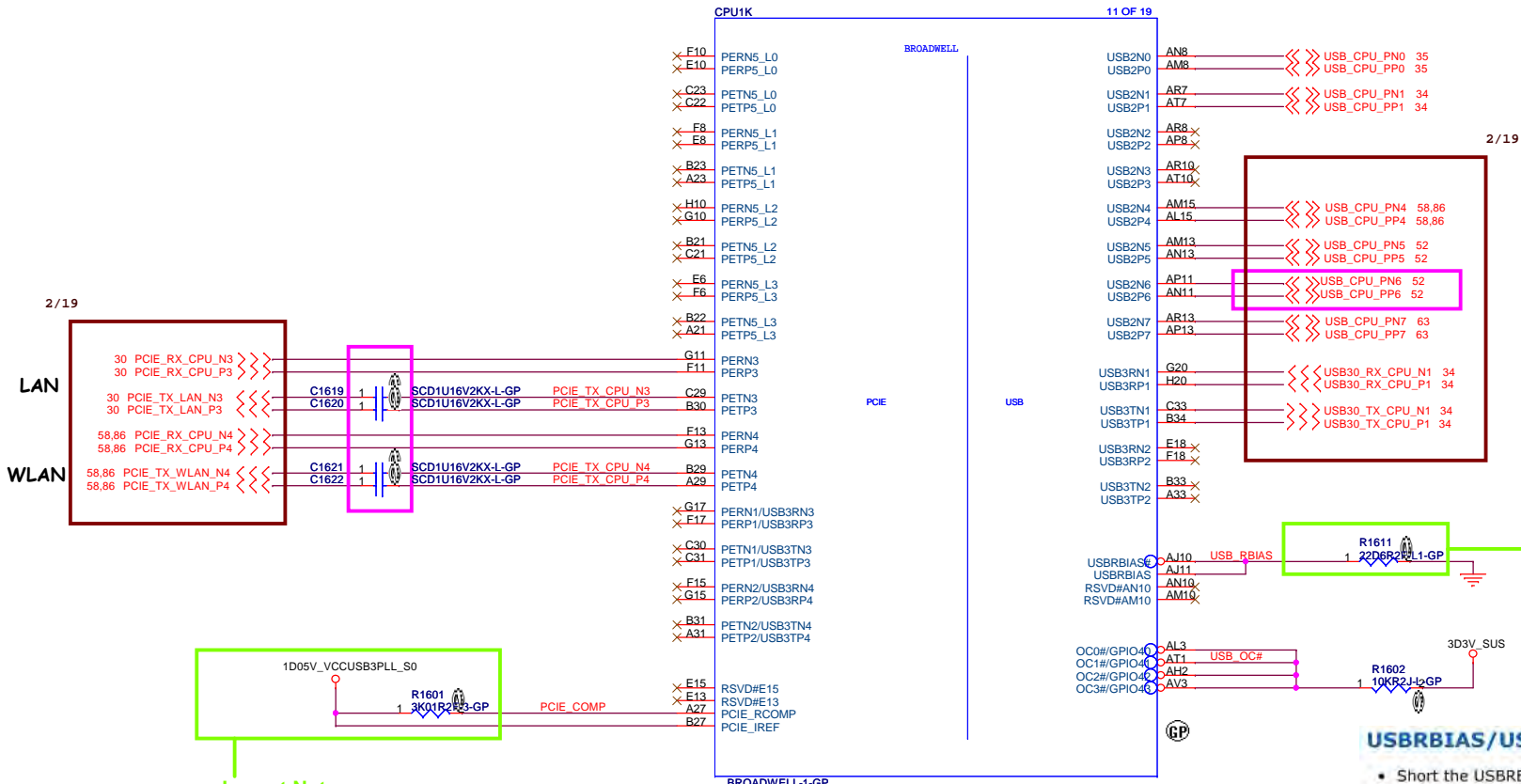
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Title CPU(EDP SIDE BAND/GPIO/DDI)		
Size A4	Document Number MA30 HB ULT	Rev 2
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SSID = PCH

USB Table

Pair	Device
0	USB2.0 Port 1
1	USB3.0 Port 2(USB2.0)
2	
3	
4	WLAN(Bluetooth)
5	Touch screen
6	CCD
7	Card reader



Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

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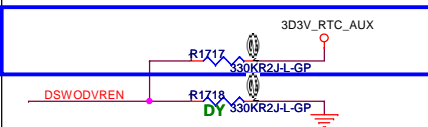
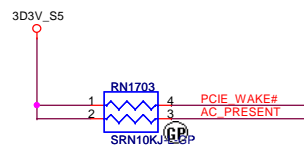
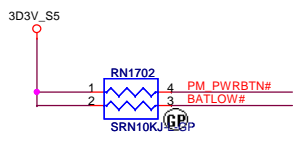
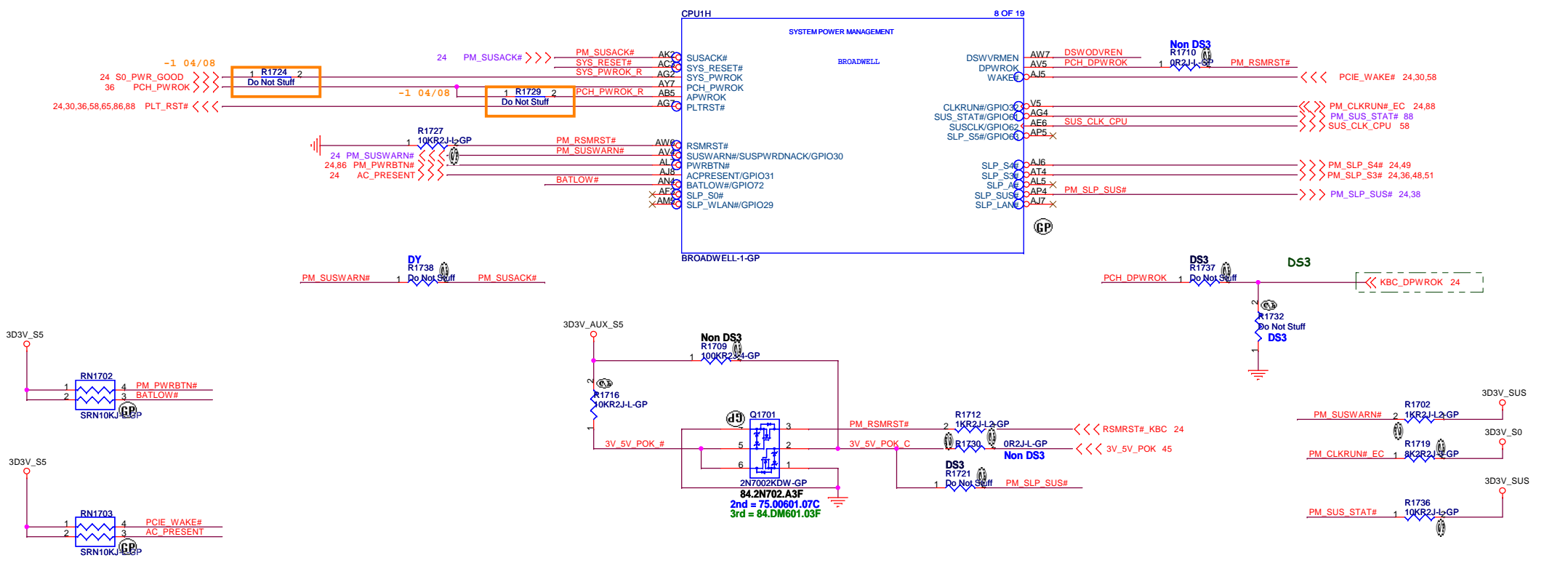
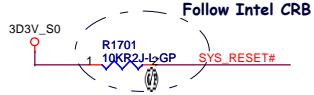
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Title		CPU (PCI/USB)	
Size	Document Number	Rev	
A3	MA30 HB ULT	2	
Date:	Tuesday, April 15, 2014	Sheet	16 of 102

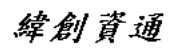
SSID = PCH

Bit	Description
31:3	Reserved
2	<p>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0':</p> <ul style="list-style-type: none"> Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. <p>NOTE: Deep Sx disabled configuration must leave this bit at '0'.</p>

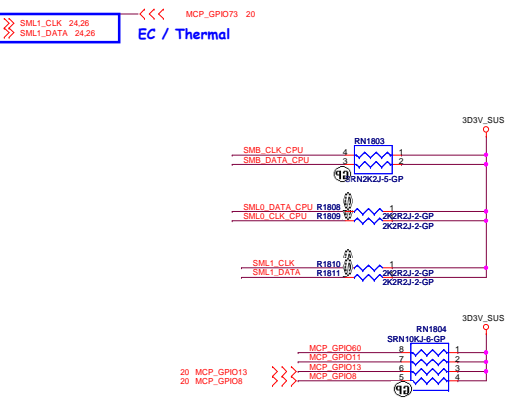
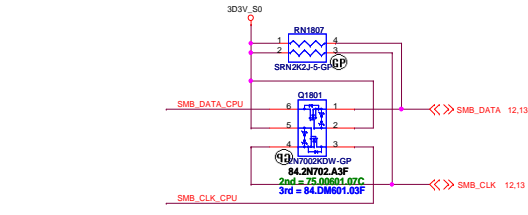
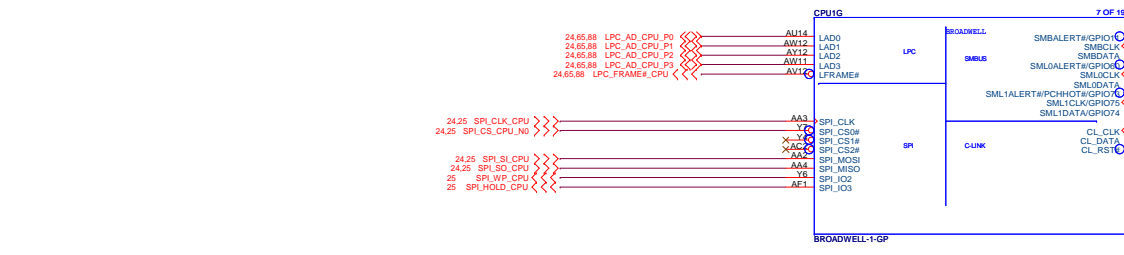
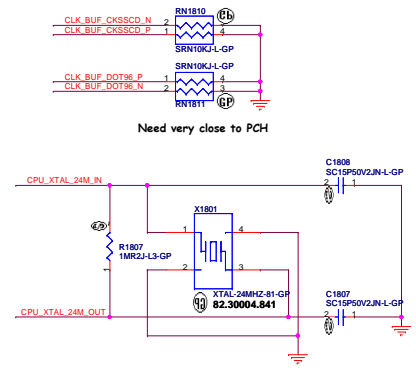
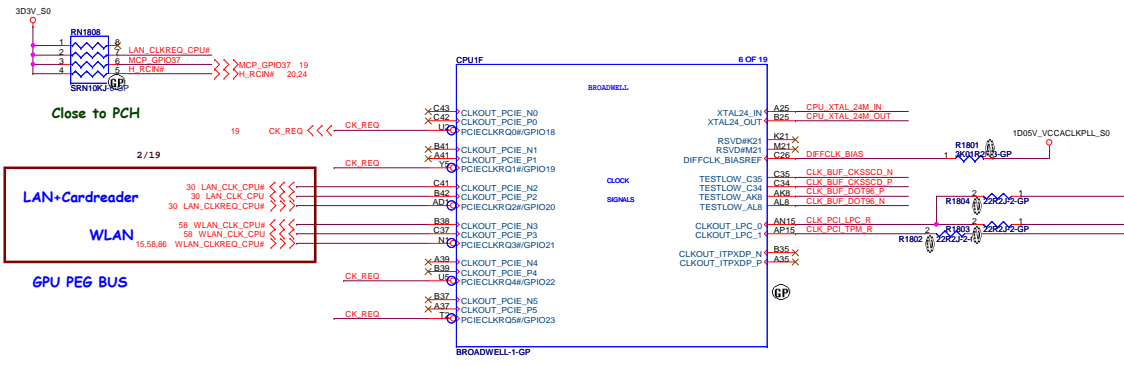
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

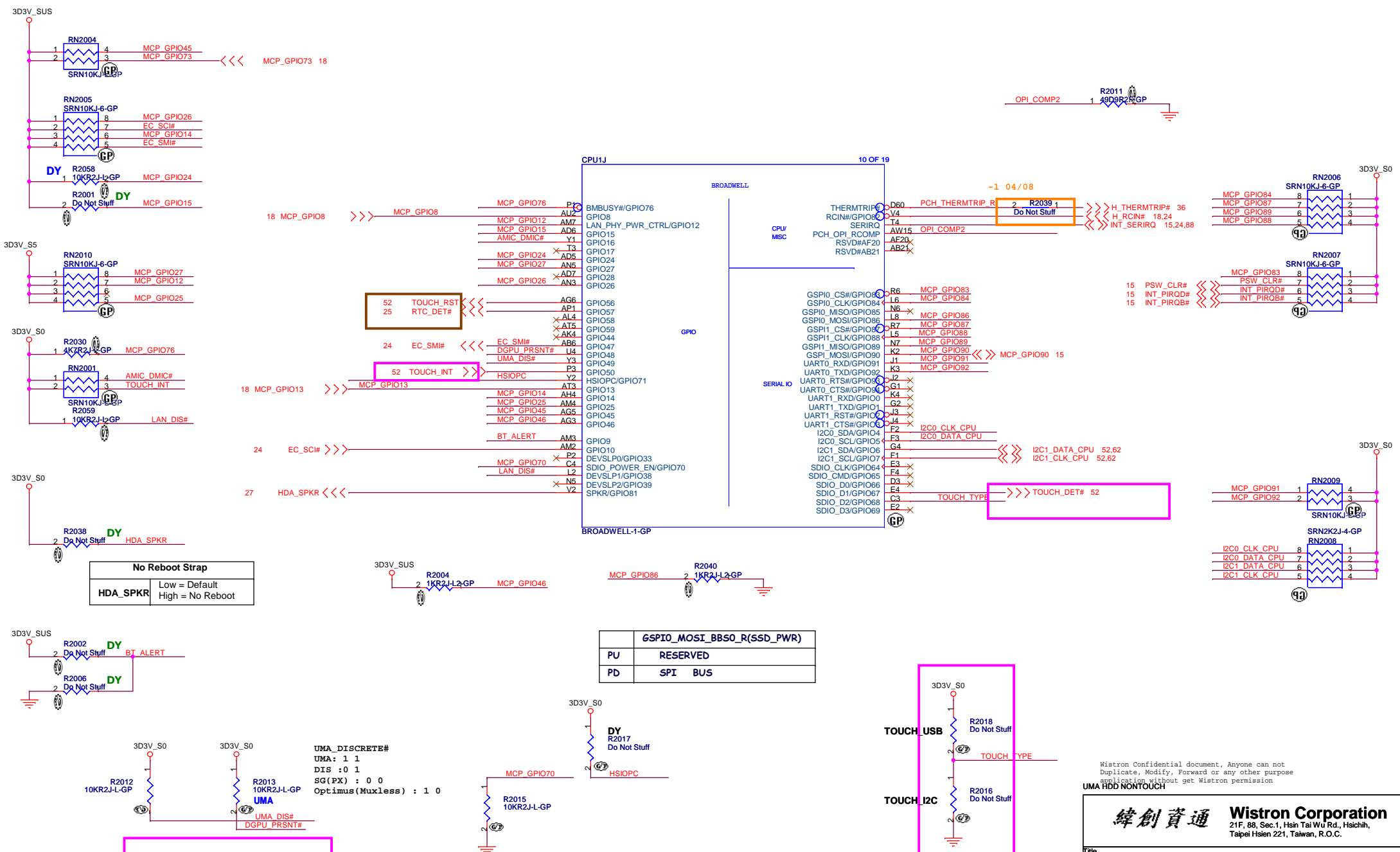
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Title	
CPU (DMI/FDI/PM)	
Size	Document Number
A3	MA30 HB ULT
Date: Tuesday, April 15, 2014	Sheet 17 of 102
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SSID = PCH



SSID = PCH



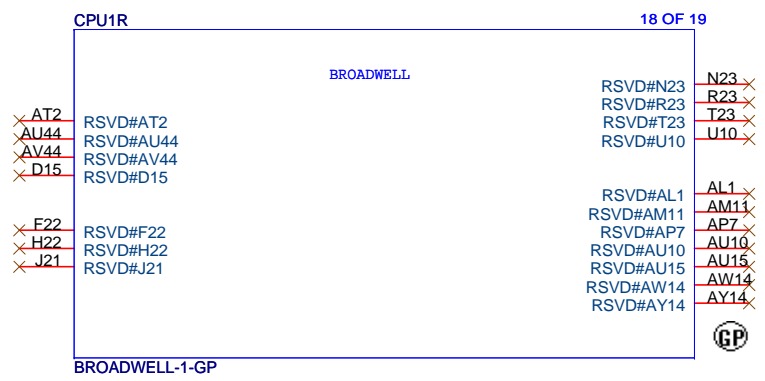
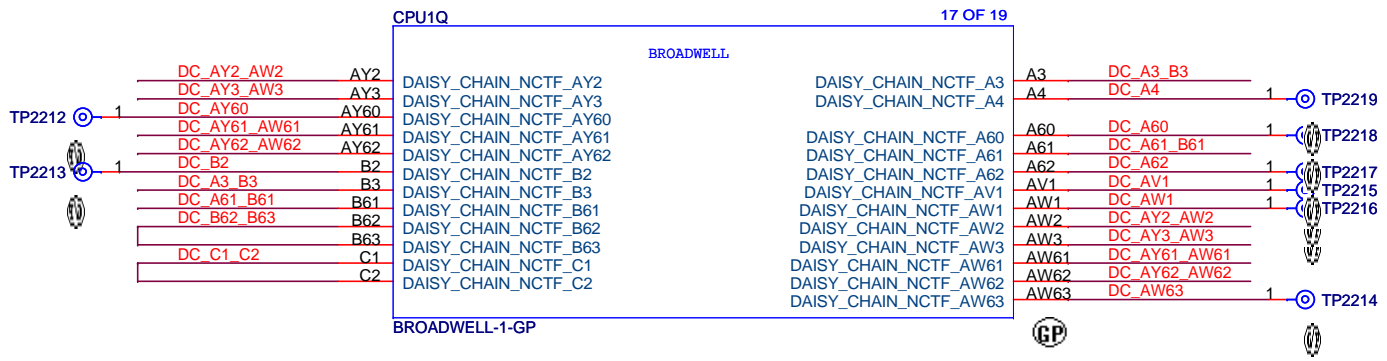
No Reboot Strap
 HDA_SPKR Low = Default
 High = No Reboot

UMA_DISCRETE#
 UMA : 1 1
 DIS : 0 1
 SG (PX) : 0 0
 Optimus (Muxless) : 1 0

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Title CPU (GPIO/MISC)		
Size A3	Document Number MA30 HB ULT	Rev 2
Date: Tuesday, April 15, 2014	Sheet 20	of 102

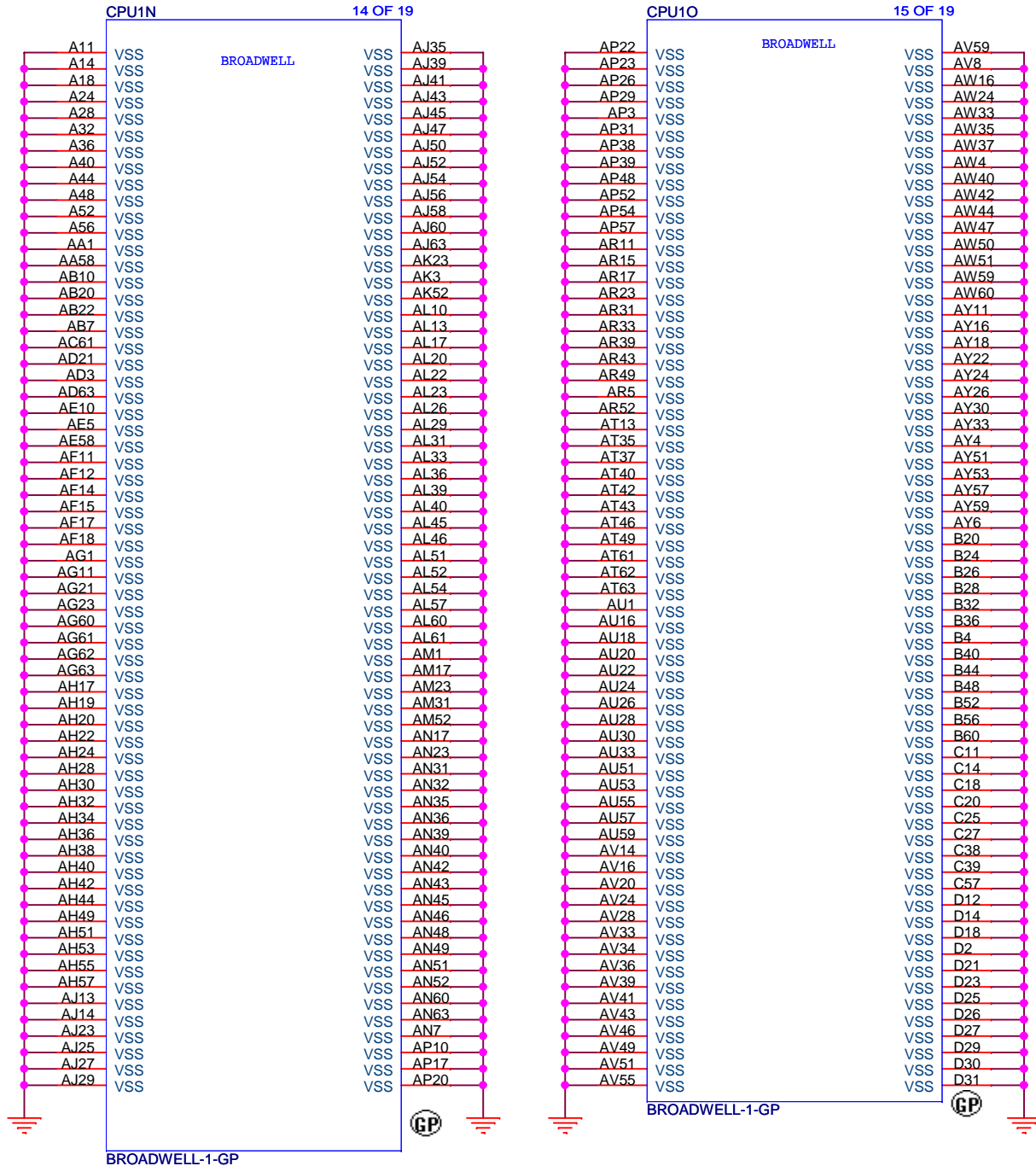


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Title			
CPU (RSVD)			
Size	Document Number	Rev	
Custom	MA30 HB ULT	2	
Date:	Tuesday, April 15, 2014	Sheet	22 of 102

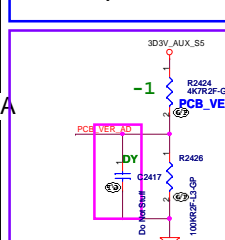
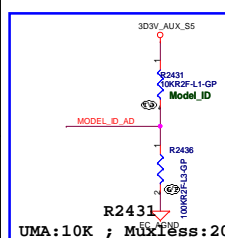
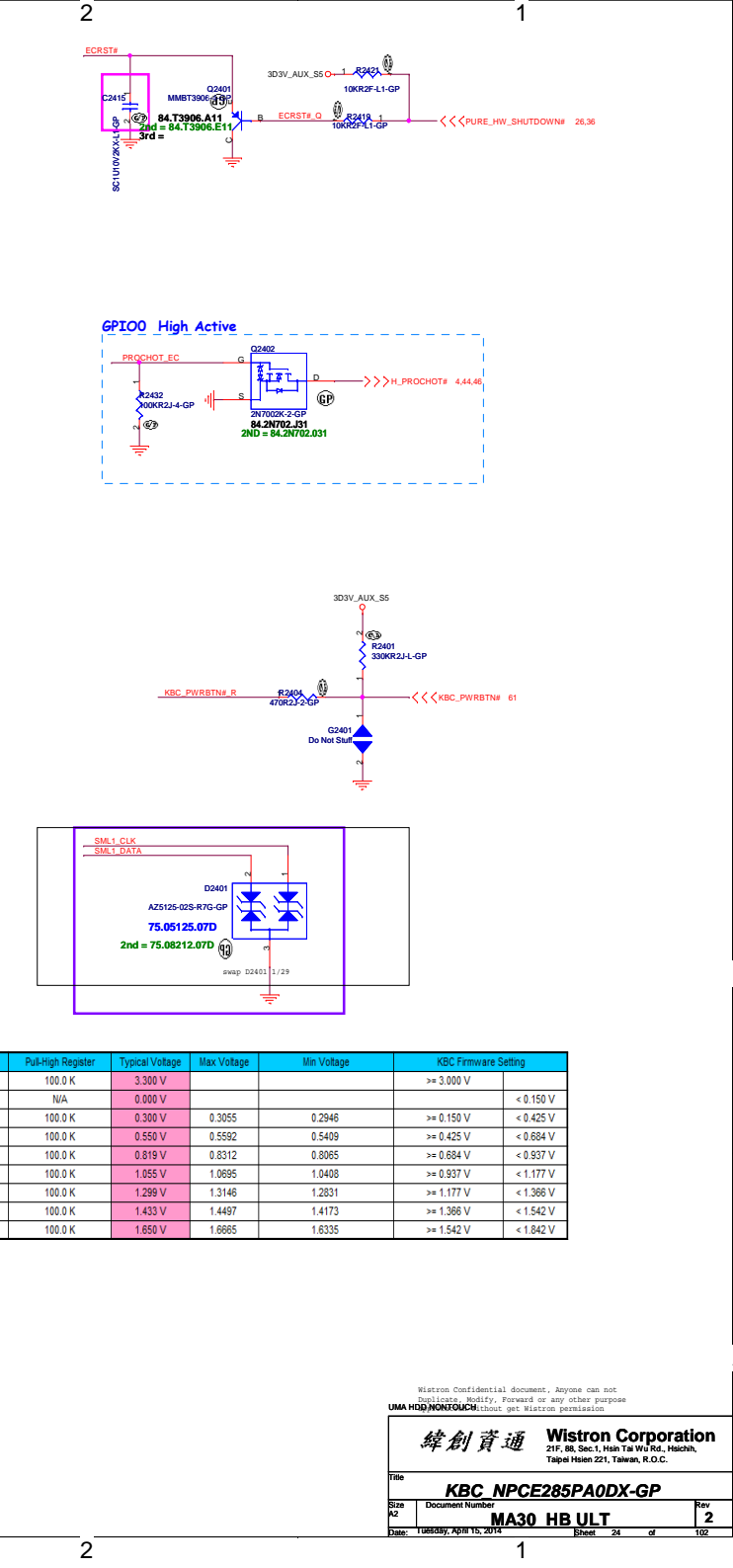
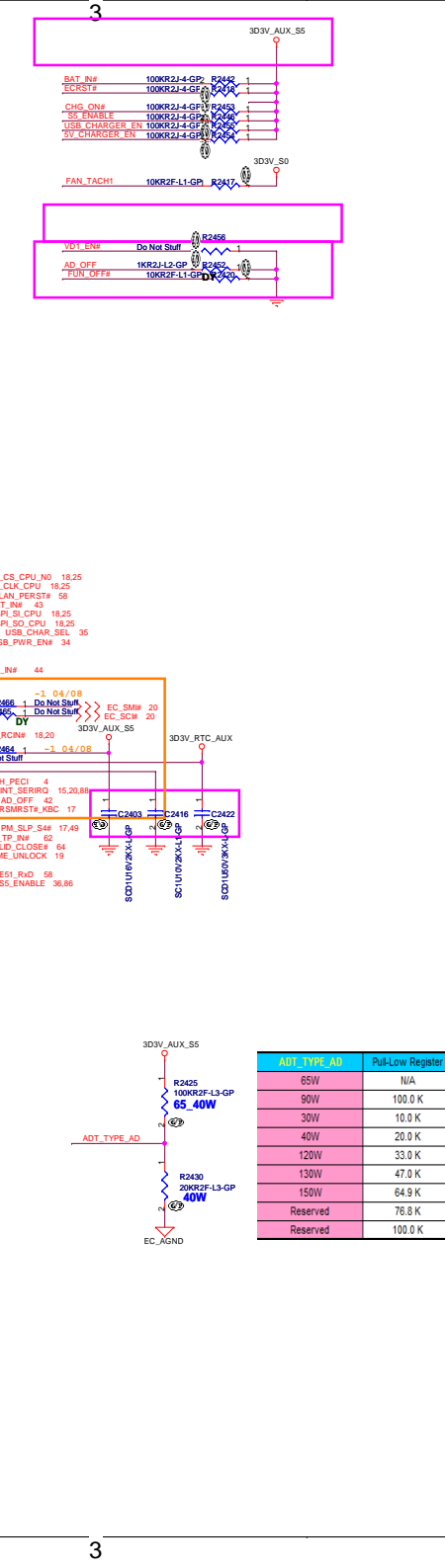
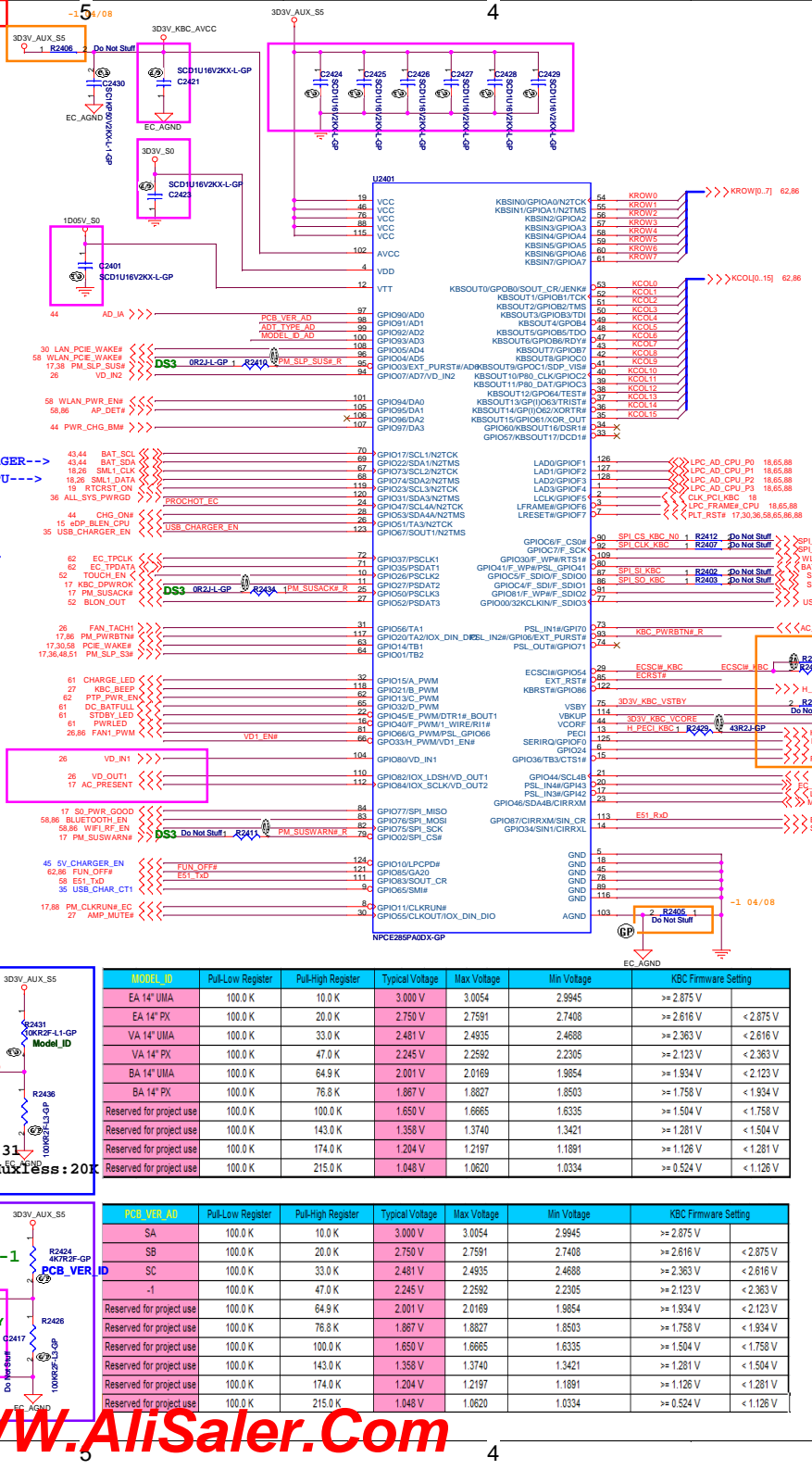
SSID = PCH



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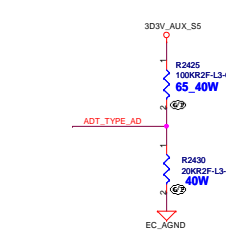
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Title		
CPU (VSS)		
Size	Document Number	Rev
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MODEL_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
EA 14" UMA	100.0 K	10.0 K	3.0054	3.0054	2.9945	>= 2.875 V
EA 14" PX	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V < 2.875 V
VA 14" UMA	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V < 2.616 V
VA 14" PX	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V < 2.363 V
BA 14" UMA	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V < 2.123 V
BA 14" PX	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V < 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V < 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V < 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V < 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.924 V < 1.126 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.0054	3.0054	2.9945	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V < 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V < 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V < 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V < 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V < 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V < 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V < 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V < 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.924 V < 1.126 V

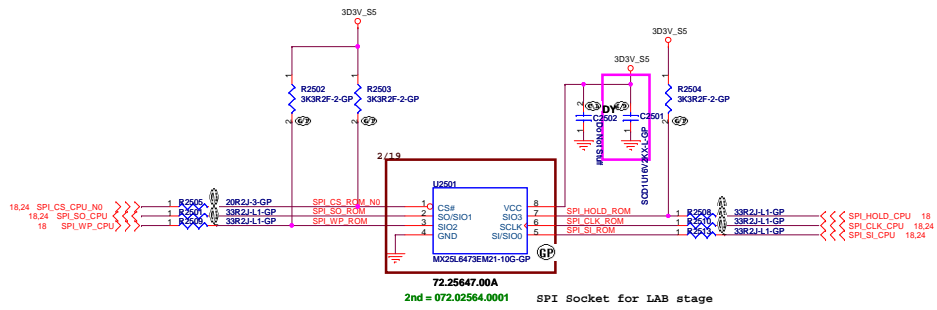


ANT_TYPL_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
85W	N/A	100.0 K	3.300 V			>= 3.000 V
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	0.2946	>= 0.150 V < 0.425 V
40W	20.0 K	100.0 K	0.550 V	0.5592	0.5409	>= 0.425 V < 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.8312	0.8065	>= 0.684 V < 0.937 V
130W	47.0 K	100.0 K	1.055 V	1.0695	1.0408	>= 0.937 V < 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.3146	1.2831	>= 1.177 V < 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	1.4173	>= 1.366 V < 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.542 V < 1.842 V

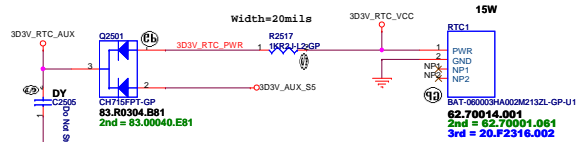
SSID = Flash.ROM SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

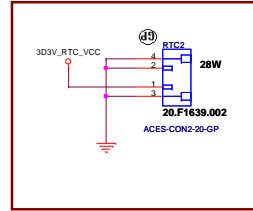
SPI FLASH ROM (8M byte)
72.25Q64.K01
2nd=072.02564.0001



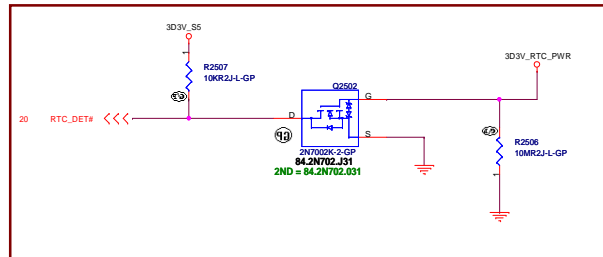
SSID = RBAT



3/6



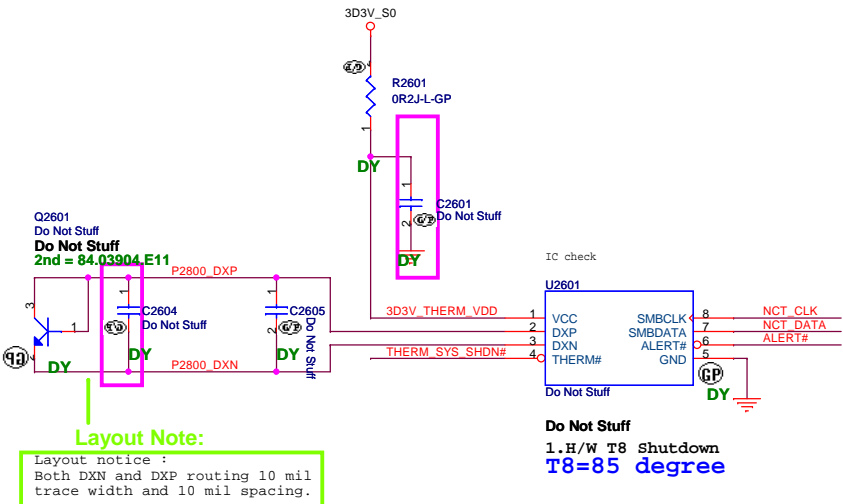
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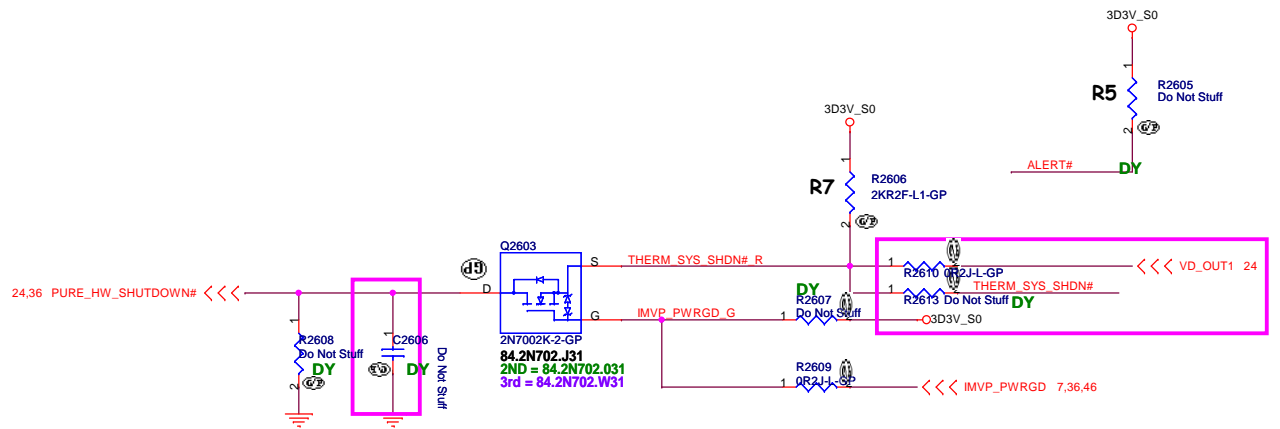
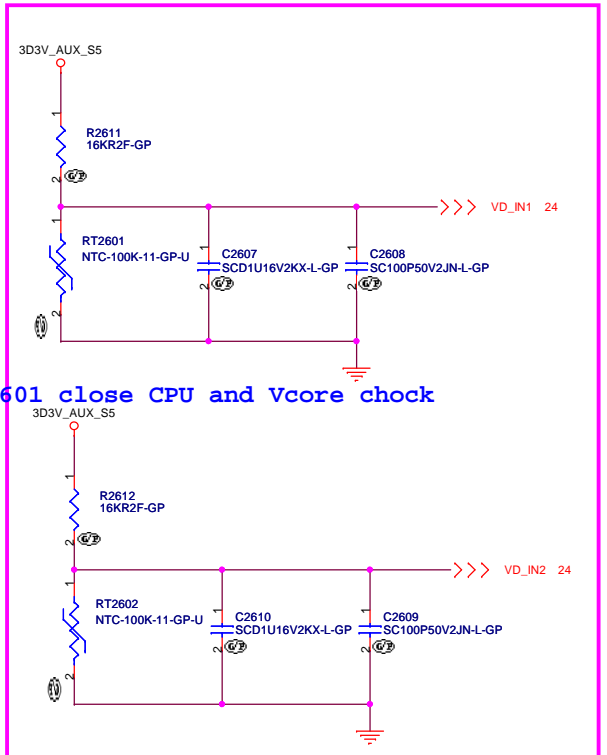
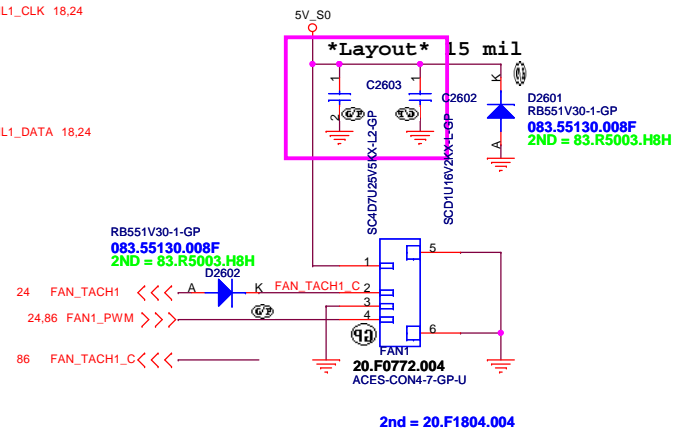
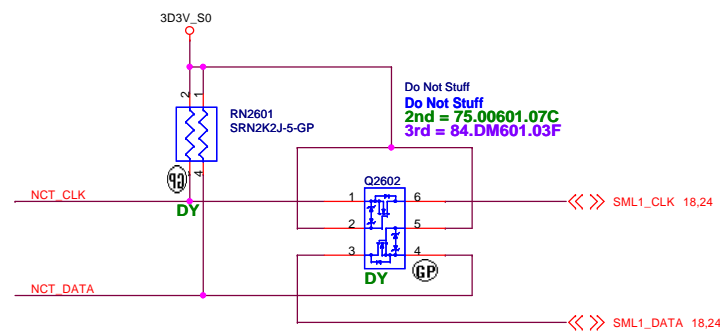
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SSID = Thermal

Thermal sensor NCT 7718W



2.System Sensor, Put on palm rest



ALERT# /T_CRIT#
Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5	77°C	87°C	97°C	107°C	117°C
	79°C	89°C	99°C	109°C	119°C
	81°C	91°C	101°C	111°C	121°C
	83°C	93°C	103°C	113°C	123°C
	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

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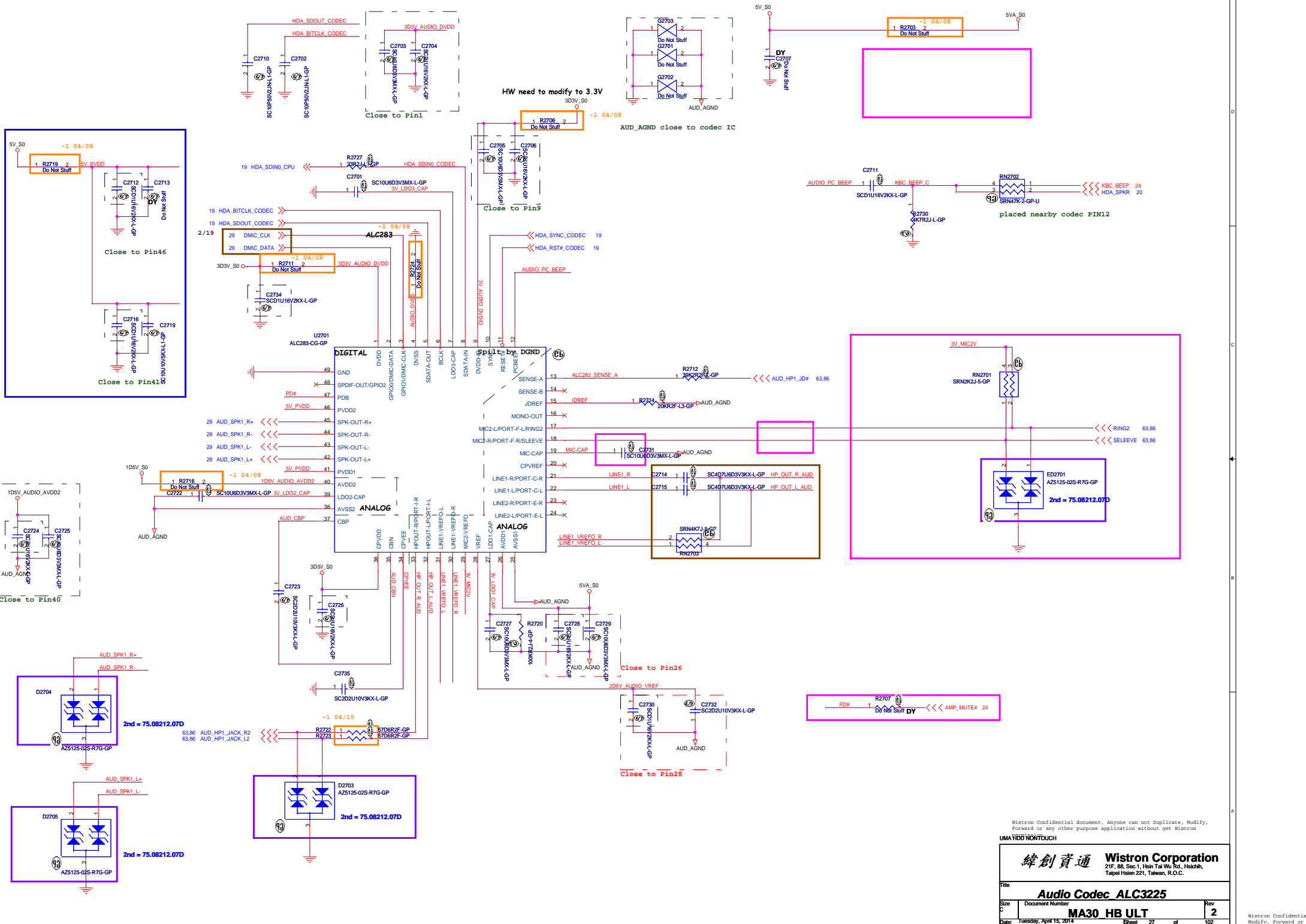
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Title: **G788P81/Fan Controller P2793**

Size A3 Document Number: **MA30 HB ULT** Rev: **SA**

Date: Tuesday, April 15, 2014 Sheet 26 of 102



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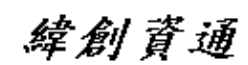
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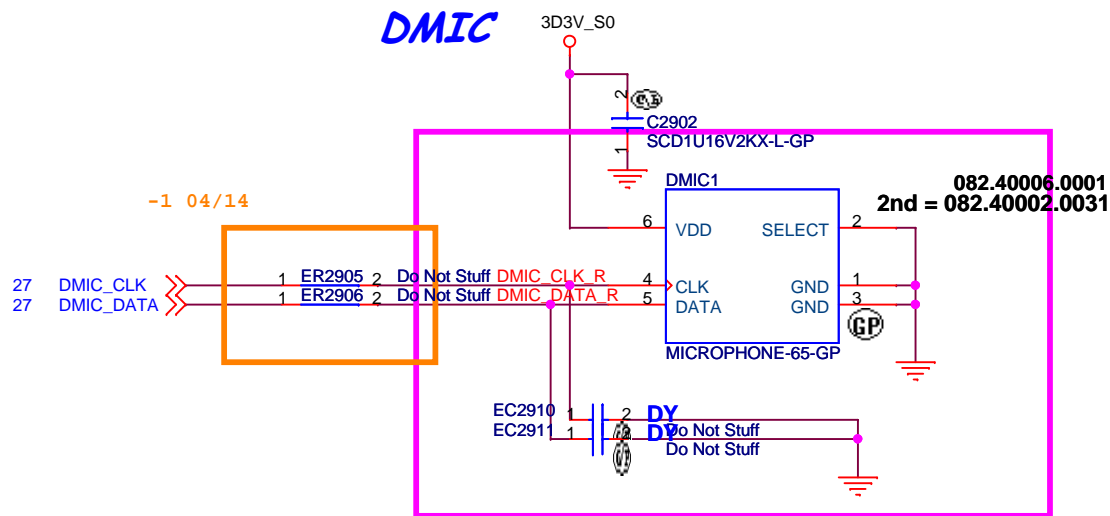
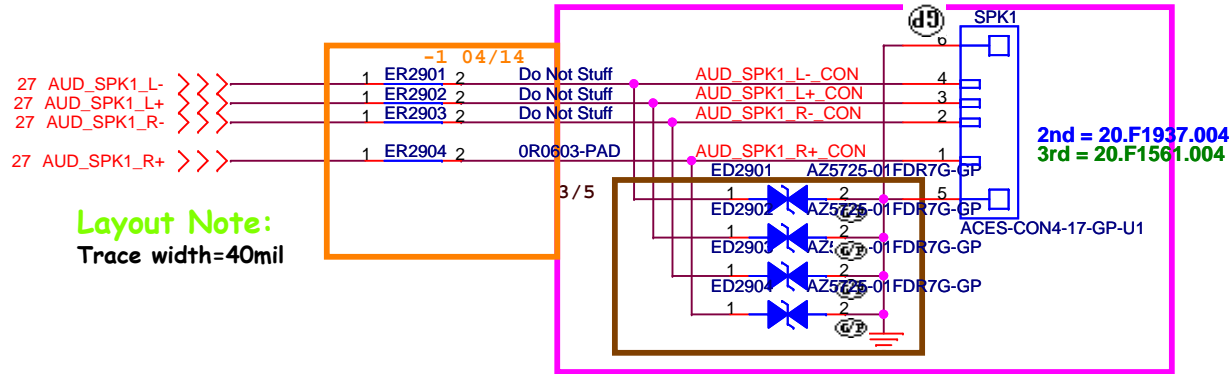
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Title <i>Audio AMP 1001</i>			
Size A4	Document Number MA30 HB ULT		Rev SA
Date: Tuesday, April 15, 2014		Sheet 28	of 102



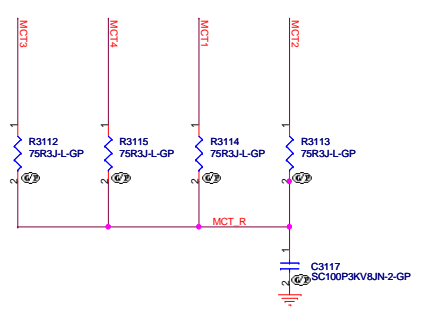
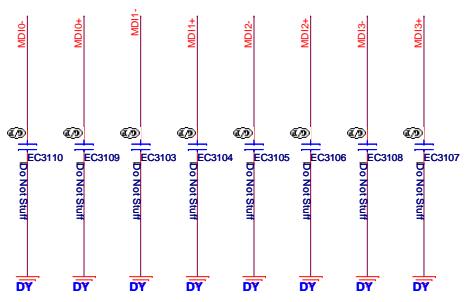
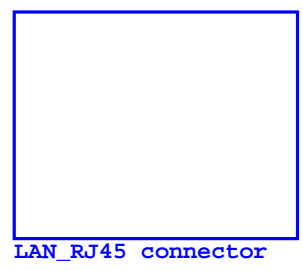
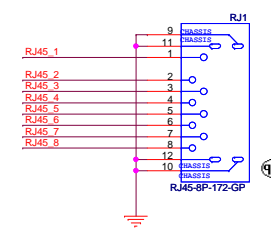
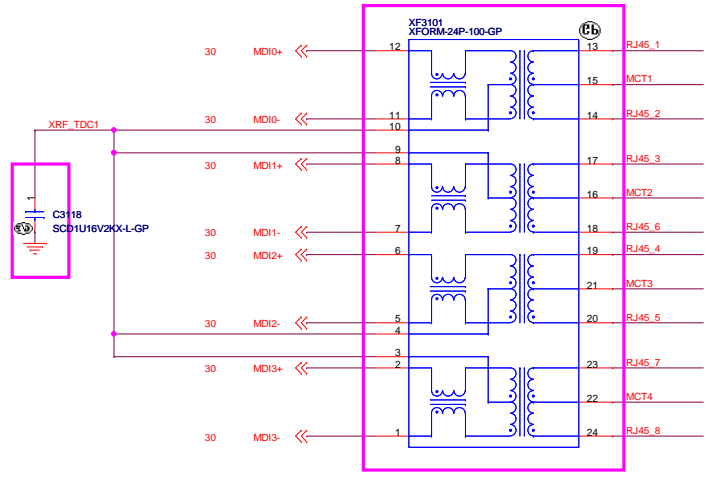
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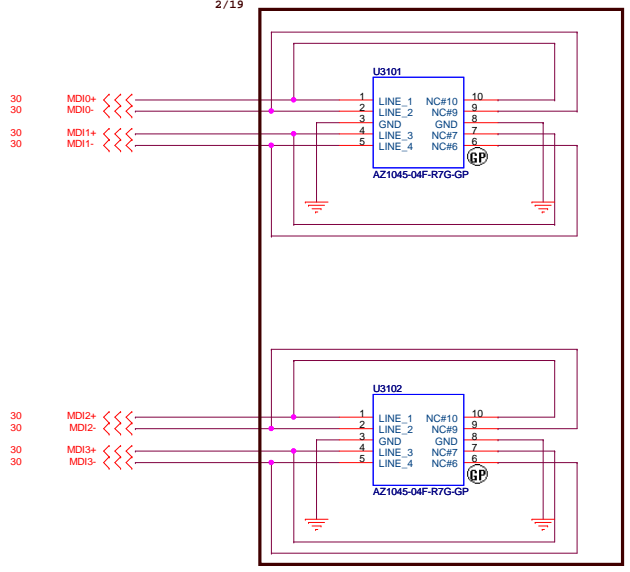
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Title		Audio Jack	
Size	Document Number	MA30 HB ULT	
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SSID = LAN



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(LAN+VGA) CONNECTOR			
Title	Document Number		Rev
Size	Custom		2
Date:	1/28/2014		Sheet 31 of 102

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Title			
RTS5229(CARD READER)			
Size	Document Number		Rev
A4	MA30 HB ULT		2
Date: Tuesday, April 15, 2014		Sheet 32	of 102

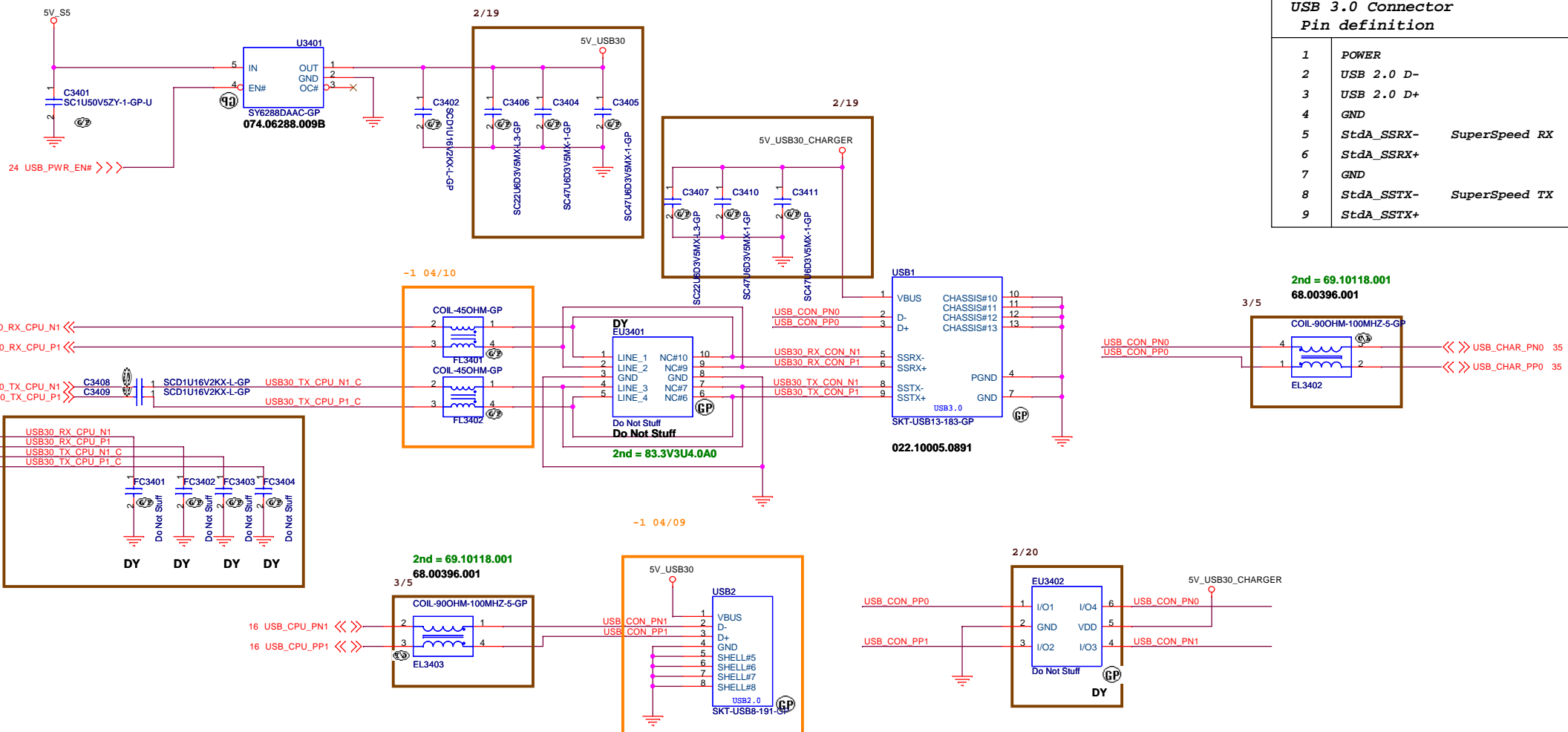
SSID = SDIO

SD//MS Card Reader

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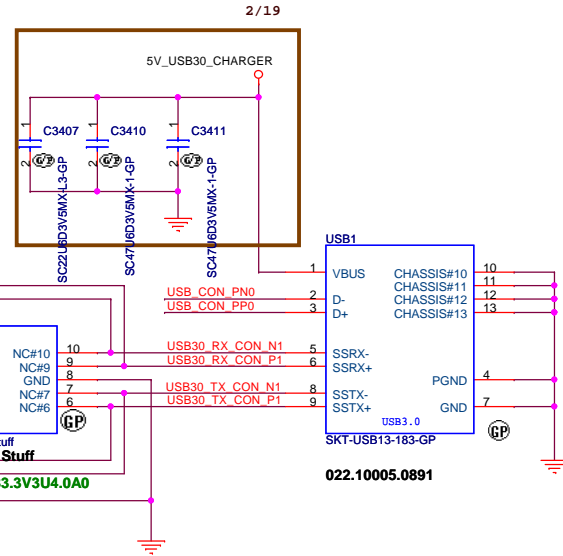
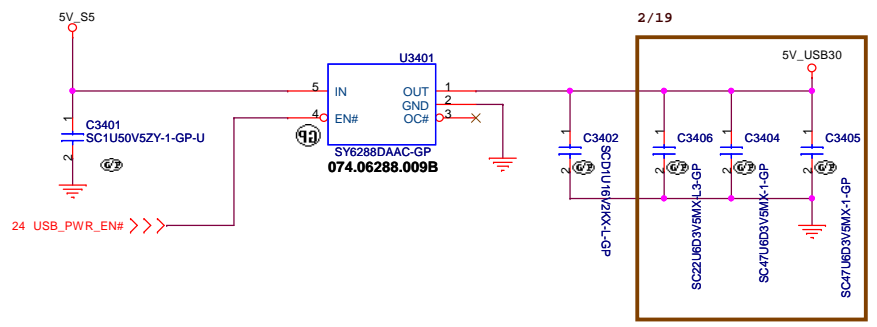
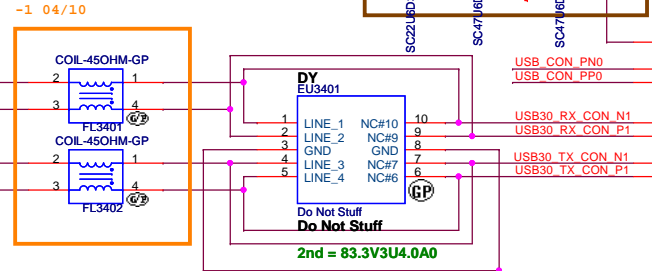
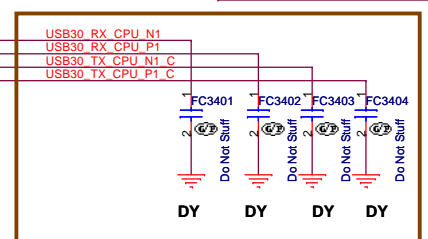
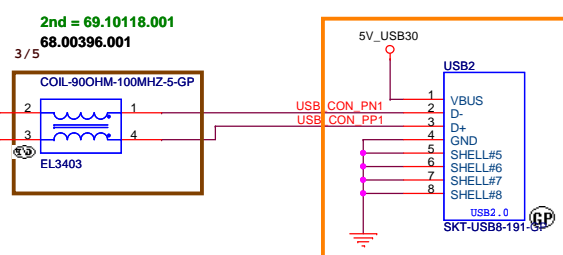
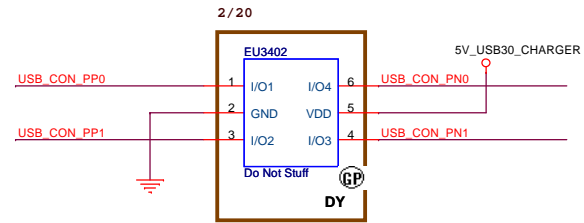
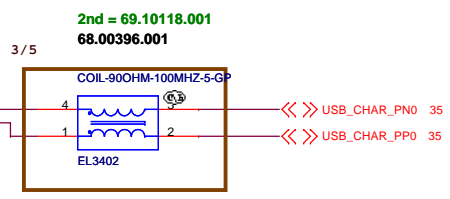
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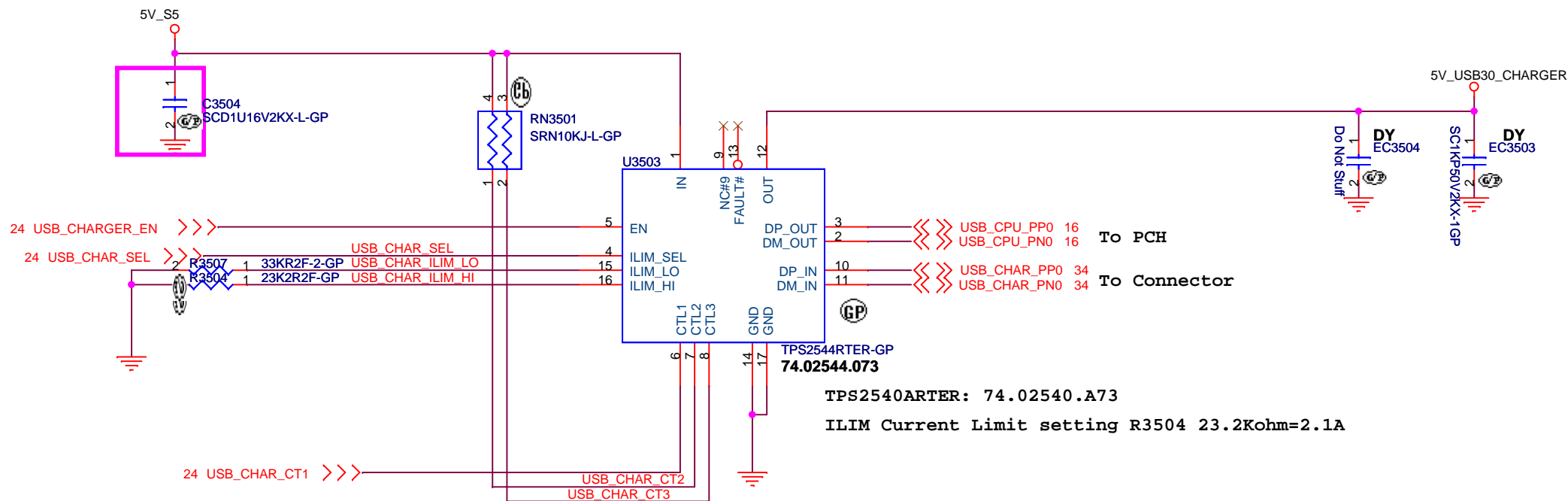
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Title			
CARD Reader CONN			
Size	Document Number		Rev
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USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+





3. Electrical Safety for USB3.0 Port

2.0 A \leq Measurement value \leq 2.2 A : Pass

1.9 A \leq Measurement value $<$ 2.0 A or 2.2 A $<$ Measurement value \leq 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port. And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A - 2.4 A).

Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

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Title

USB CHARGER

Size
A4

Document Number

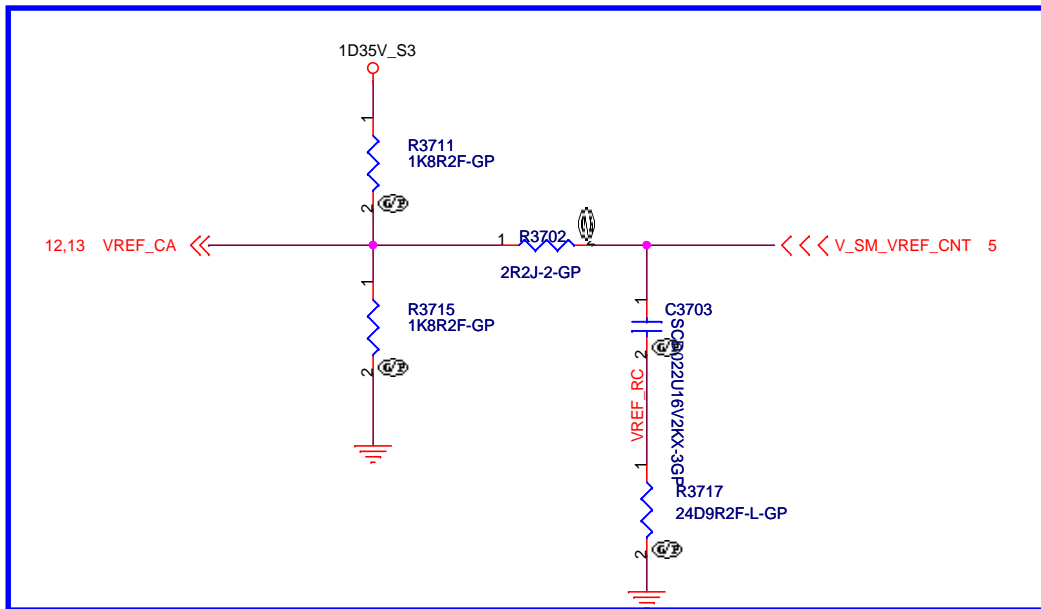
MA30 HB ULT

Rev

SA

Date: Tuesday, April 15, 2014

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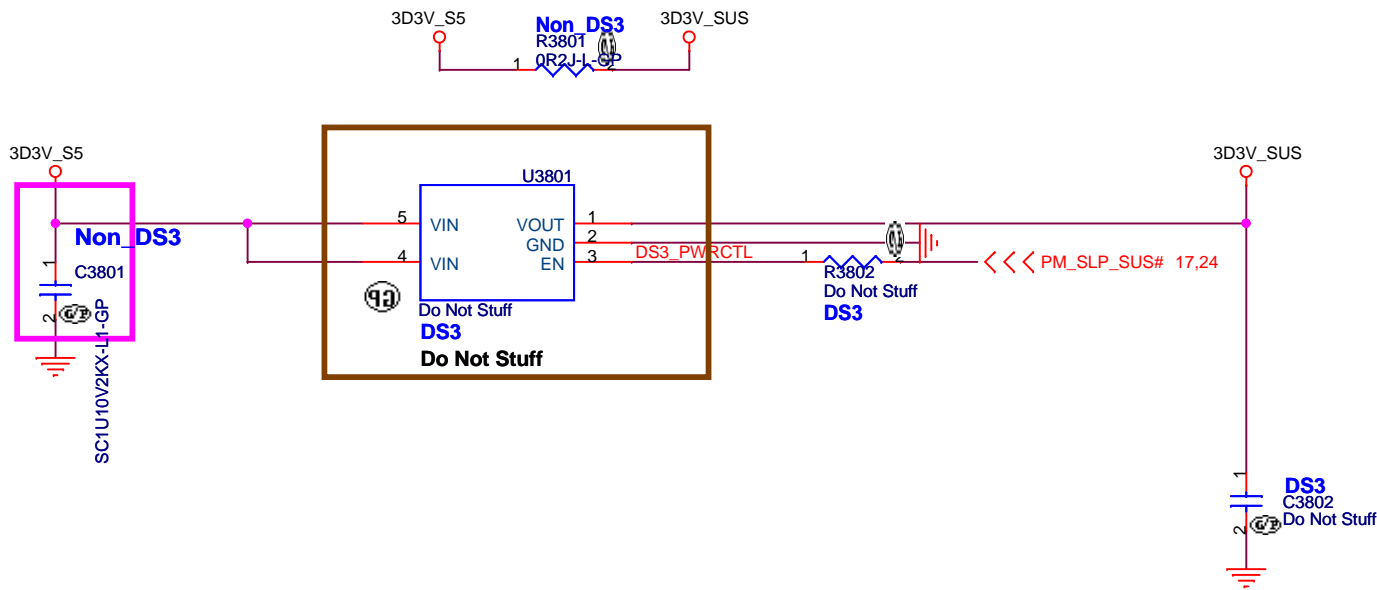


For Intel Recommend Close to DIMM

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ADAPTER OCP / S3 reduction	
Size	Document Number
Custom	MA30 HB ULT
Date:	Rev
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37	102



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DS3

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2

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Power Sequence

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Title			
1D05 M			
Size	Document Number	Rev	
Custom	MA30 HB ULT	2	
Date:	Tuesday, April 15, 2014	Sheet	39 of 102

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Title		
Connected Standby1		
Size	Document Number	Rev
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Title
Connected Standby2

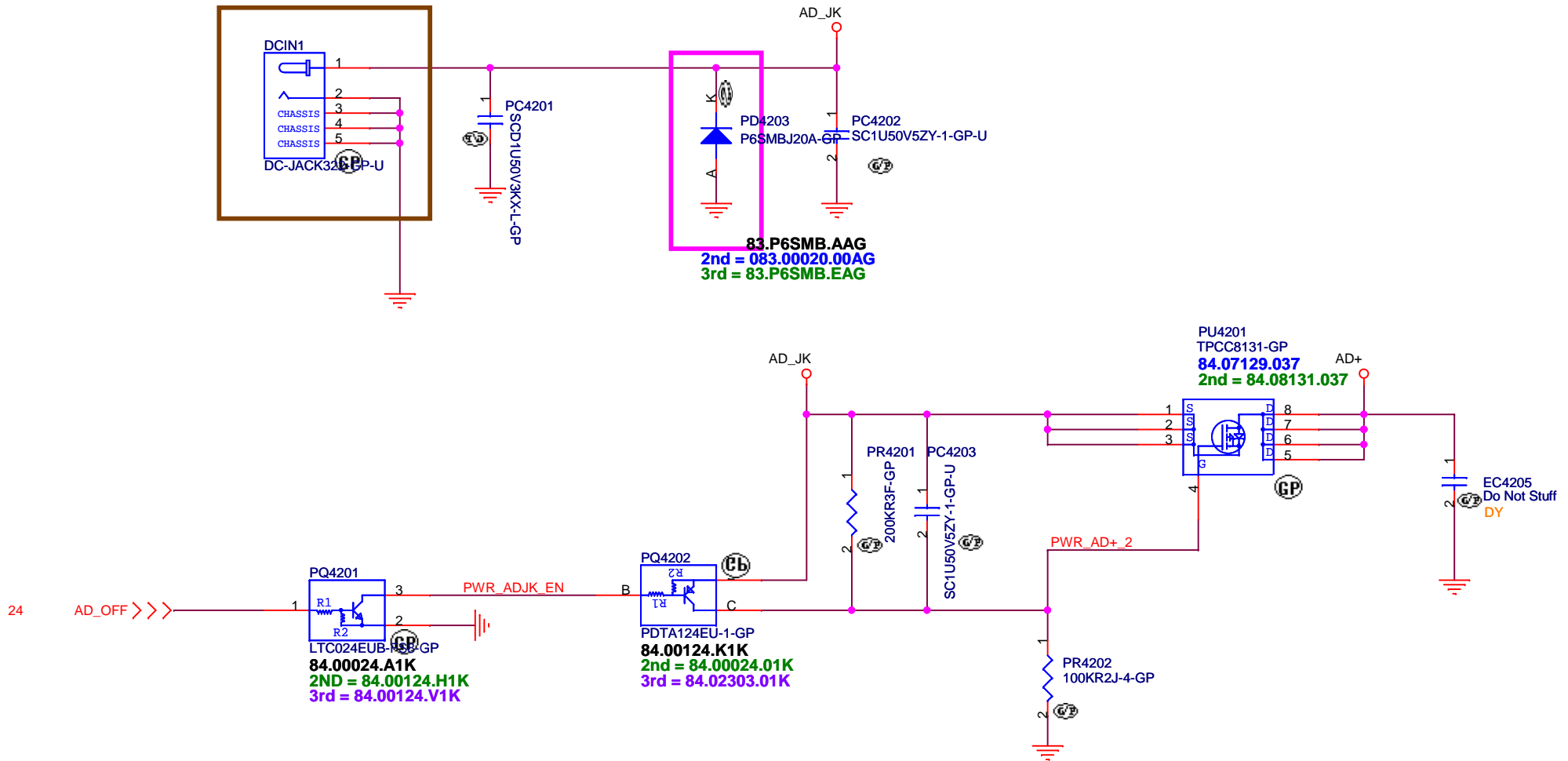
Size A	Document Number MA30 HB ULT	Rev 2
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ANNIE solution

Adaptor in to generate DCBATOUT

3 / 4

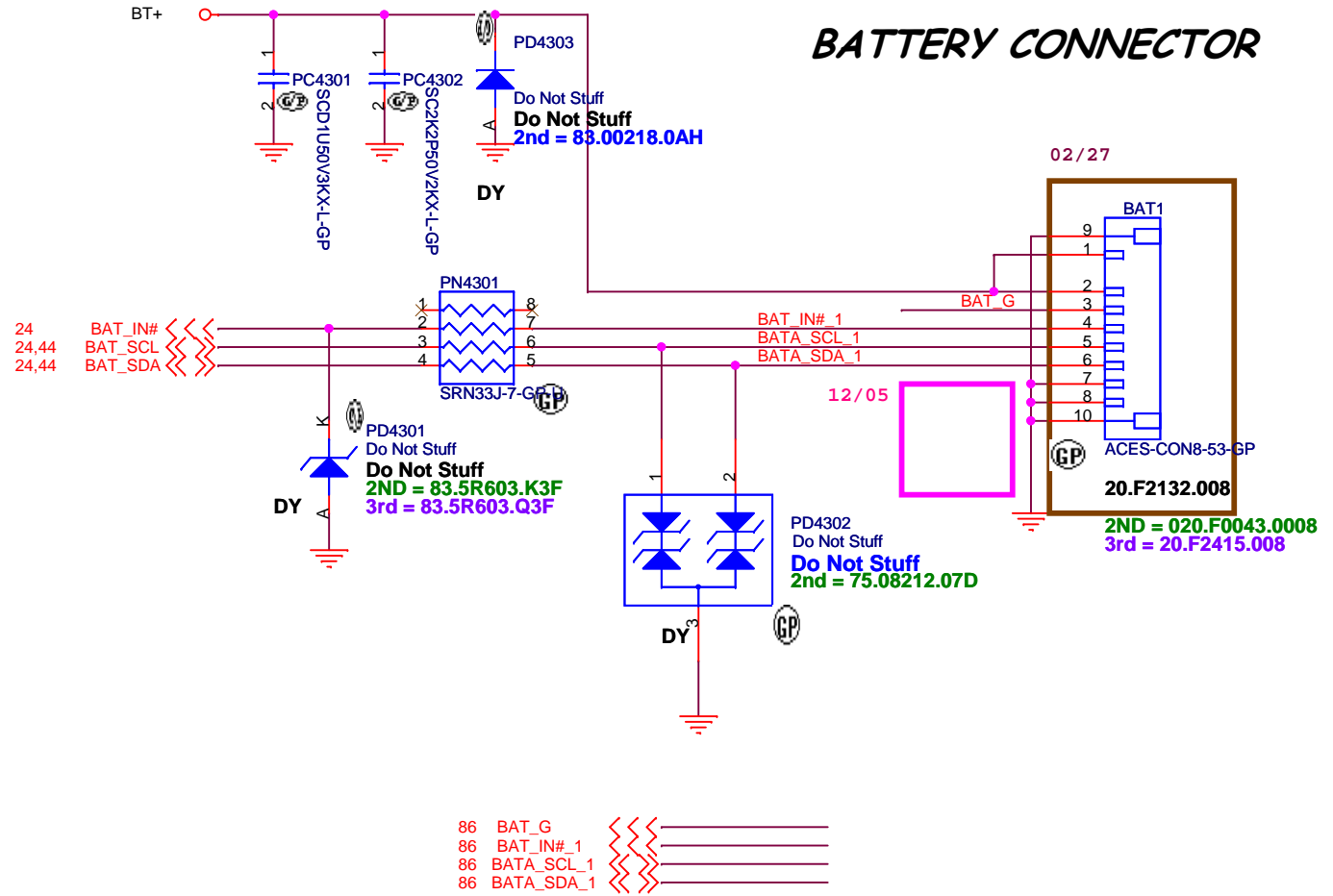
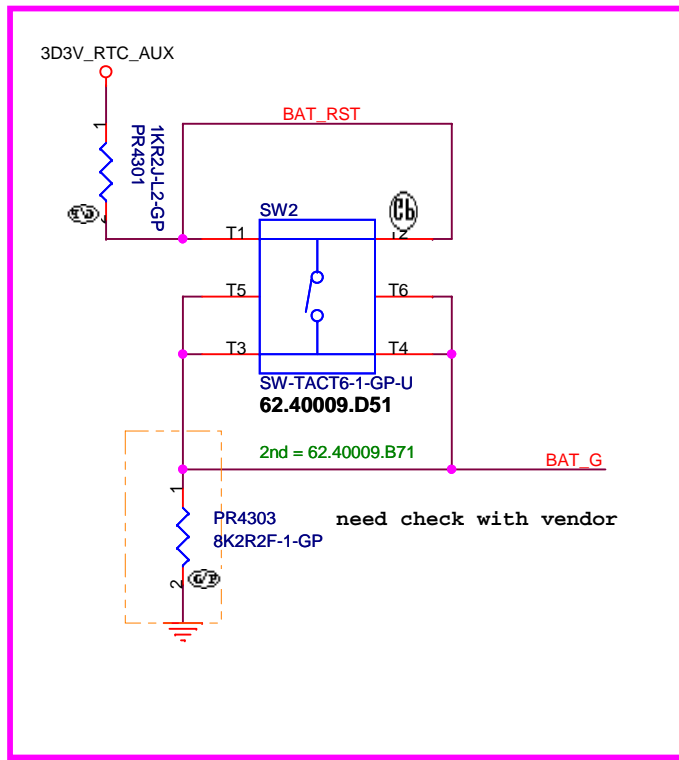


DC IN connector

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Title			
DCIN JACK			
Size A4	Document Number MA30 HB ULT	Rev 2	
Date: Tuesday, April 15, 2014	Sheet 42	of	102



BATTERY CONNECTOR

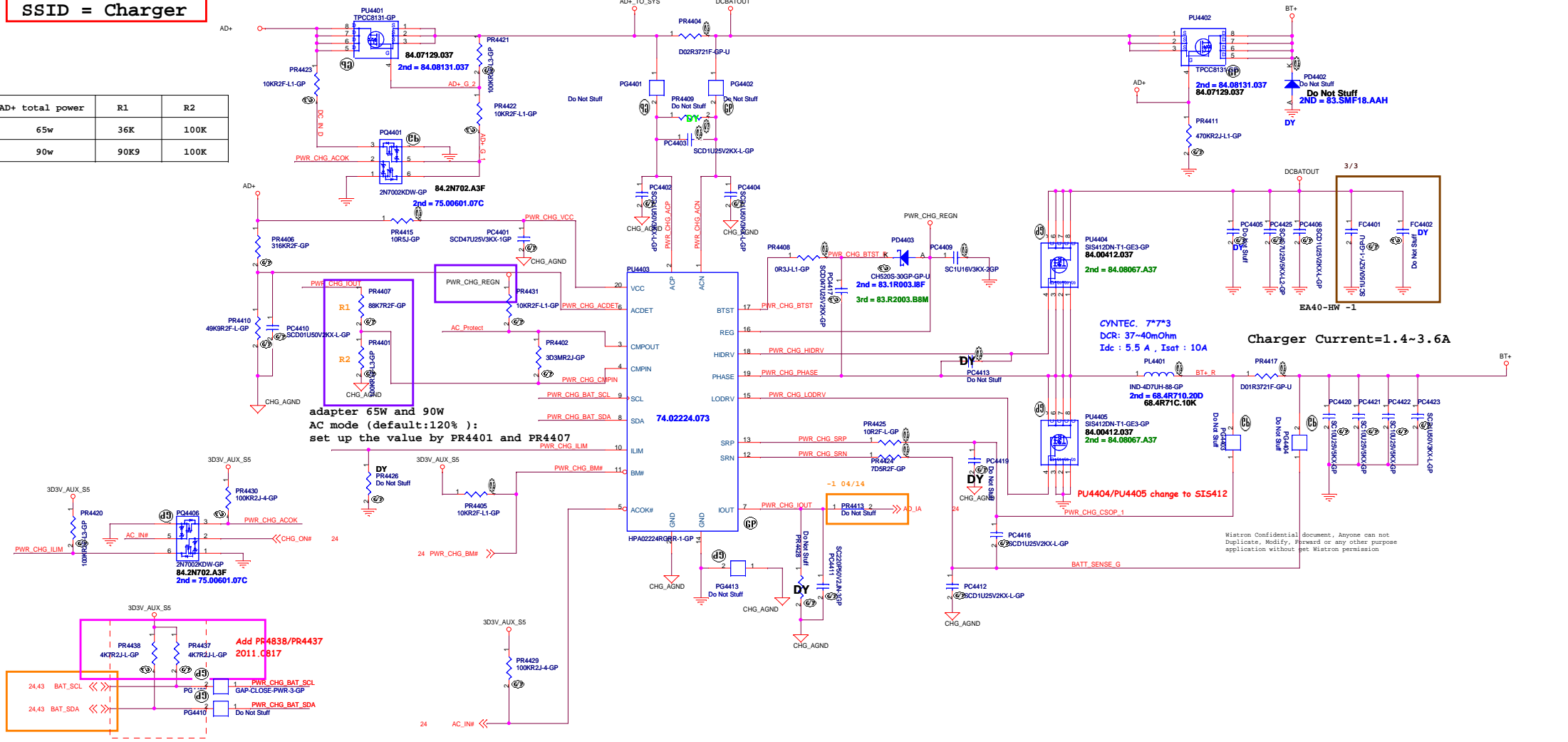
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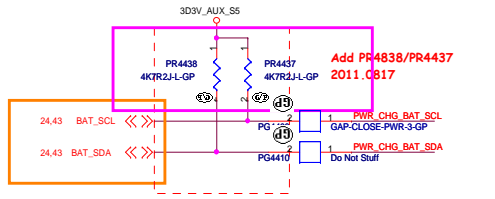
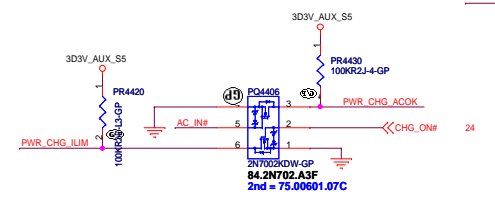
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Title			
BATT CONN			
Size A4	Document Number MA30 HB ULT	Rev 2	
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SSID = Charger

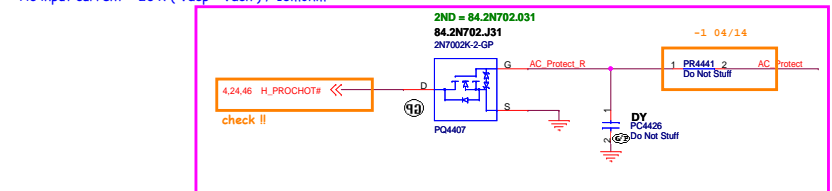
AD+ total power	R1	R2
65w	36K	100K
90w	90K9	100K



adapter 65w and 90w
AC mode (default:120%):
set up the value by PR4401 and PR4407



AC adapter detect current:
Ac input current = $20 \times (V_{acc} - V_{acn}) / 10m\Omega$



CYNTEC, 7*7*3
DCR: 37~40mOhm
I_{dc}: 5.5 A, I_{sat}: 10A
Charger Current=1.4~3.6A

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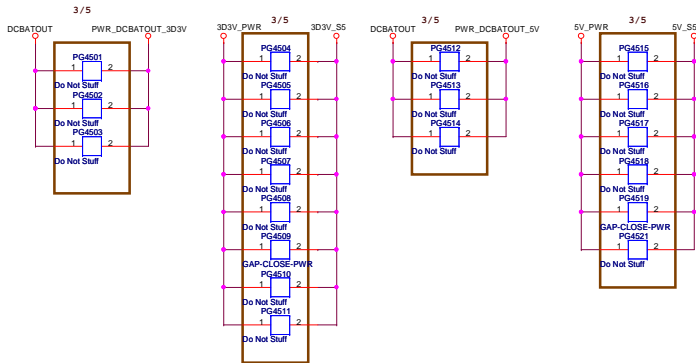
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24737**

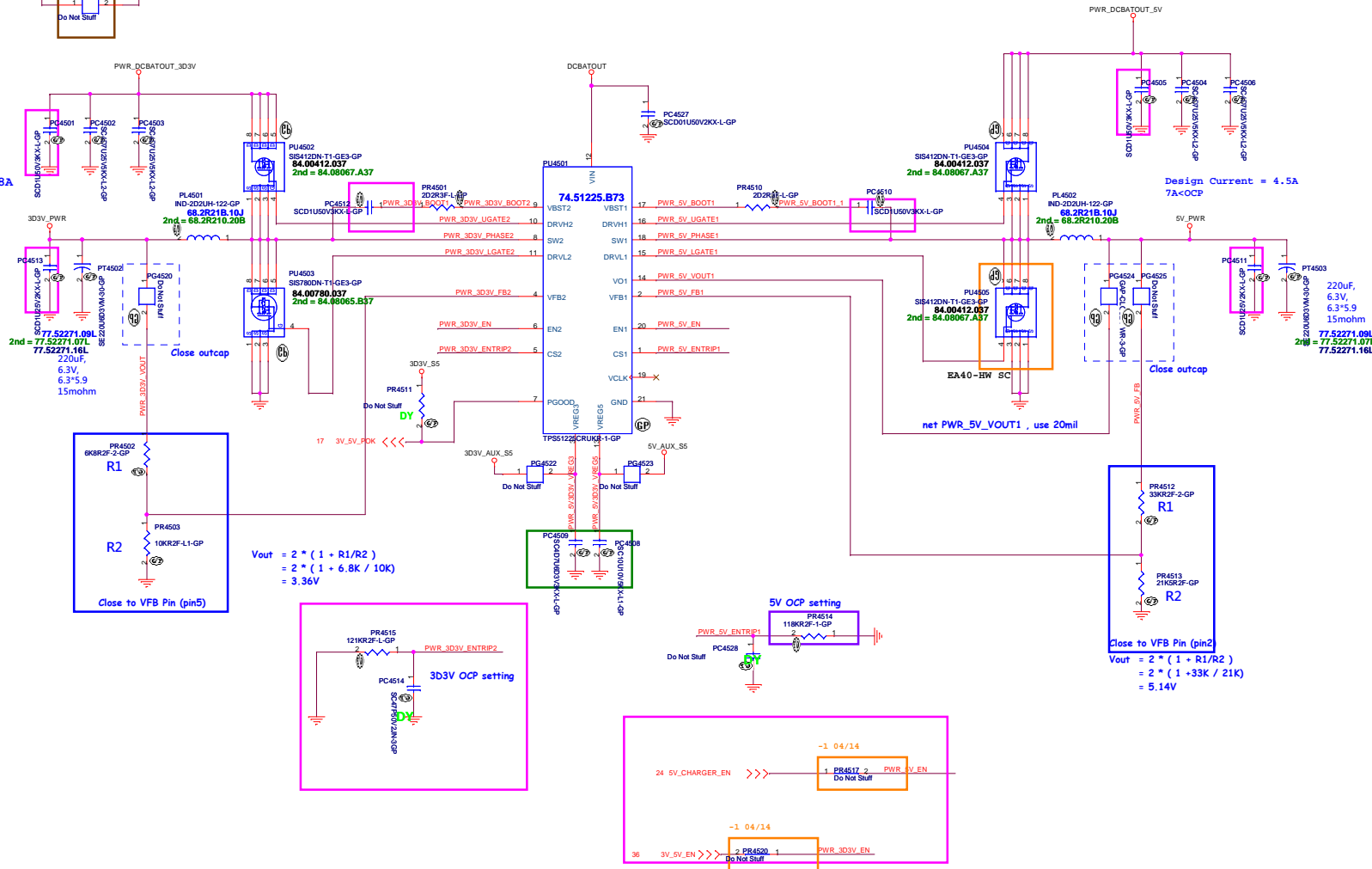
Rev: SA

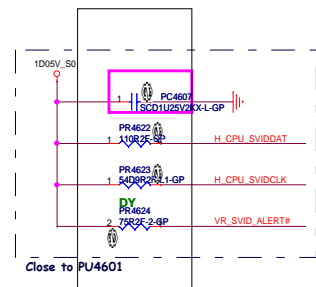
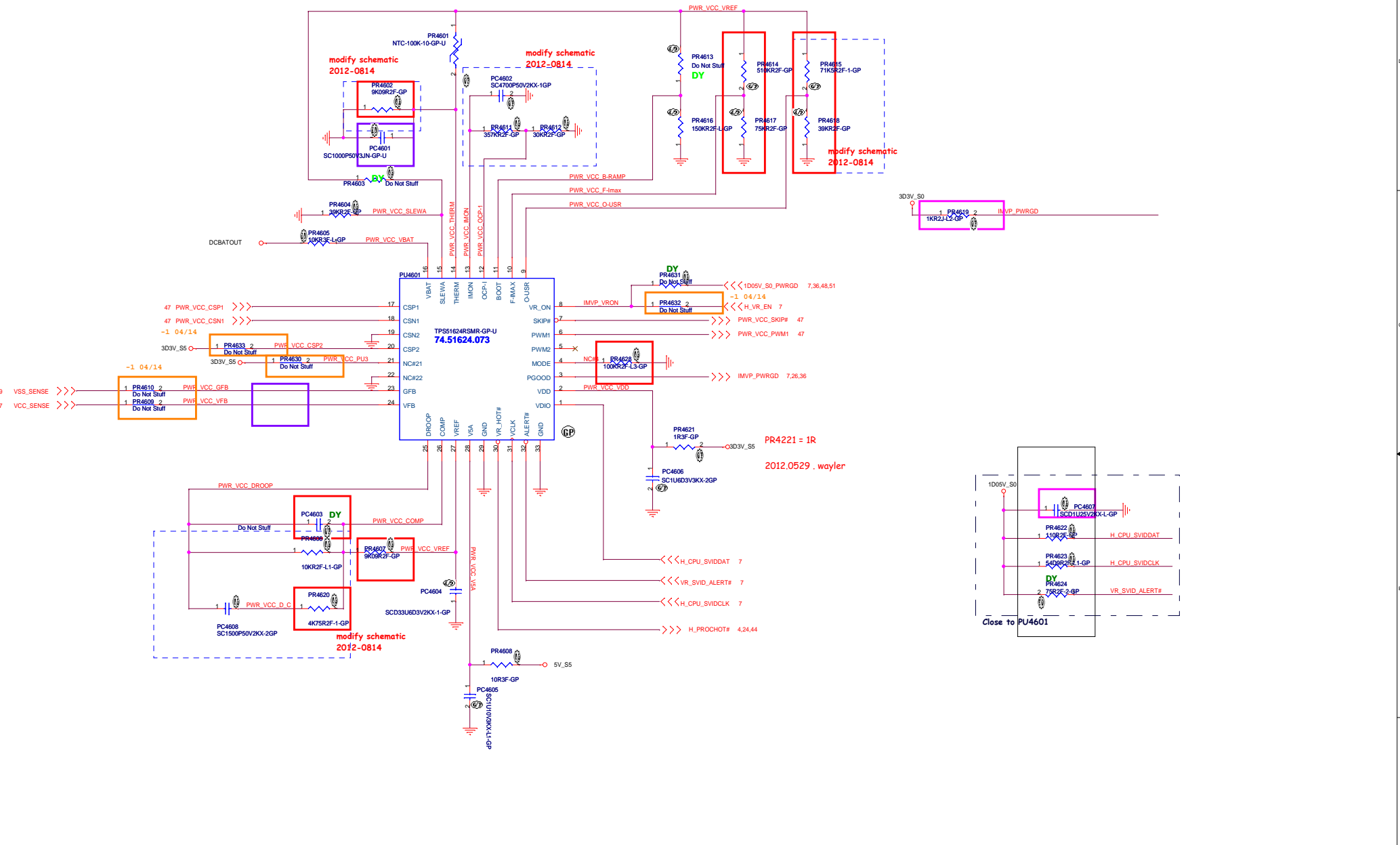
Date: Tuesday, April 15, 2014

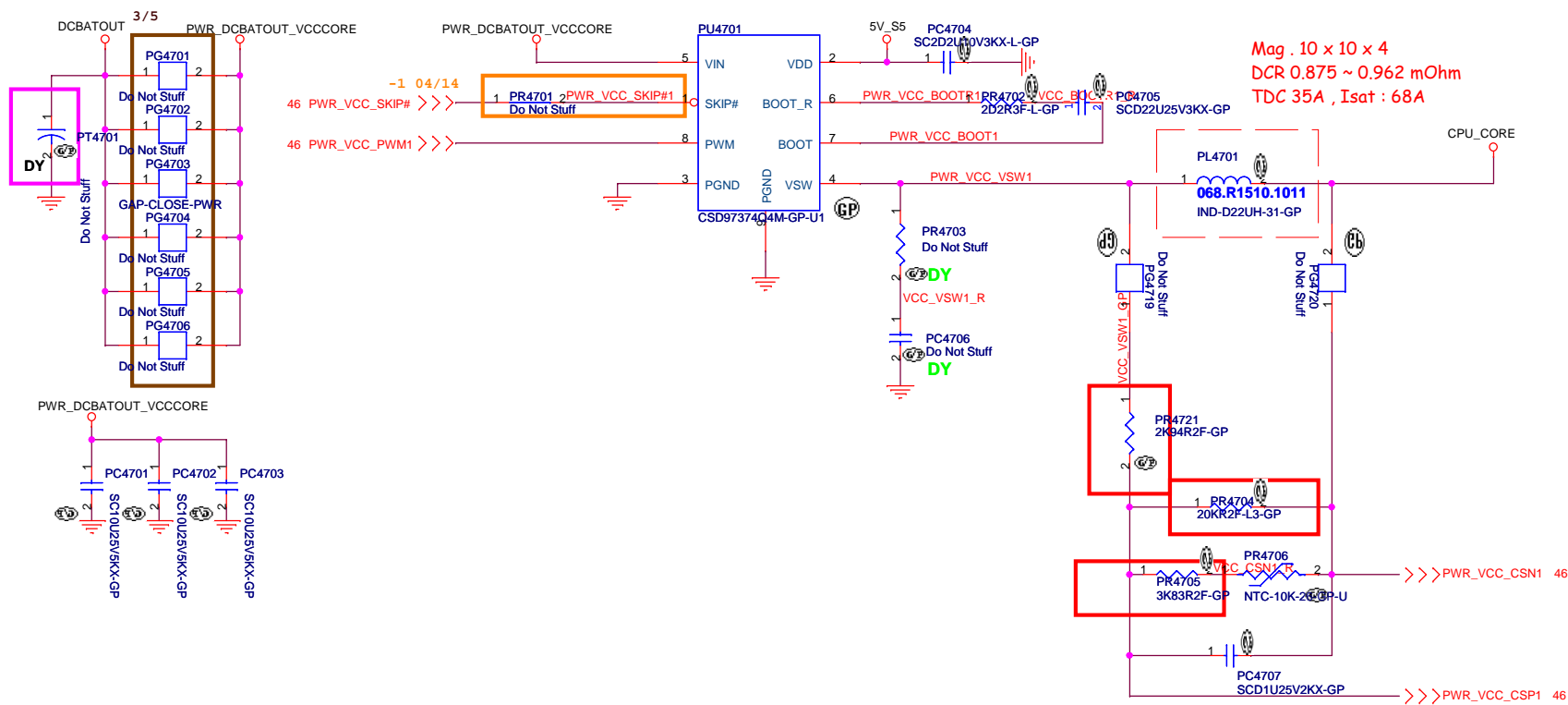
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I_{omax} = 7.998A
OCP > 11A



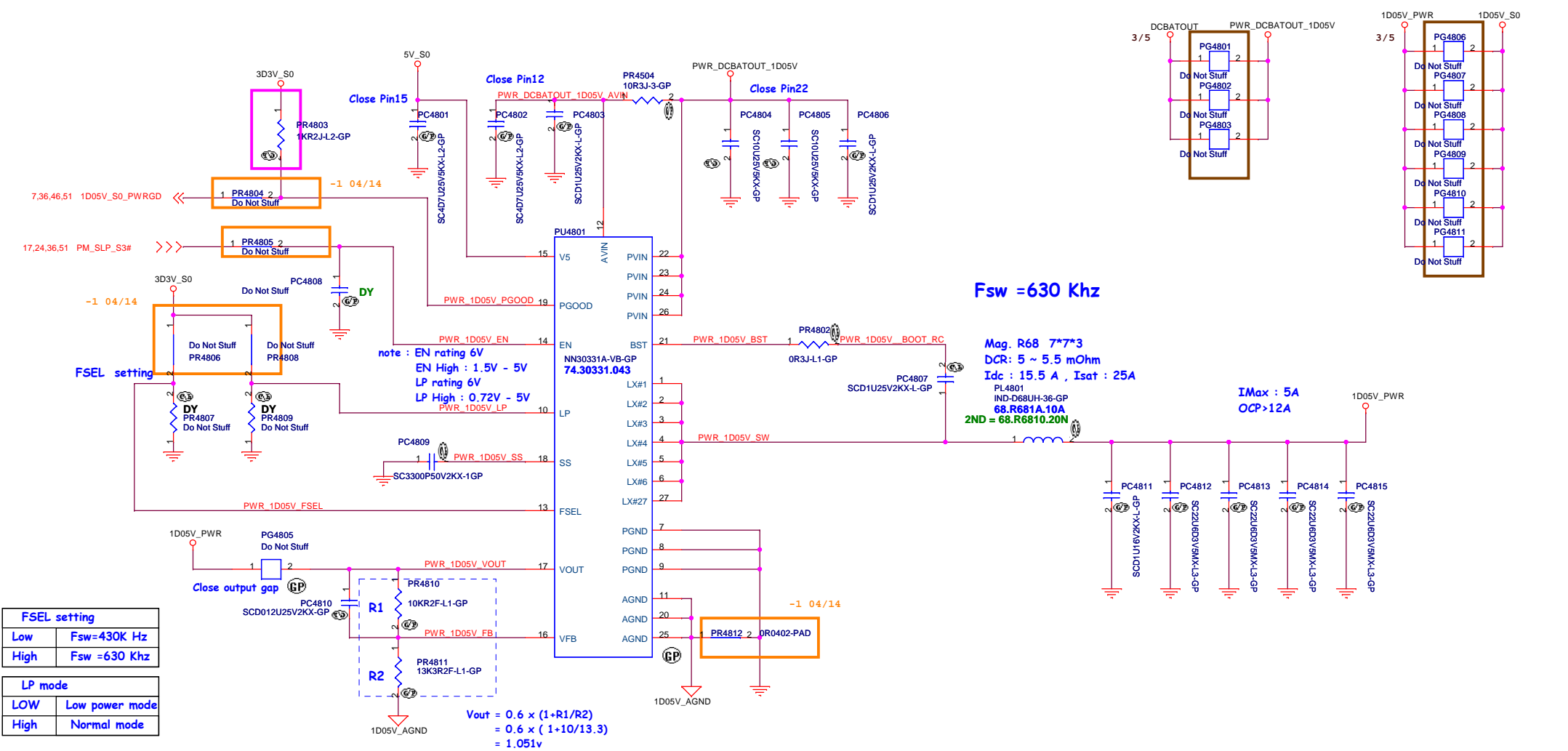




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Title			
TPS51622 CPUCORE(2/2)			
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NN30331 for 1D05V



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Title: **DC to DC 1D05V(NN30331)**

Size A3 Document Number **MA30 HB ULT** Rev **SA**

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Title		
1D8V S0 SYW232		
Size	Document Number	Rev
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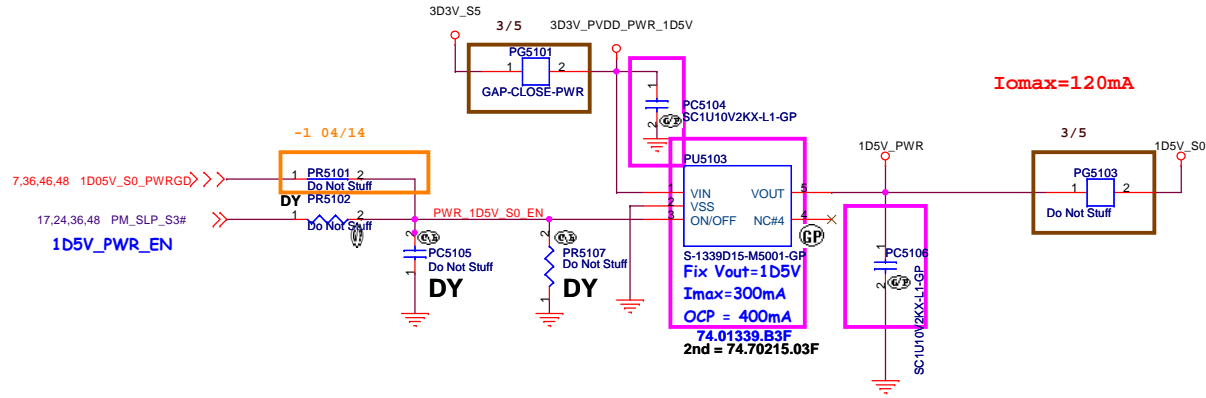
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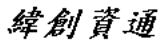
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SYW232 for 1D5V_S0

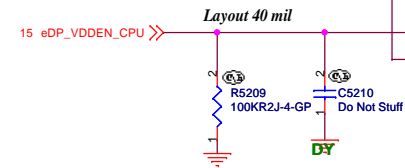
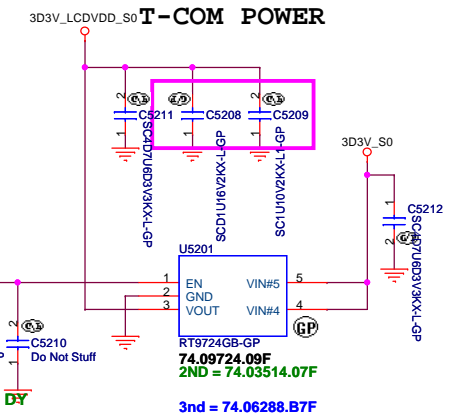
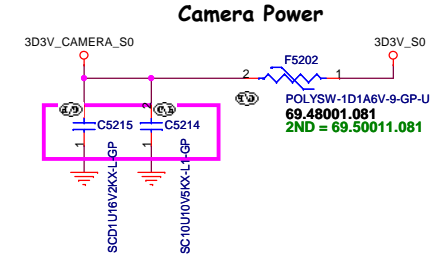
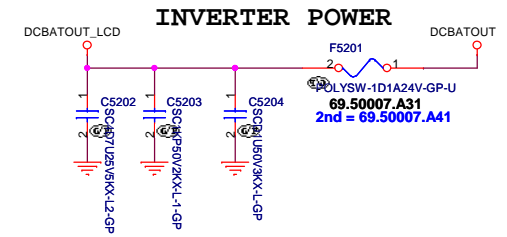
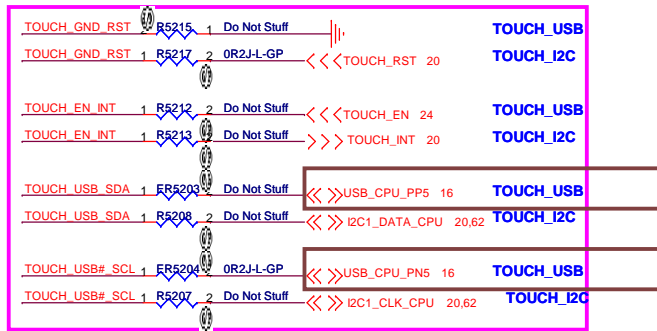
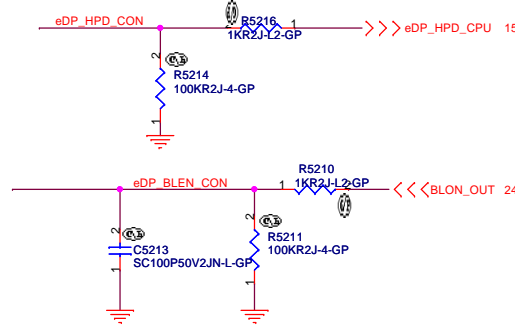
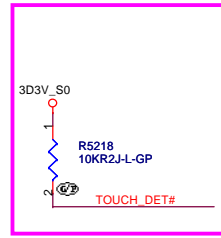
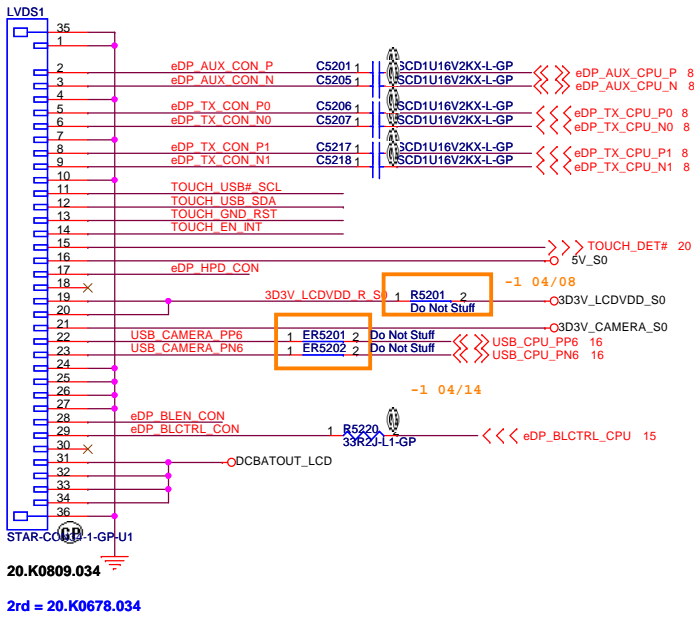


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Title 1D5V_S0 SYW232	
Size A3	Document Number MA30 HB ULT
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SSID = VIDEO



EDP connector

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File			EDP Connector		
Size	Document Number	Rev			
A3	MA30 HB ULT	SA			
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Title		
CRT Board Connector		
Size	Document Number	Rev
A3	MA30 HB ULT	SA
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5

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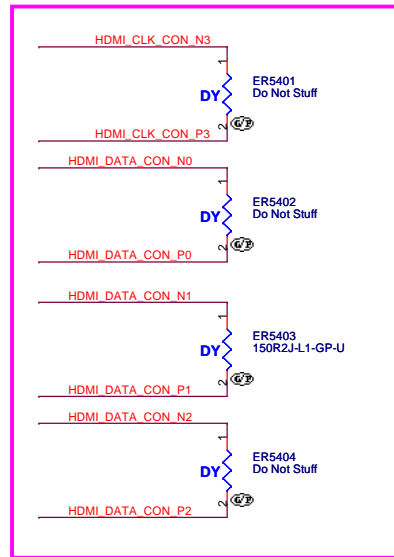
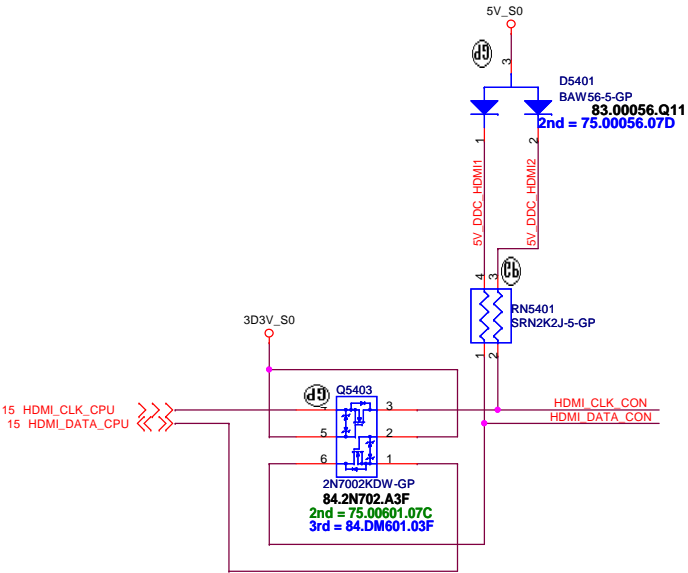
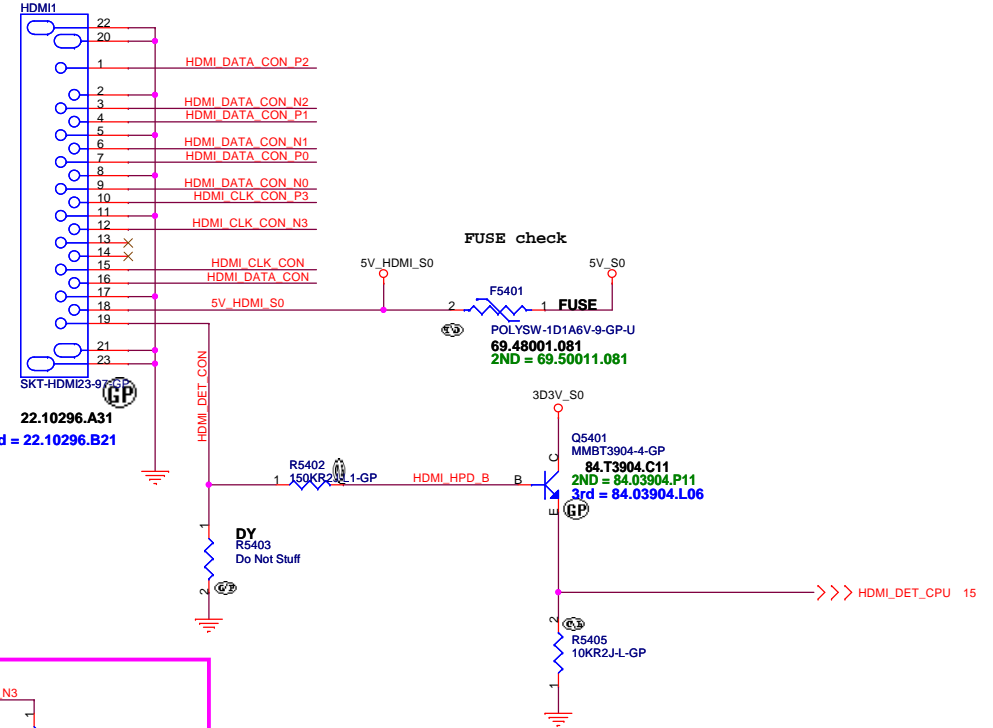
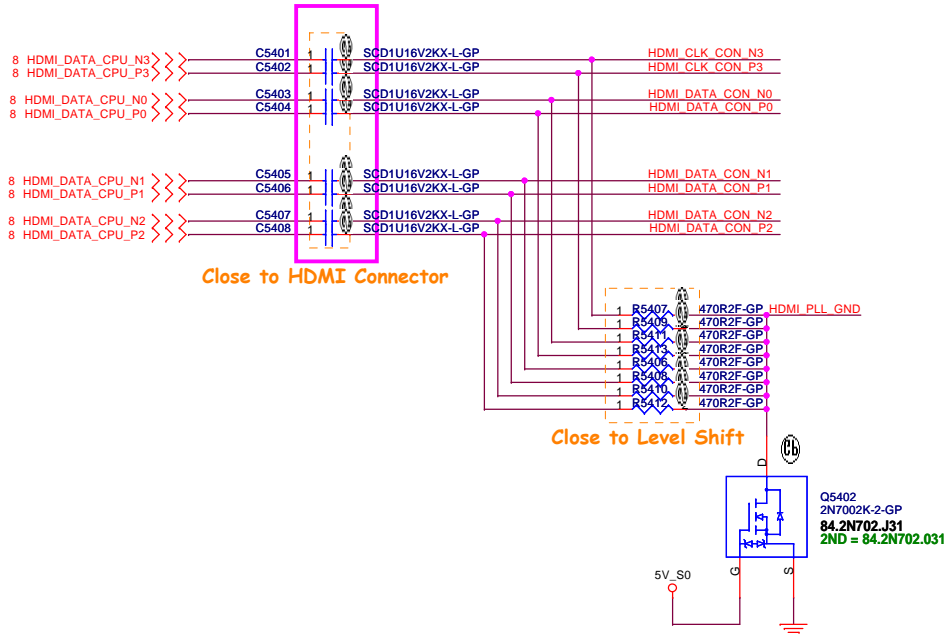
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SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

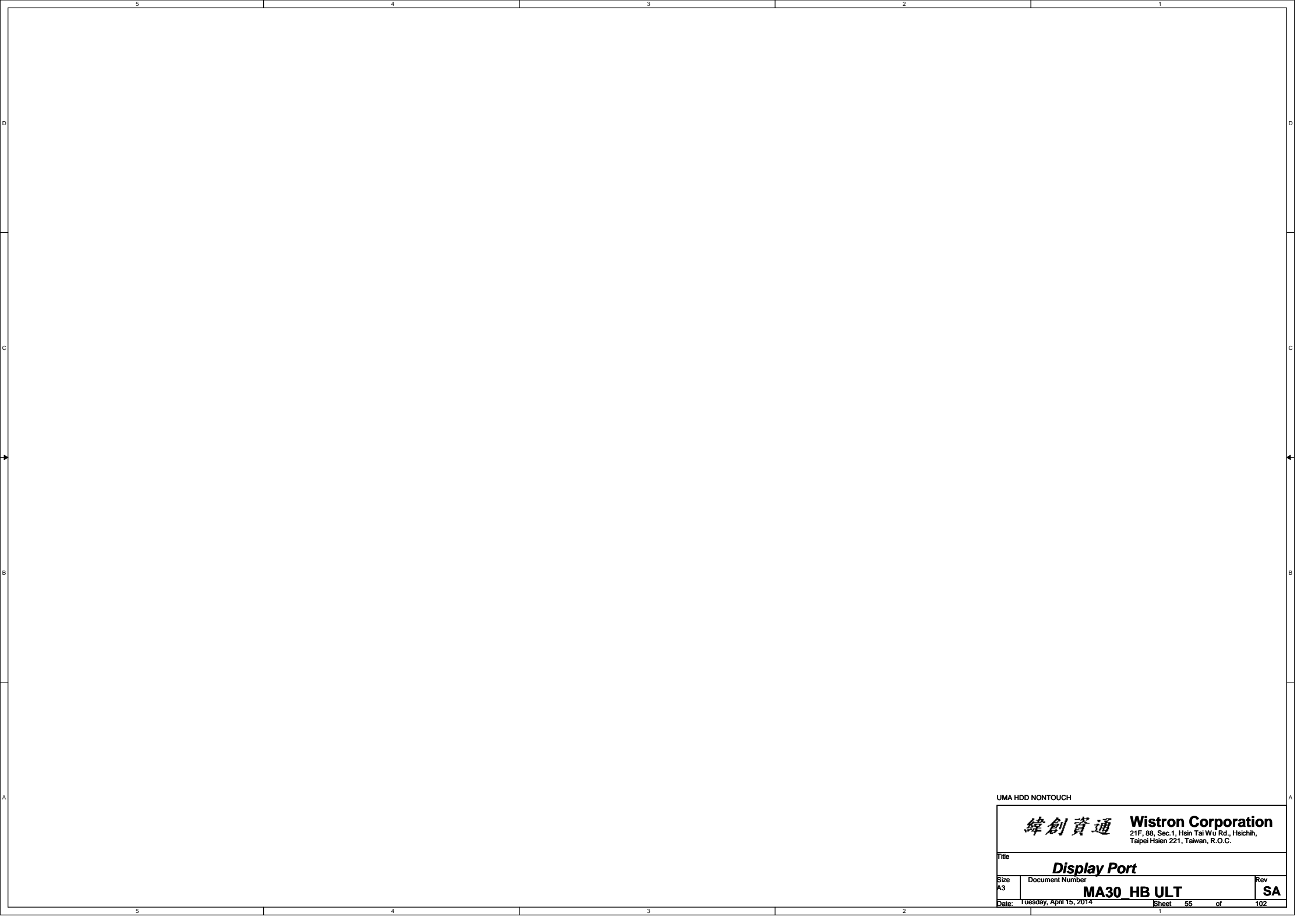


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Title HDMI Level Shifter/Connector		
Size A3	Document Number MA30 HB ULT	Rev SA
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Title

Display Port

Size
A3

Document Number

MA30 HB ULT

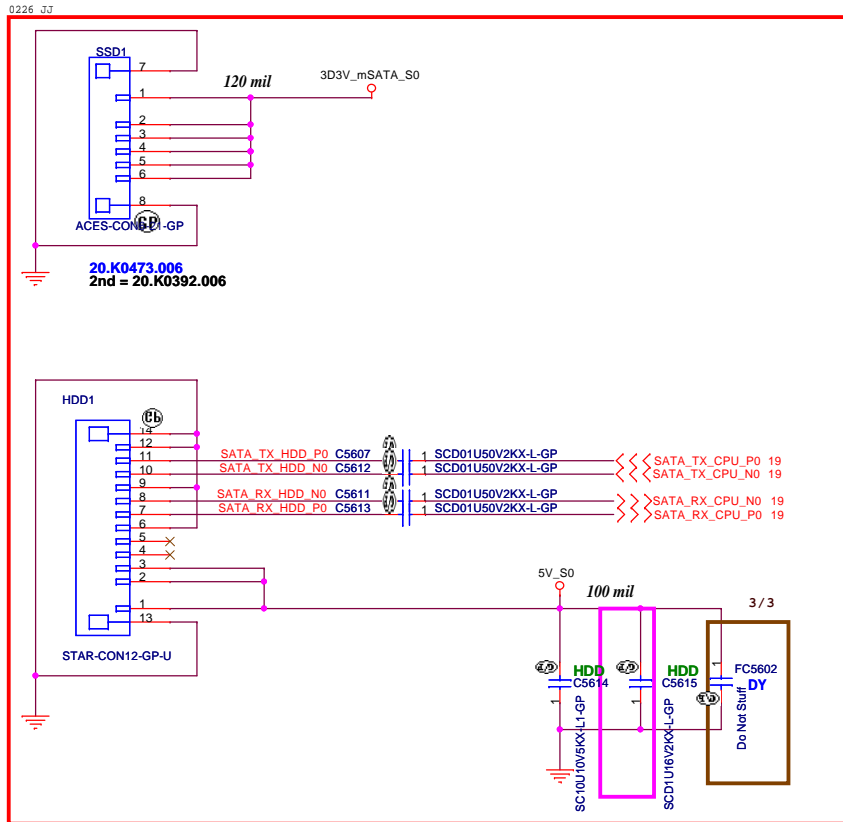
Rev

SA

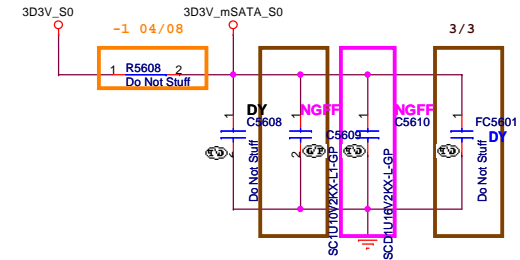
Date: **Tuesday, April 15, 2014**

Sheet **55** of **102**

SATA HDD Connector



AC coupling caps near connector < 100 mils
Delay HDD power off timing for 800ms-900ms after SATA controller shut down.



NGFF SSD Connector

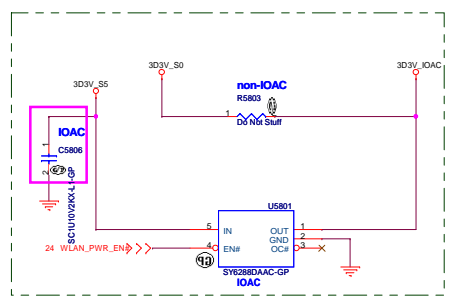
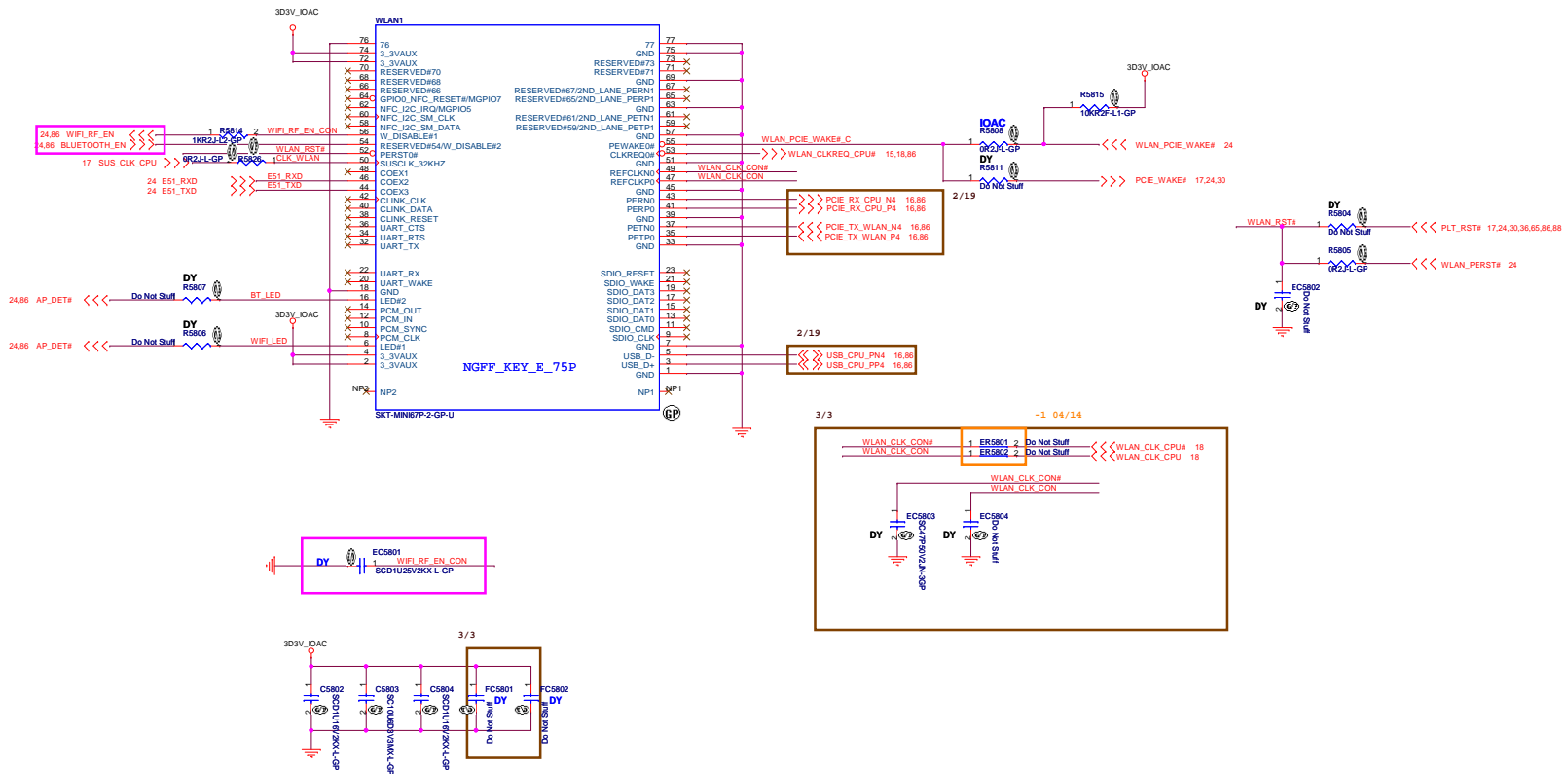
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HDD / ODD / NGFF SSD			
File	Document Number		
Size A3	MA30 HB ULT		Rev SA
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Title			
E-SATA			
Size A4	Document Number EA40 HB ULT		Rev 2
Date: Tuesday, April 15, 2014		Sheet 57	of 102



Debug Card Circuit

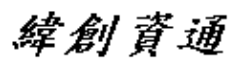
UMA HDD NONTOUCH			
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Title			
MINICARD(WLAN)			
Size A2	Document Number	Rev	
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Date: Tuesday, April 15, 2014	Sheet	68	of 102

SSID = Wireless

Mini Card Connector(mSATA)

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Title			
WWAN CONN			
Size A4	Document Number MA30 HB ULT		Rev 2
Date: Tuesday, April 15, 2014		Sheet 59	of 102

SSID = mSATA

Mini Card Connector(mSATA)

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Taipei Hsien 221, Taiwan, R.O.C.

Title

mSATA Connector

Size

A4

Document Number

MA30 HB ULT

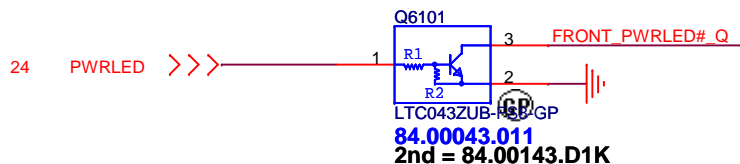
Rev

2

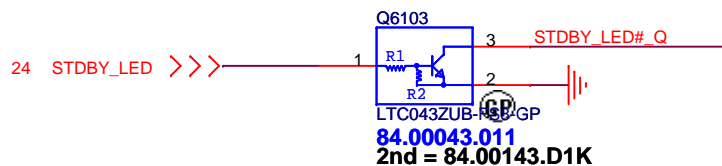
Date: Tuesday, April 15, 2014

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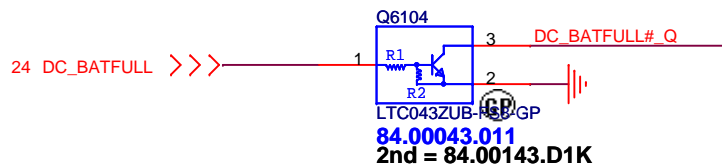
Power button_LED



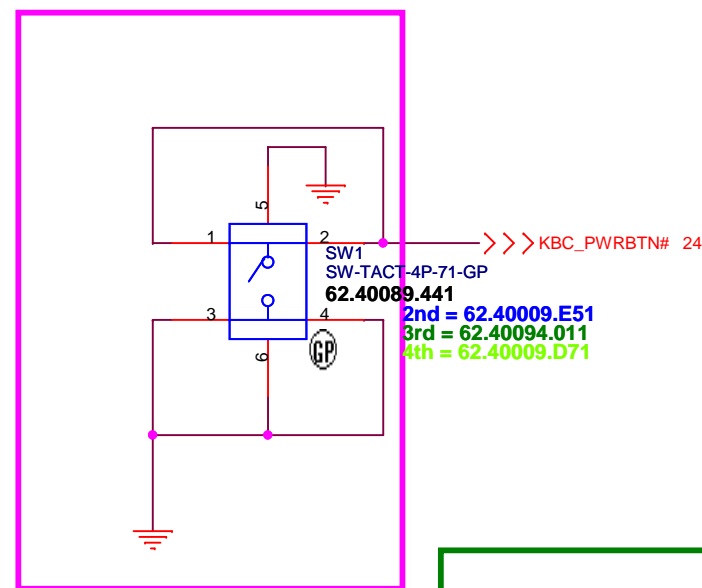
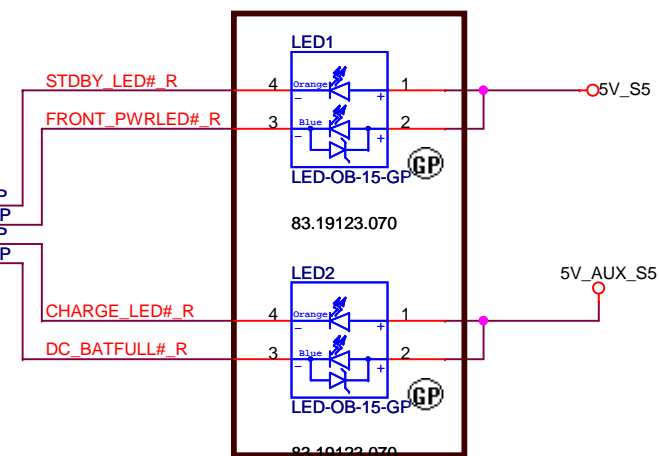
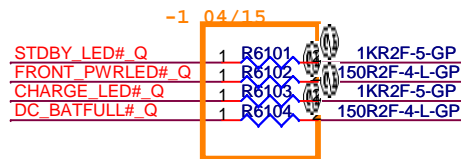
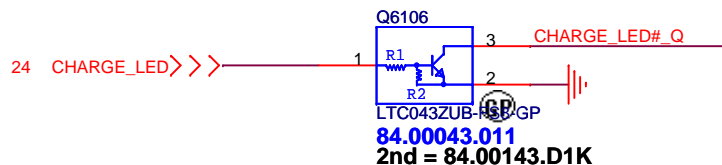
Power STDBY_LED



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)





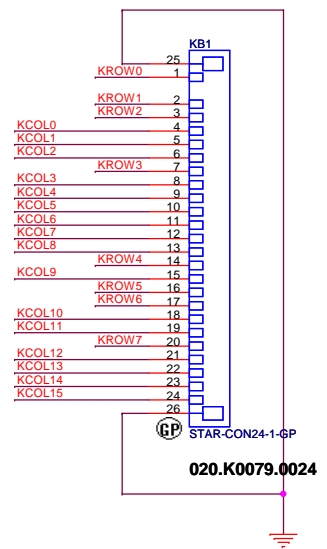
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Title LED Bard/Power Button		
Size A4	Document Number MA30 HB ULT	Rev SA
Date: Tuesday, April 15, 2014	Sheet 61	of 102

SSID = Key Board CN & TP CN

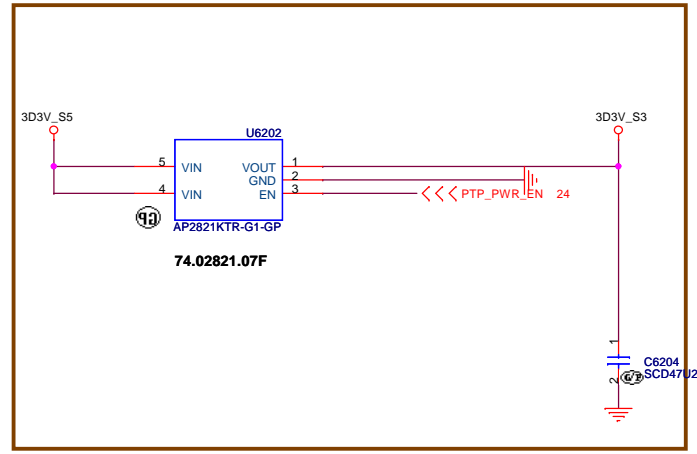
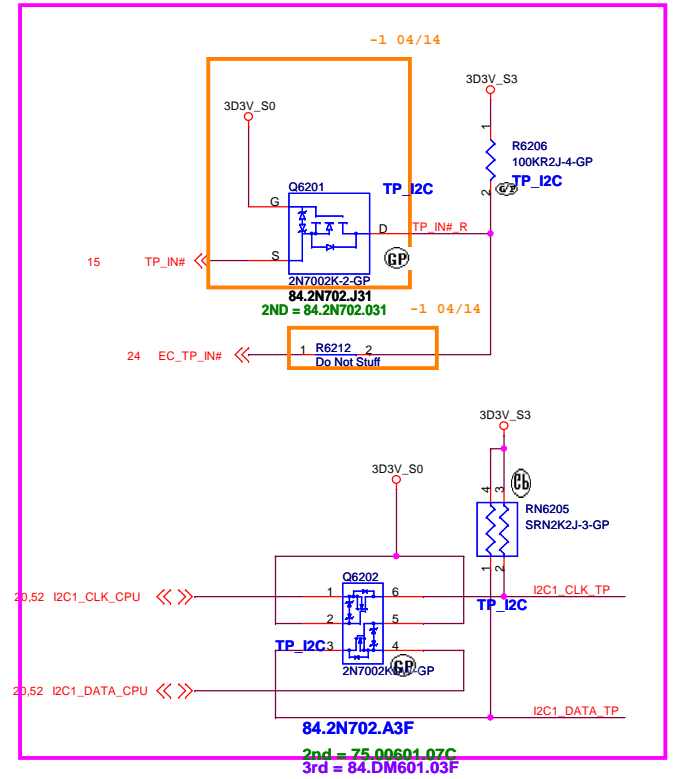
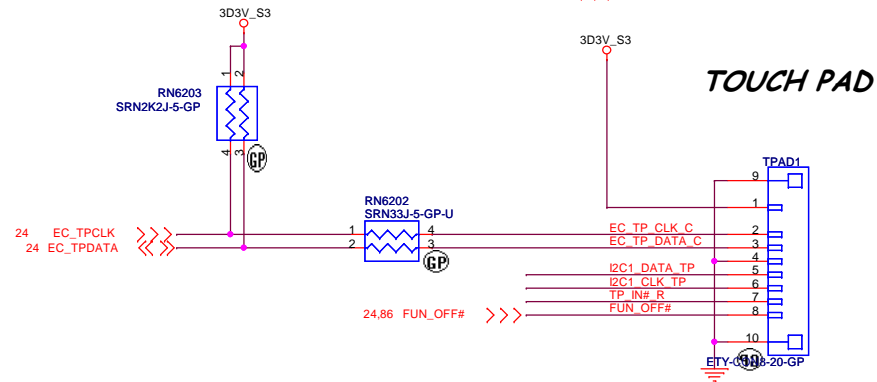
24,86 KROW[0..7] <<<>>> 
 24,86 KCOL[0..15] <<<>>> 



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1

86 EC_TP_CLK_C <<<>>> 
 86 EC_TP_DATA_C <<<>>> 
 86 I2C1_DATA_TP <<<>>> 
 86 I2C1_CLK_TP <<<>>> 
 86 TP_IN#_R <<<>>> 



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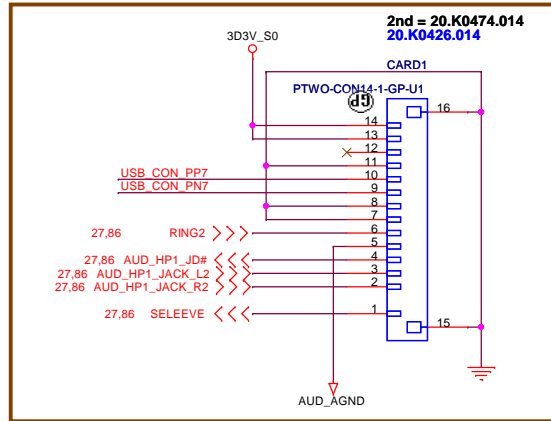
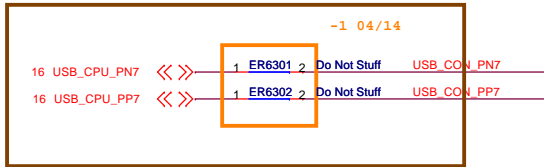
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Title **Key Board/Touch Pad**

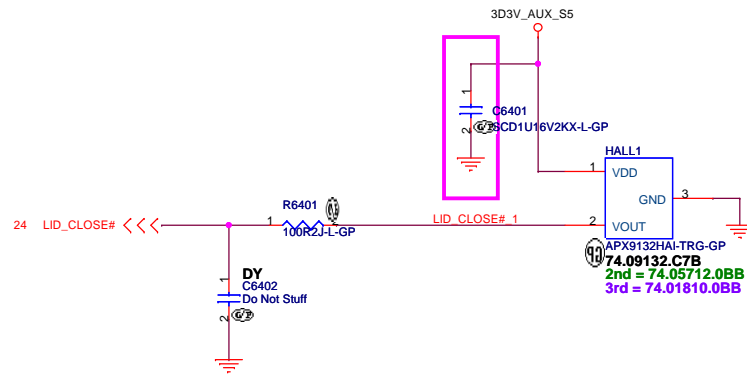
Size A3	Document Number MA30 HB ULT	Rev 2
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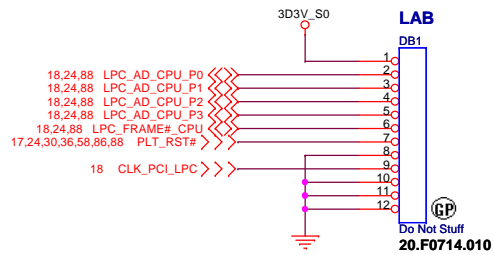
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Title			
IO Board Connector			
Size A3	Document Number MA30 HB ULT		Rev 2
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Title Hall Sensor		
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Title		
Dubug connector		
Size	Document Number	Rev
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Title		
SENSOR HUB		
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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Title

G Sensor

Size

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Title			
Thunderbolt (1/5)			
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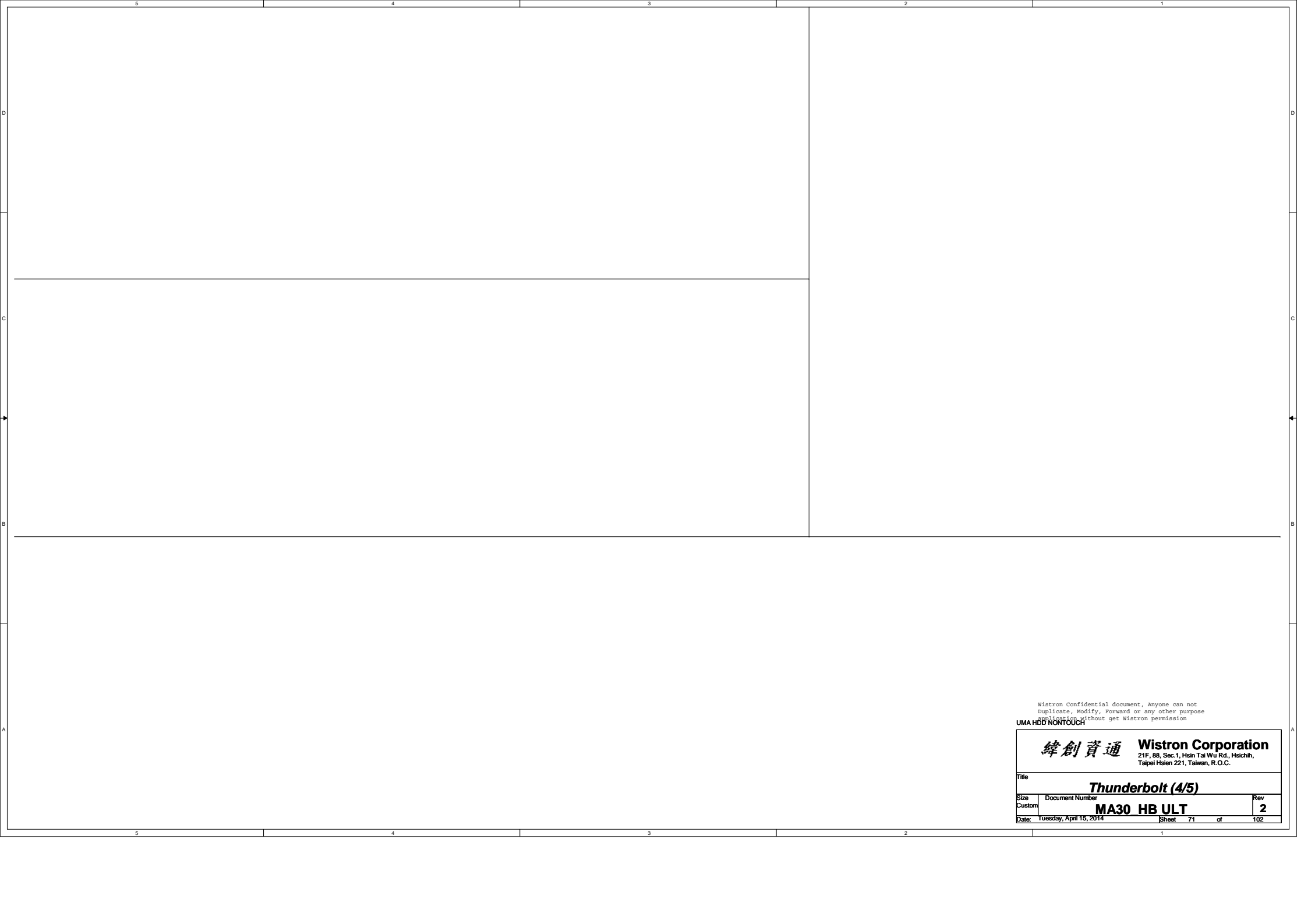
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Title			
Thunderbolt (2/5)			
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Title			
Thunderbolt (3/5)			
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Title			
Thunderbolt (4/5)			
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Title			
Thunderbolt (5/5)			
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Title		GPU(PEG)	
Size	Document Number	Rev	
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Title		
GPU (DIGITALOUT)		
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Title

GPU (VRAM I/F)

Size Document Number Rev

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GPU (POWER/GND)			
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GPU-VRAM1,2 (1/4)			
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Title		
GPU-VRAM3,4 (2/4)		
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GPU-VRAM5,6 (3/4)		
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Title		
GPU-VRAM7,8 (4/4)		
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Title		
RT8812A VGA CORE		
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DISCRETE VGA POWER			
Doc	Document Number	Rev	
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Doc	Version: 001 TO 014	03	01

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Switchable GFX LCD(1/2)			
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Switchable GFX LCD(2/2)			
Size A4	Document Number MA30 HB ULT		Rev 2
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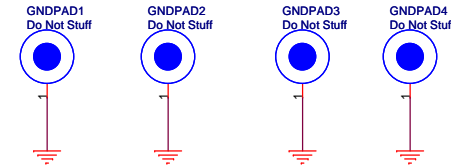
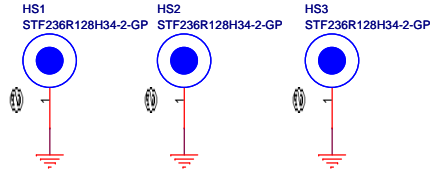
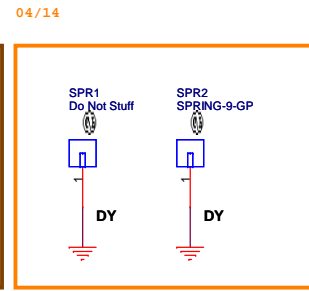
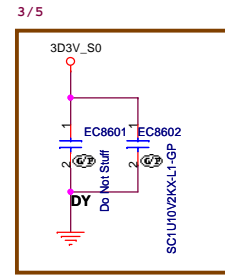
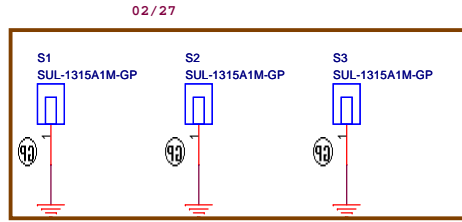
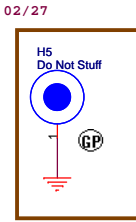
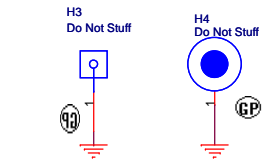
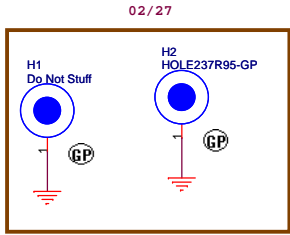
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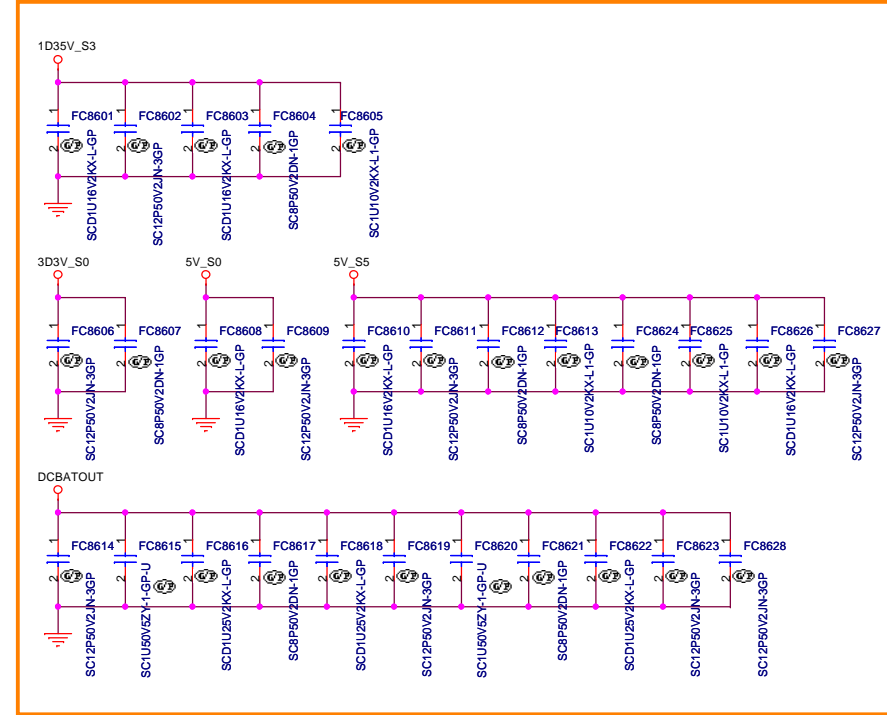
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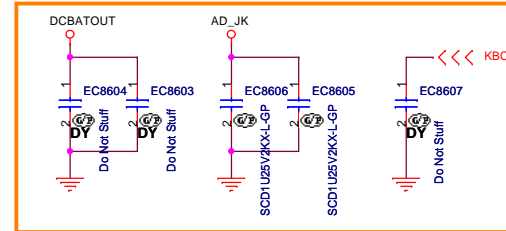
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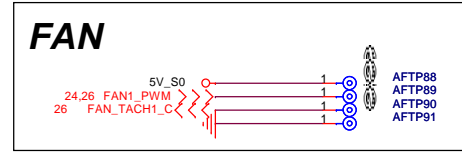
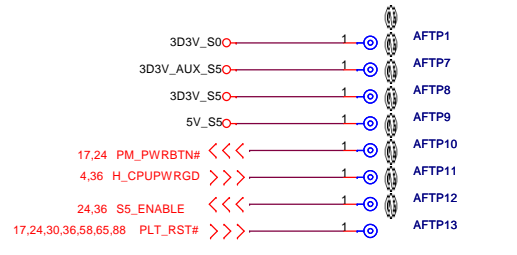


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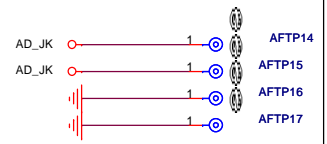
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Title UNUSED PARTS/EMI Capacitors		
Size A3	Document Number MA30 HB ULT	Rev 2
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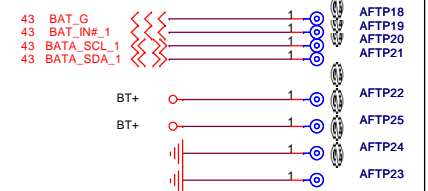
Check test point Test Point放在Dimm Door打開可量測處



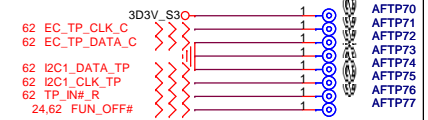
DCIN



BARRETY



Touch PAD



CARD BD

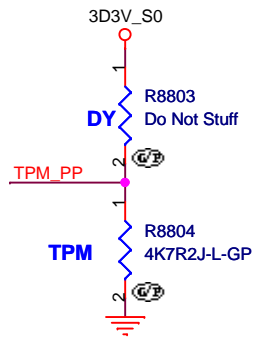
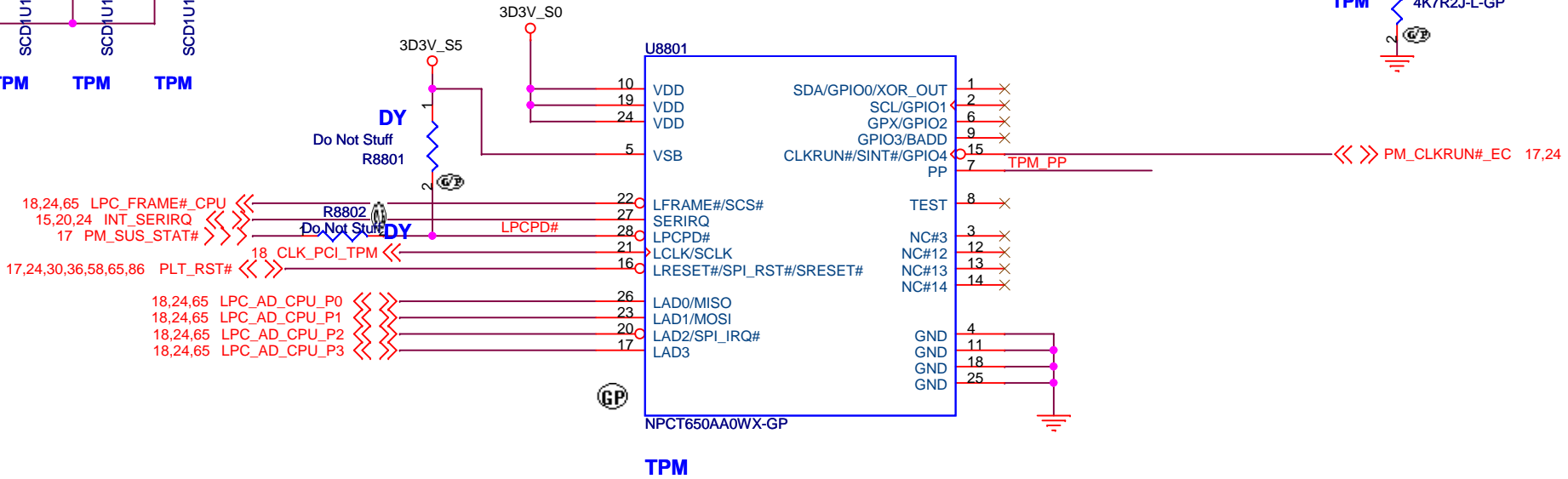
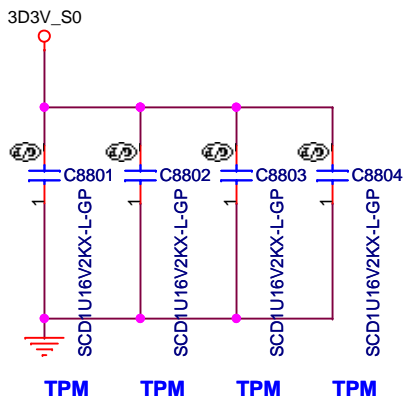


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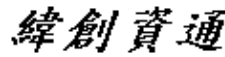
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Title		
NFC		
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TPM		
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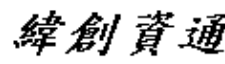
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Title **Express Card**

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Title **Smart Card socket**

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Title **Switchable GFX eDP**

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Title **Bottom Docking**

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Title		
Inter LAN WG1217LM		
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Title **LAN Switch**

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	JTAG_TMS	Open	NA	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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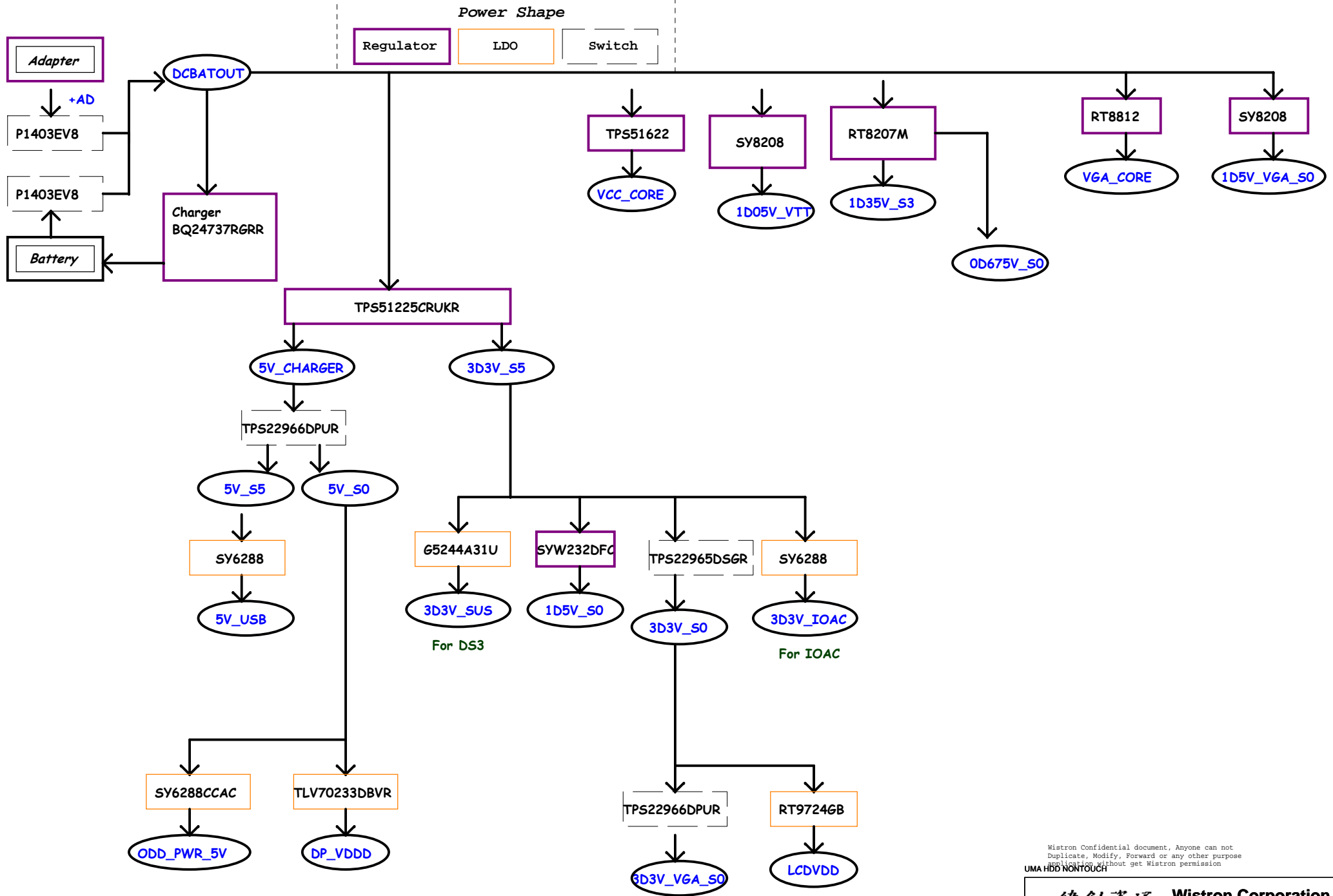
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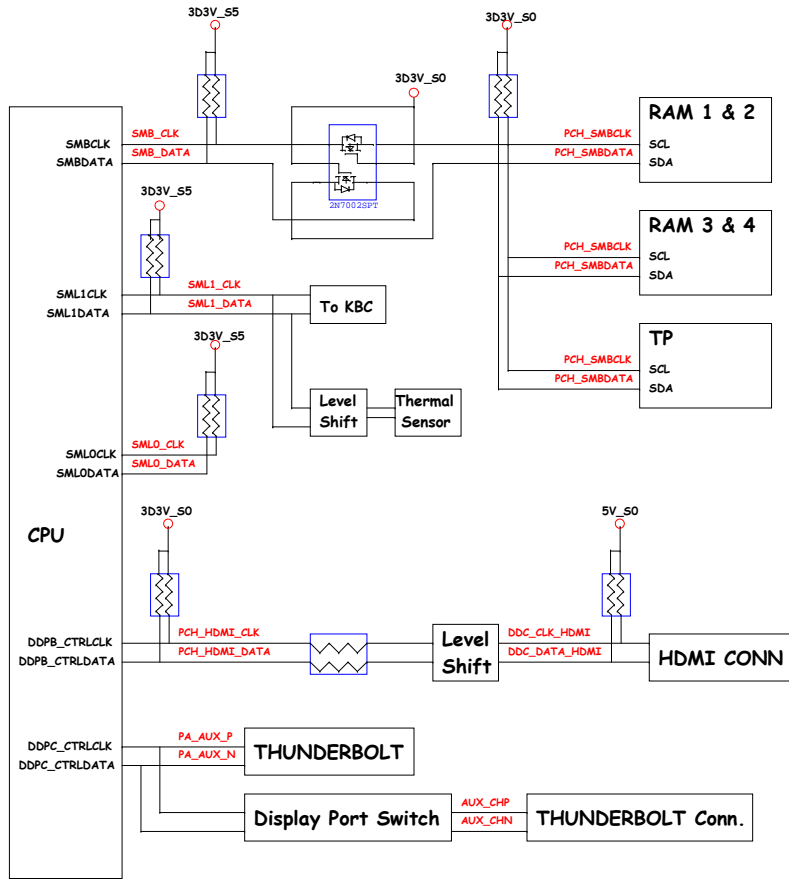
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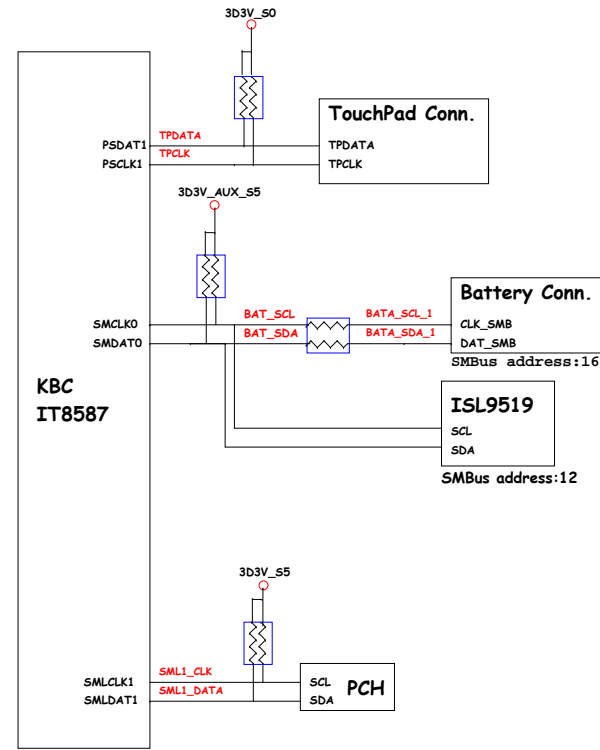
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PCH SMBus Block Diagram



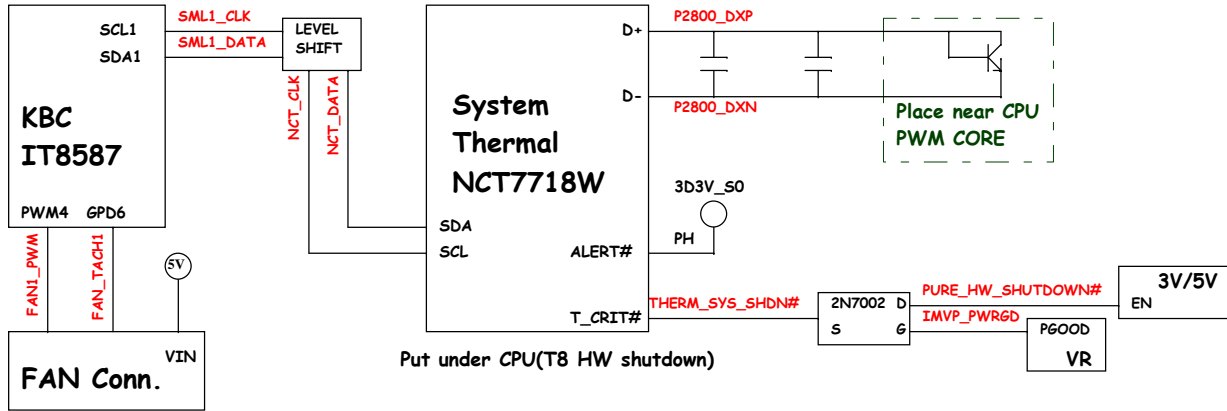
KBC SMBus Block Diagram



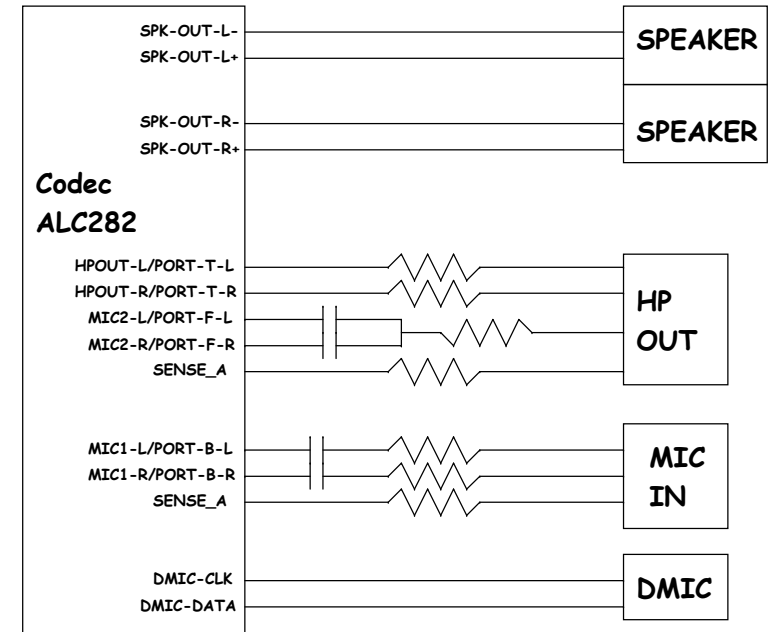
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Thermal Block Diagram



Audio Block Diagram



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Title **THERMAL/AUDIO BLOCK DIAGRAM**

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